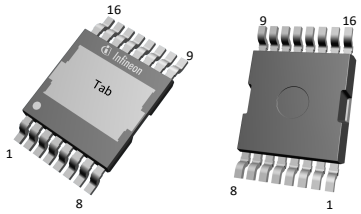
MOSFET

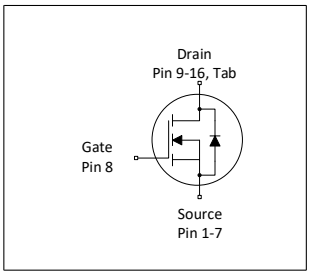
OptiMOS™ 5 Power-Transistor, 100 V

PG-HDSOP-16



Features

- Optimized for motor drives and battery powered applications
- Optimized for top side cooling
- High current capability
- 175°C rated
- 100% avalanche tested
- Superior thermal performance
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21



Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	1.9	mΩ
I_D	279	A
Q_{oss}	163	nC
Q_G	128	nC

Type / Ordering Code	Package	Marking	Related Links
IPTC019N10NM5	PG-HDSOP-16	19N10NM5	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- - - -	- - - -	279 197 169 31	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=6 V, T_C=100 °C V_{GS}=10 V,T_A=25 °C,R_{thJA}=40°C/W[2)]
Pulsed drain current[3)]	$I_{D,pulse}$	-	-	1116	A	T_A=25 °C
Avalanche energy, single pulse[4)]	E_{AS}	-	-	400	mJ	I_D=130 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	300 3.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W[2)]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, Top	R_{thJC}	-	-	0.5	°C/W	-
Thermal characterization parameter, junction to lead (Pin 1-7)[5)]	Ψ_{JL}	-	9	-	°C/W	-
Thermal characterization parameter, junction to lead (Pin 9-16)[5)]	Ψ_{JL}	-	3	-	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	40	-	°C/W	-

[1)] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3)] See Diagram 3 for more detailed information
[4)] See Diagram 13 for more detailed information
[5)] Ψ_{JL} is a temperature characterization parameter according to JESD51-12 referring to the temperature difference between junction and leads in the case of natural convection. It can be used to estimate the component junction temperature in the application by measuring the temperature at the leads in the stated application environment

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3	3.8	V	V_{DS}=V_{GS}, I_D=210 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	5 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	1.6 2.0	1.9 2.6	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=6 V, I_D=65 A
Gate resistance	R_G	-	1.2	-	Ω	-
Transconductance	g_{fs}	-	240	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	9100	12000	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	1400	1800	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	61	110	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	21	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=3.5 Ω
Rise time	t_r	-	11	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=3.5 Ω
Turn-off delay time	$t_{d(off)}$	-	49	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=3.5 Ω
Fall time	t_f	-	38	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=3.5 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	41	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	27	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate to drain charge[1)]	Q_{gd}	-	26	39	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	40	-	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate charge total[1)]	Q_g	-	128	160	nC	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	163	217	nC	V_{DS}=50 V, V_{GS}=0 V

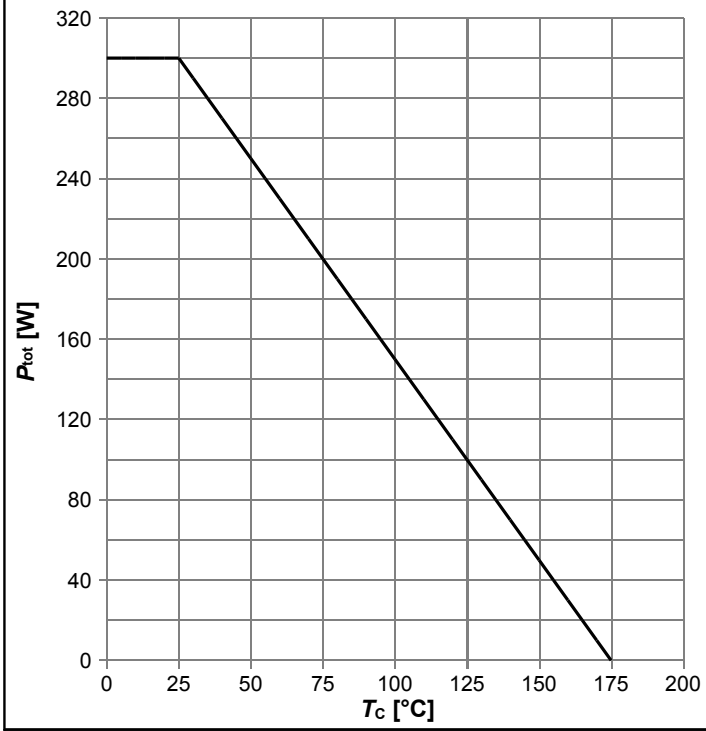
[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	256	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1116	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.86	1	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	79	-	ns	V_R=50 V, I_F=50 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	177	-	nC	V_R=50 V, I_F=50 A, di_F/dt=100 A/µs

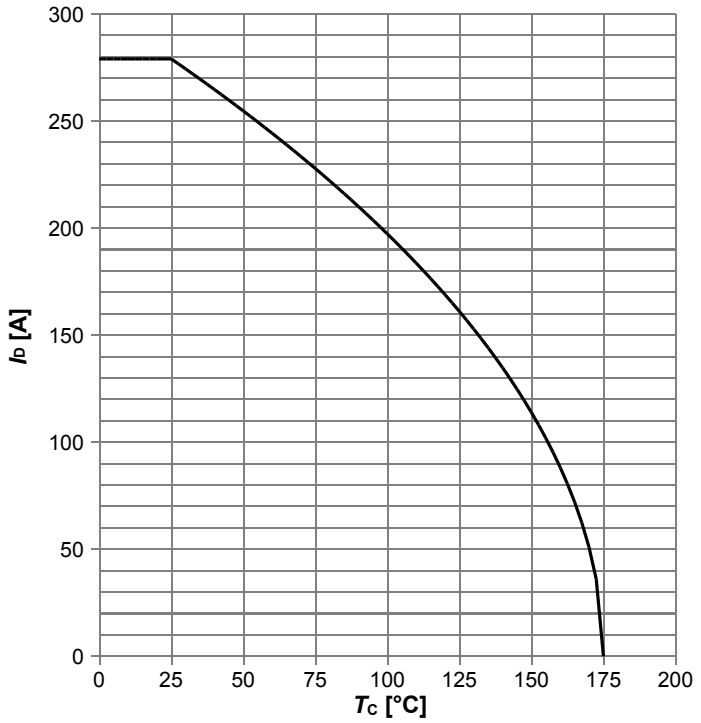
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



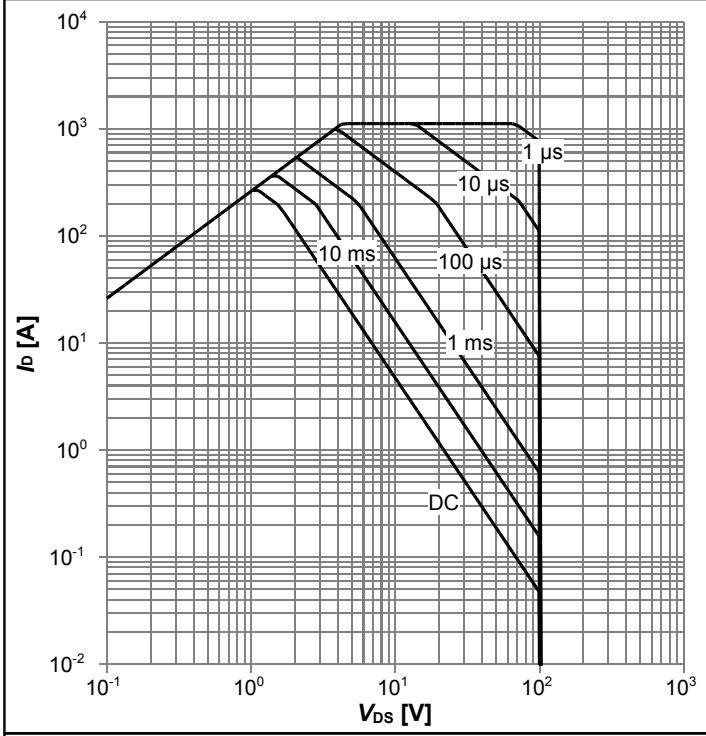
$P_{tot}=f(T_C)$

Diagram 2: Drain current



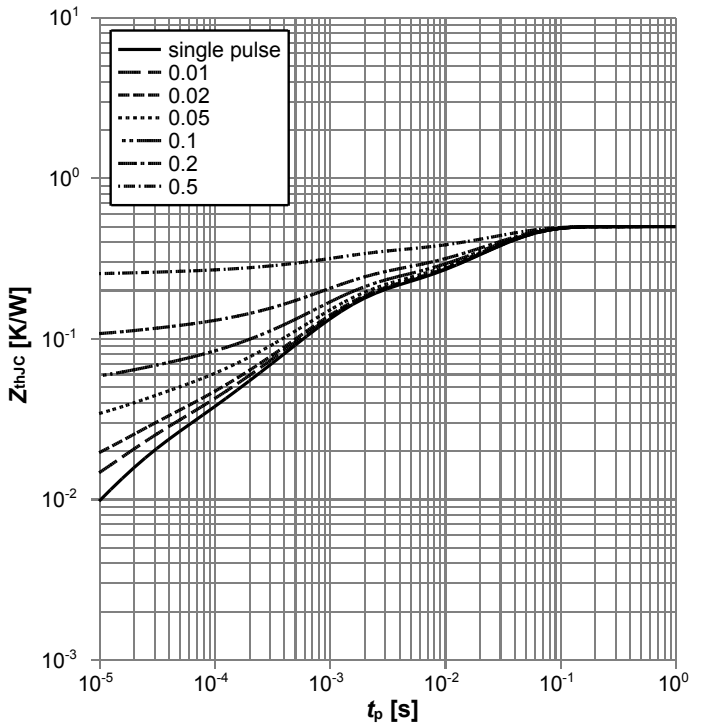
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



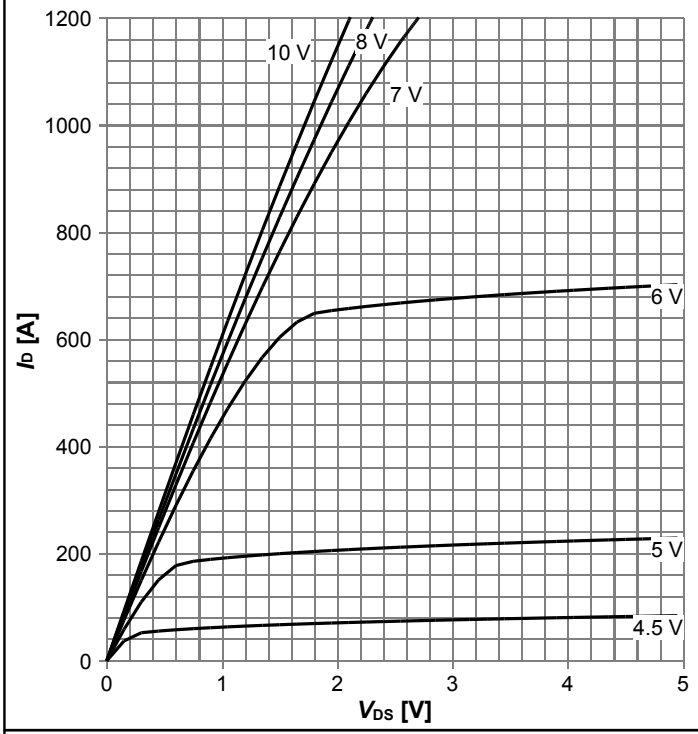
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



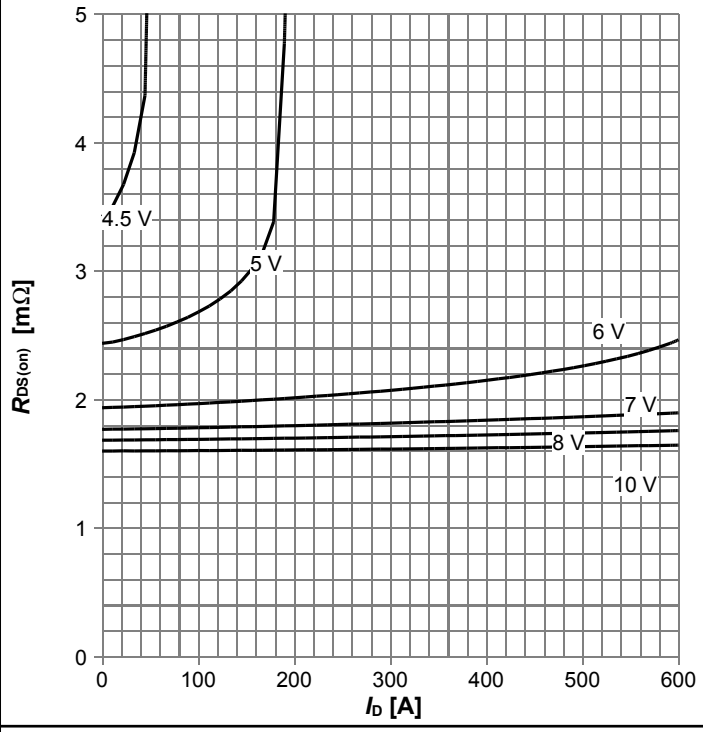
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



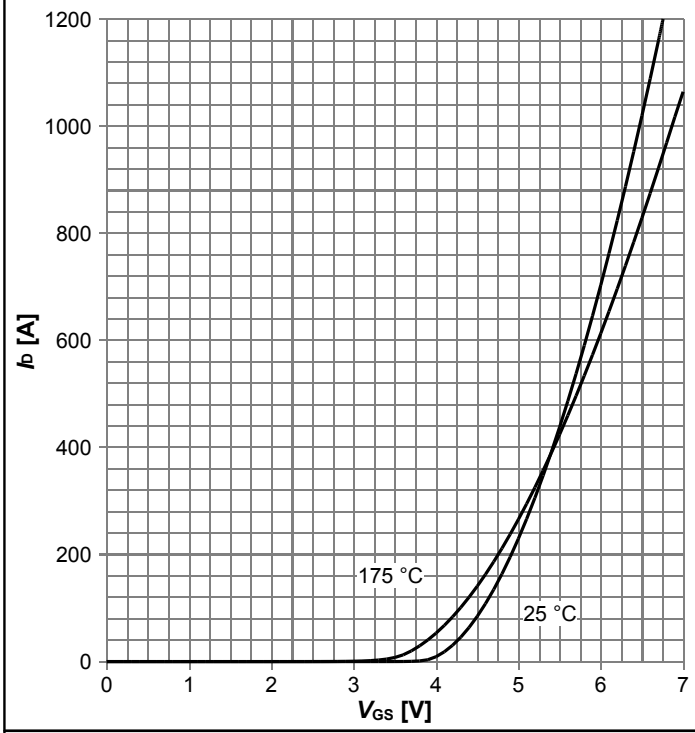
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



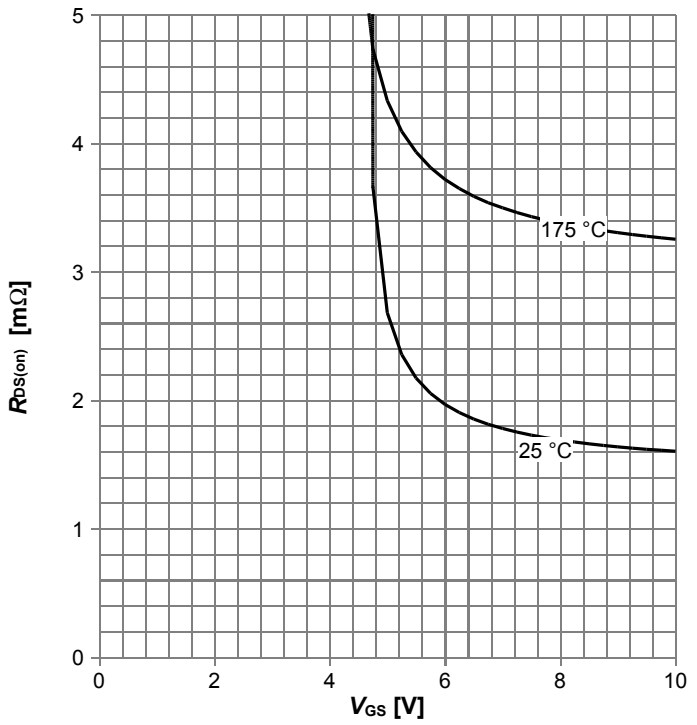
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



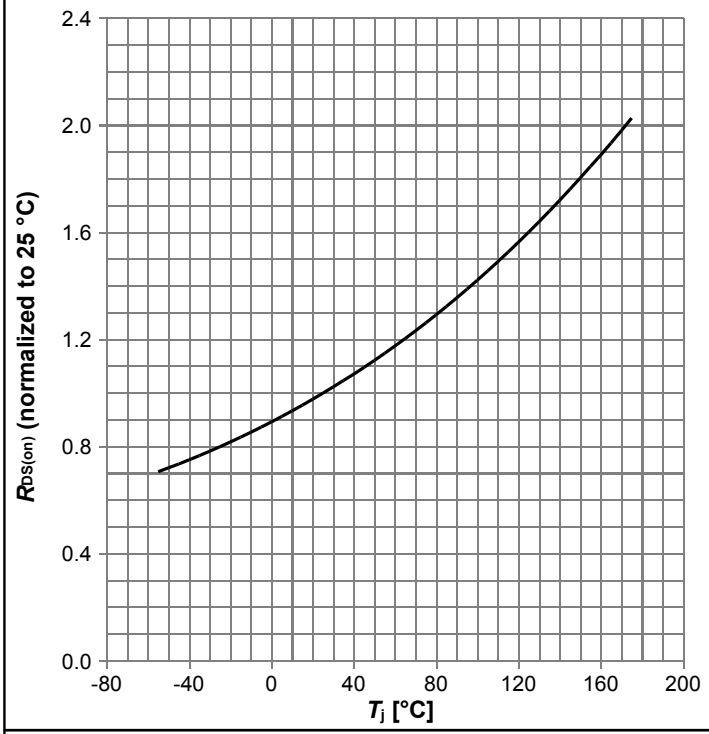
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



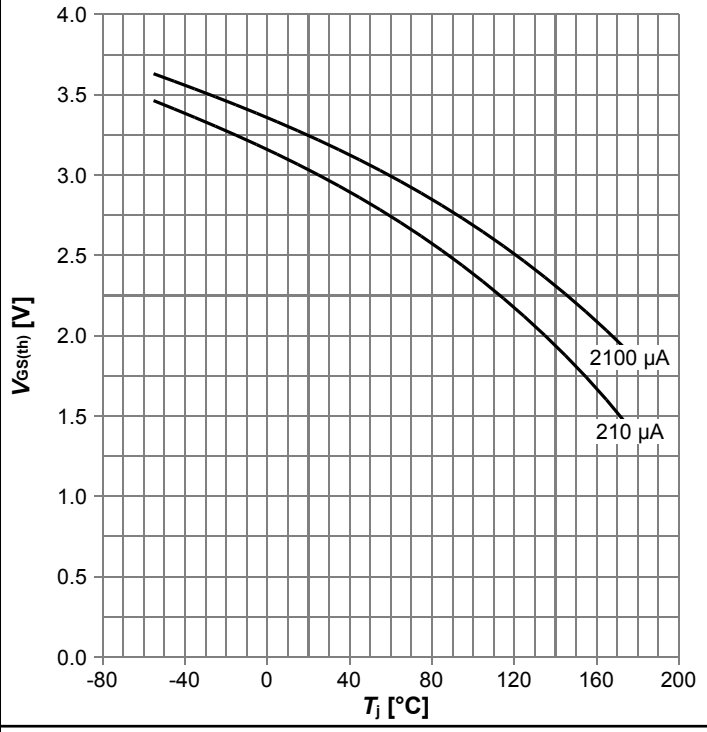
$R_{DS(on)}$=f(V_{GS}), I_D=100 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



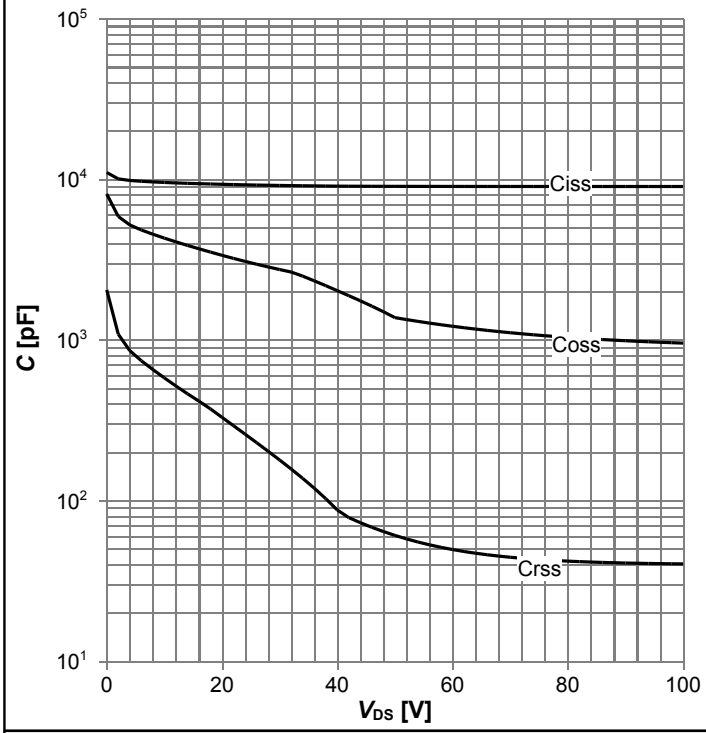
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



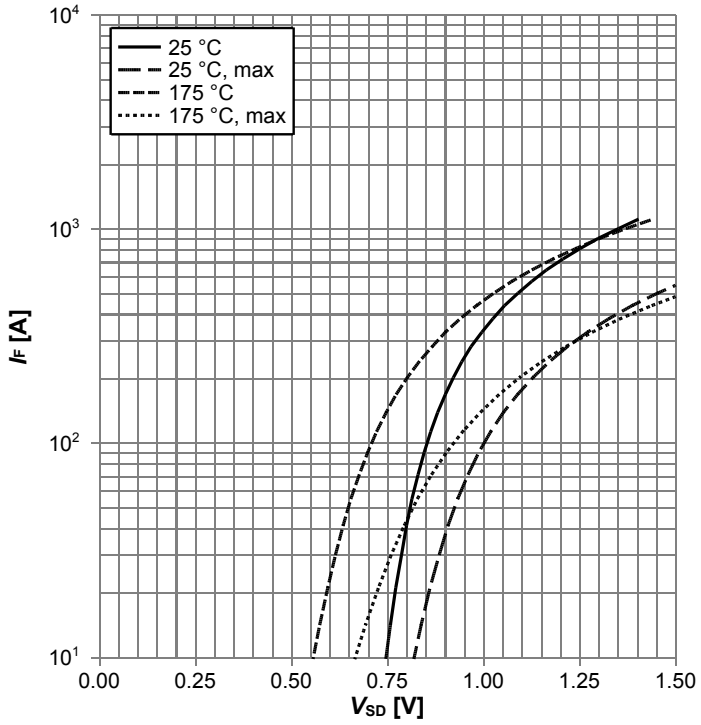
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



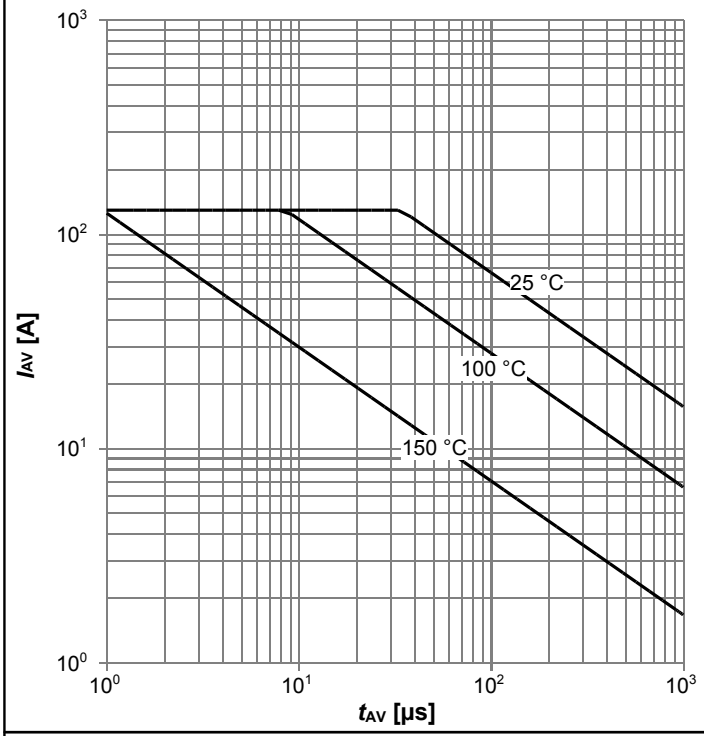
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



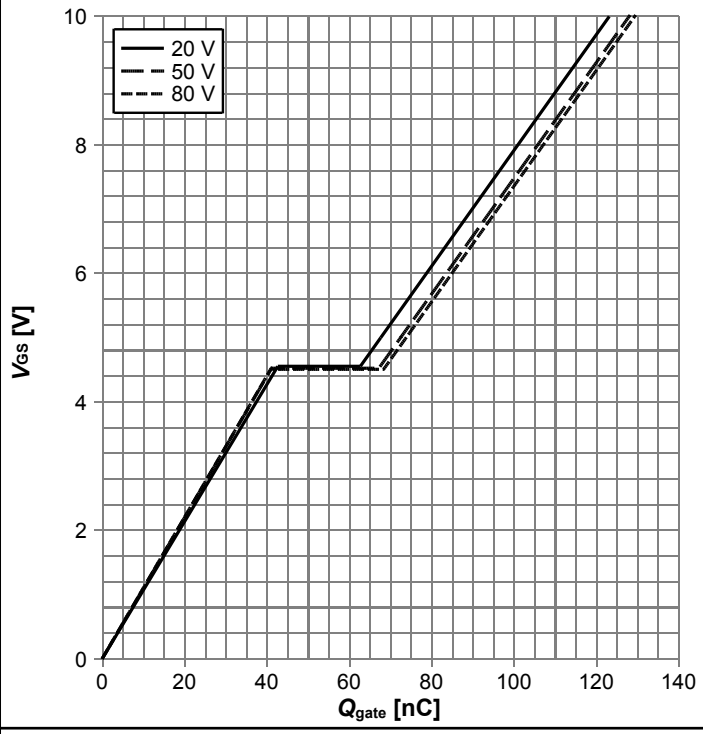
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



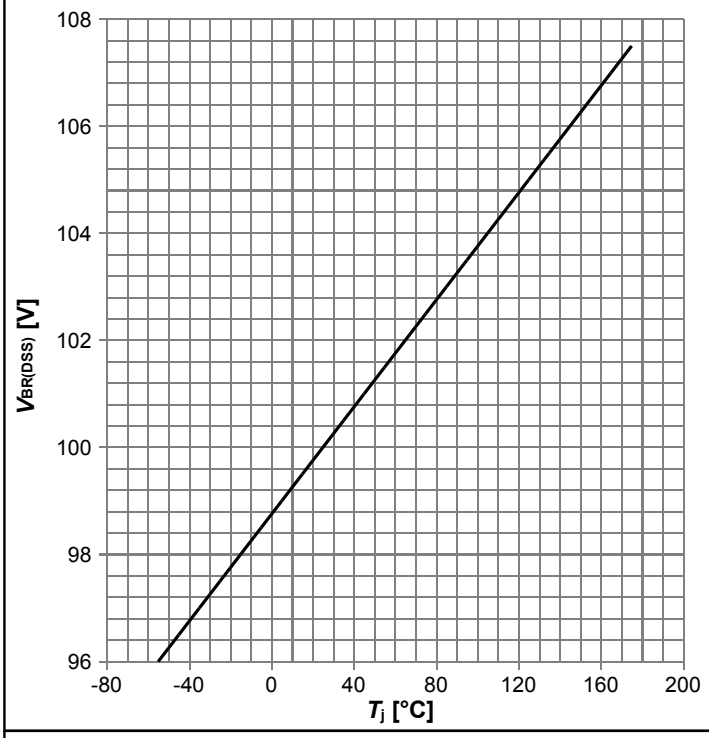
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



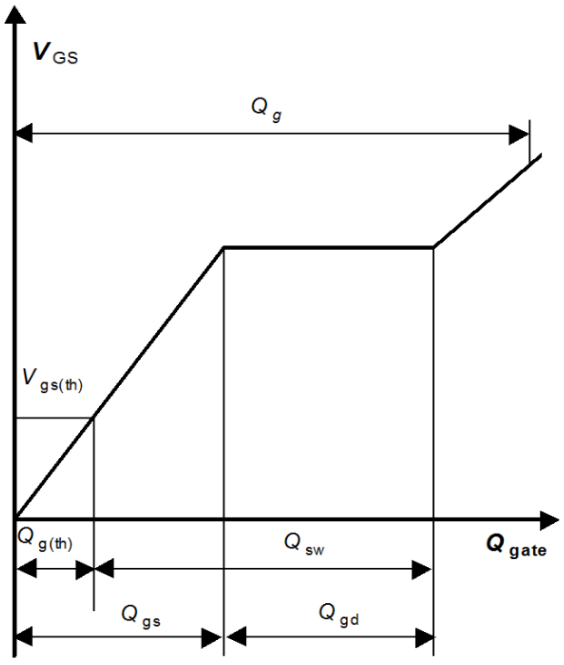
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

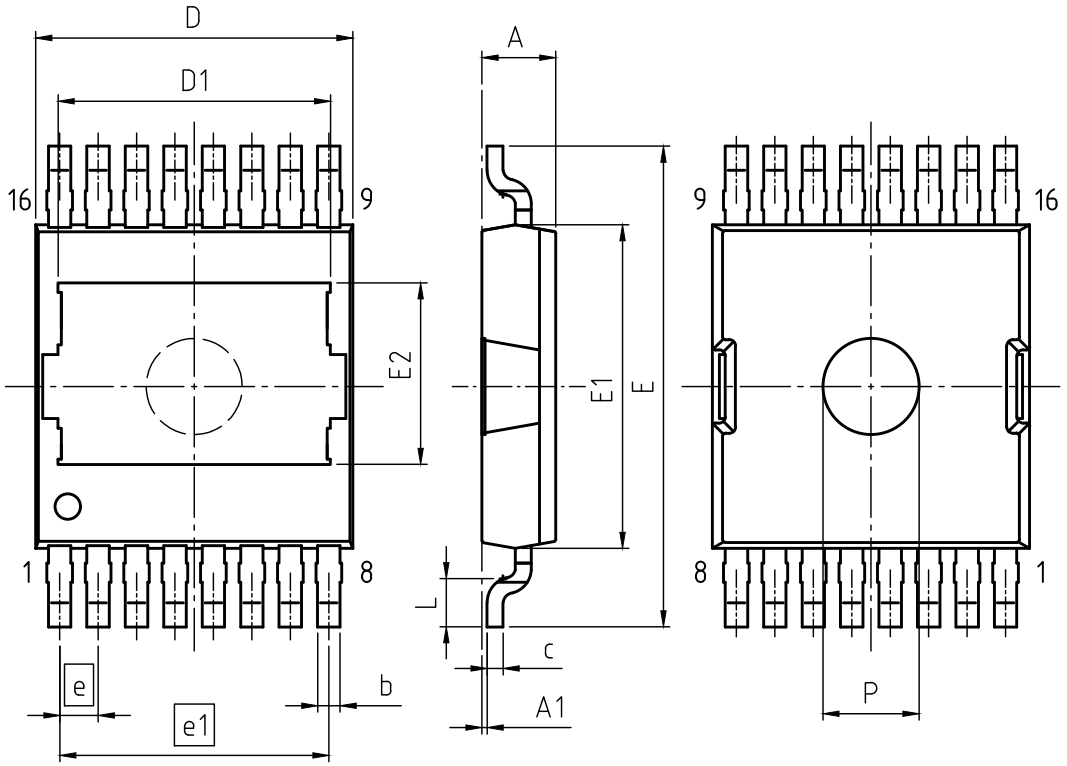


$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-HDSOP-16-U01	
REVISION: 01	DATE: 18.12.2020	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	2.25	2.35
A1	0.01	0.16
b	0.60	0.80
c	0.40	0.60
D	9.70	10.10
D1	8.20	8.40
E	14.80	15.20
E1	10.00	10.30
E2	5.57	5.77
e	1.20	
e1	8.40	
L	1.40	1.60
P	2.90	3.10

Figure 1 Outline PG-HDSOP-16, dimensions in mm

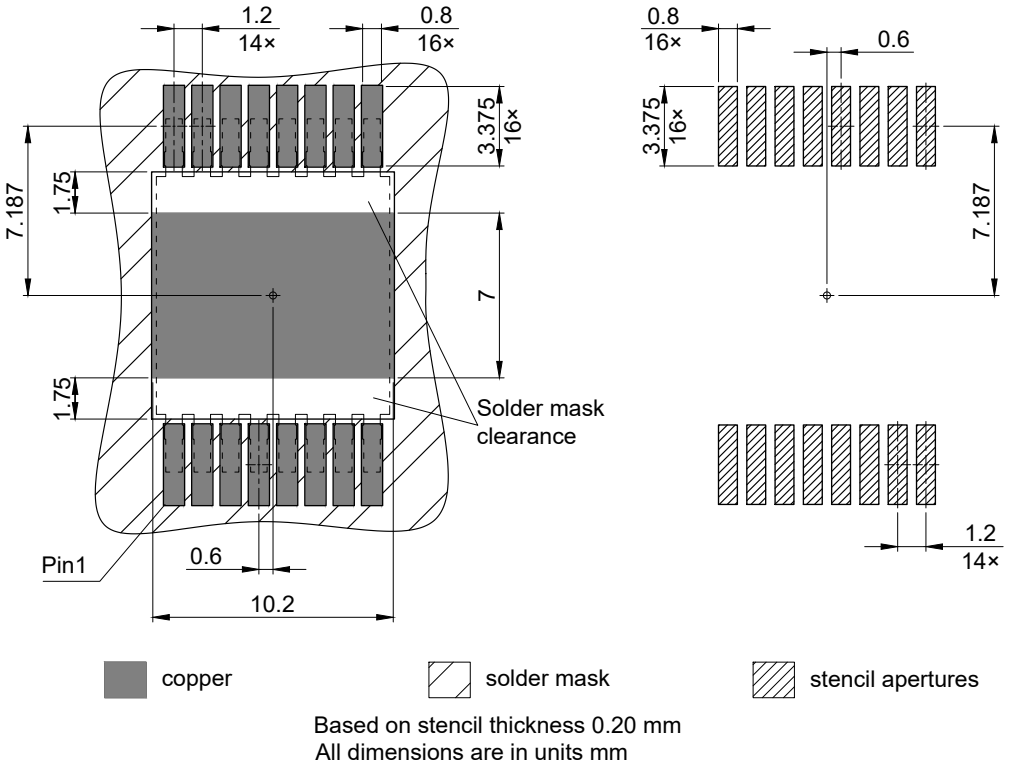
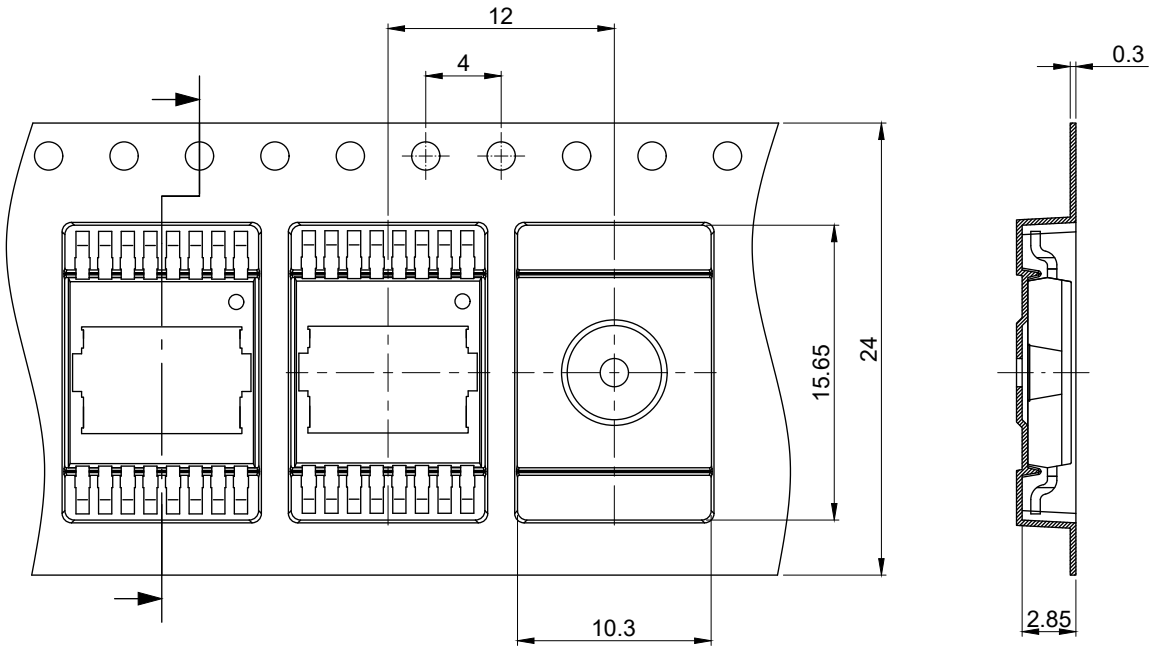


Figure 2 Outline Footprint (PG-HDSOP-16), dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Outline Tape (PG-HDSOP-16), dimensions in mm

Revision History

IPTC019N10NM5

Revision: 2022-05-10, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2021-02-02	Release of final version
2.1	2022-05-10	Update package drawings and Idss max at 25°C

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Infineon Technologies AG
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