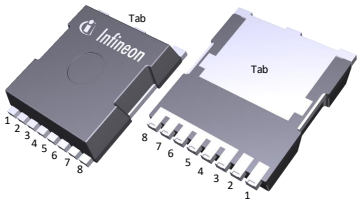
MOSFET

TOLL

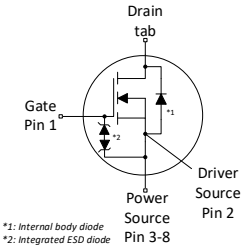
600V CoolMOS™ CM8 Power Transistor



Built on Infineon's world-class super-junction MOSFET platform with an integrated fast body diode, making it suitable for a wide range of applications. It enables highest power density at lowest possible system cost with superior reliability. It is enhancing Infineon's WBG offering and the successor of the 600 V CoolMOS™ 7 MOSFET family.

Features

- Best-In-Class SJ Mosfet Performance
- Address broad hard and soft switching applications with outstanding commutation ruggedness
- Integrated fast body diode and ESD protection
- .XT interconnection technology for best-in-class thermal performance



Benefits

- Provides the best price performance ratio with Best-In-Class SJ Mosfet Performance
- Ease of use and shorter design in cycle
- Enable multiple topologies
- 14-42% lower R_{th} for improved thermal performance

Potential applications

- Datacenter, AI server, Telecom Power Supply
- Micro and Residential Hybrid Inverter
- Portable and Residential Energy Storage, UPS
- EV Charging, Light electric vehicles, Electric Forklift
- High Voltage Solid State Power Distribution
- Home & Professional Tools
- Charger, Adapters, TV and Console SMPS

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	120	mΩ
$Q_{g,typ}$	24	nC
$I_{D,pulse}$	68	A
E_{oss} @ 400V	3.4	µJ
Body diode di_F/dt	1300	A/µs
ESD class (HBM)	2	

Type / Ordering code	Package	Marking	Related links
IPT60R120CM8	PG-HSOF-8	60R120C8	see Appendix A

Table of contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	24	A	T_C=25°C
Continuous drain current	I_D	-	-	15	A	T_C=100°C
Pulsed drain current [2]	$I_{D,pulse}$	-	-	68	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	40	mJ	I_D=2.2A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.20	mJ	
Avalanche current, single pulse	I_{AS}	-	-	2.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	154	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	
Extended operating junction temperature	T_j	150	-	175	°C	≤50 h in the application lifetime
Mounting torque	-	-	-	-	Ncm	-
Continuous diode forward current	I_S	-	-	24	A	T_C=25°C
Diode pulse current [2]	$I_{S,pulse}$	-	-	68	A	
Reverse diode dv/dt [3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}≤24A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/µs	
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j,max}$.

[2] Pulse width t_p limited by $T_{j,max}$

[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.81	K/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	K/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	K/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.7	4.2	4.7	V	V_{DS}=V_{GS}, I_D=0.2mA
Zero gate voltage drain current	I_{DSS}	- -	- 31.2	1 -	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	1.2	µA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.100 0.22	0.120 -	Ω	V_{GS}=10V, I_D=8.3A, T_j=25°C V_{GS}=10V, I_D=8.3A, T_j=150°C
Gate resistance	R_G	-	9.8	-	Ω	f=1MHz

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1045	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	15	-	pF	
Effective output capacitance, energy related [4]	$C_{o(er)}$	-	42	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related [5]	$C_{o(tr)}$	-	421	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	16.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=4.0A, R_G=10.0Ω; see table 9
Rise time	t_r	-	6	-	ns	
Turn-off delay time	$t_{d(off)}$	-	89.5	-	ns	
Fall time	t_f	-	10.6	-	ns	

[4] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

[5] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 6 Gate charge characteristics

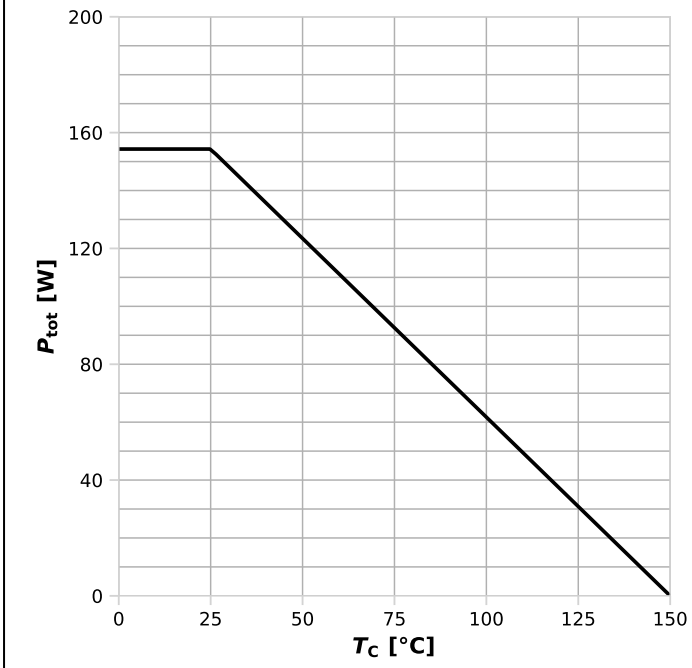
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	V_{DD}=400V, I_D=4.0A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	9	-	nC	
Gate charge total	Q_g	-	24	-	nC	
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=4.0A, T_j=25°C
Reverse recovery time	t_{rr}	-	69.53	86.91	ns	V_R=400V, I_F=4.0A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.24	0.36	µC	
Peak reverse recovery current	I_{rrm}	-	6.87	-	A	

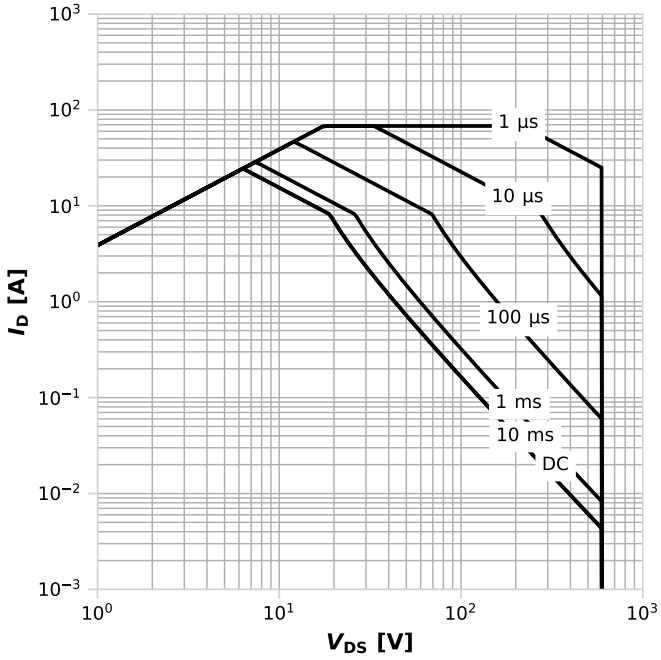
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



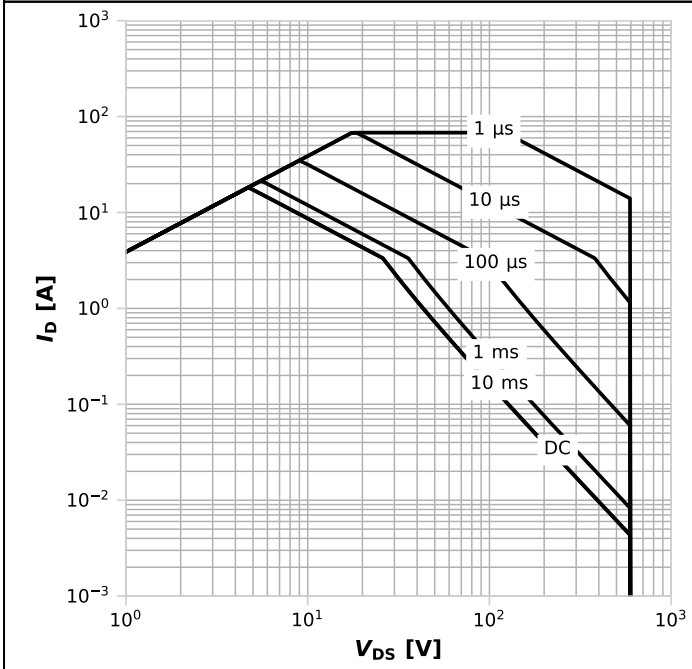
P_{tot}=f(T_C)

Diagram 2: Safe operating area



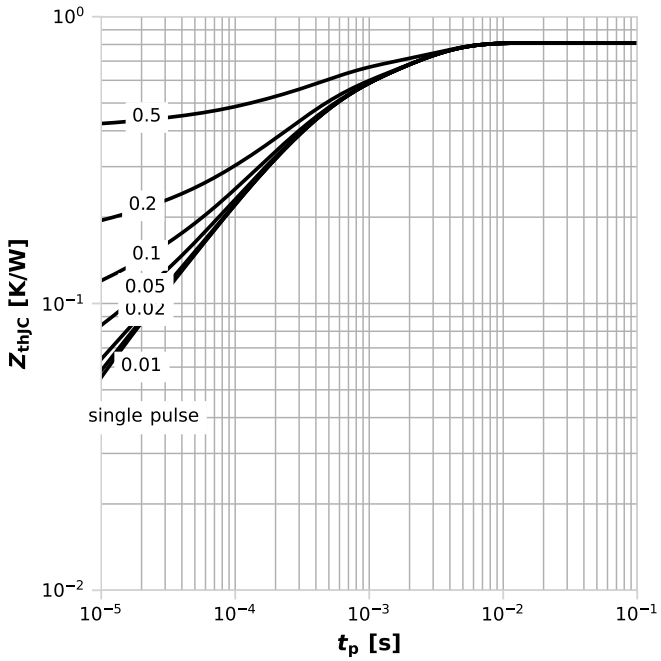
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

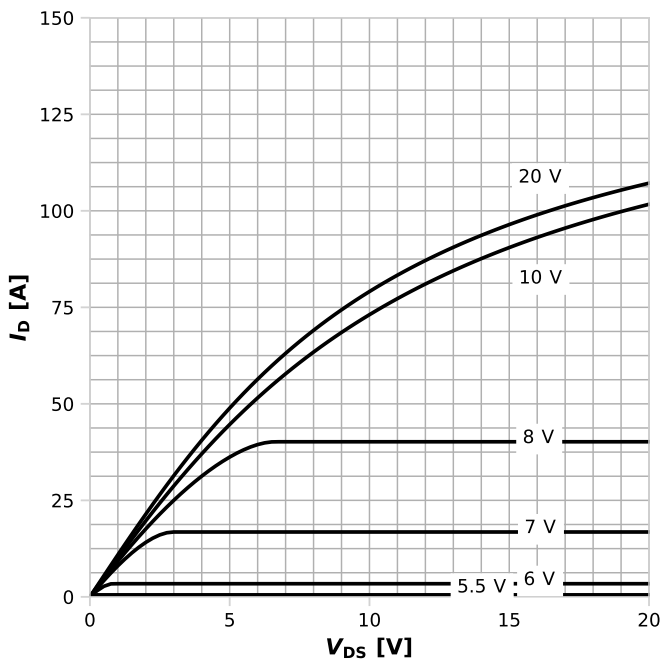
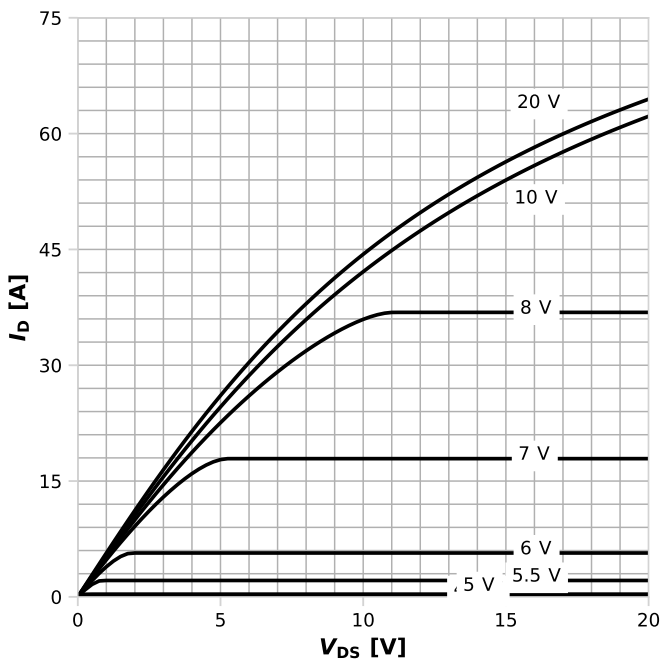
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
$I_D=f(V_{DS})$; T_j=25 °C; parameter: V_{GS}	$I_D=f(V_{DS})$; T_j=125 °C; parameter: V_{GS}

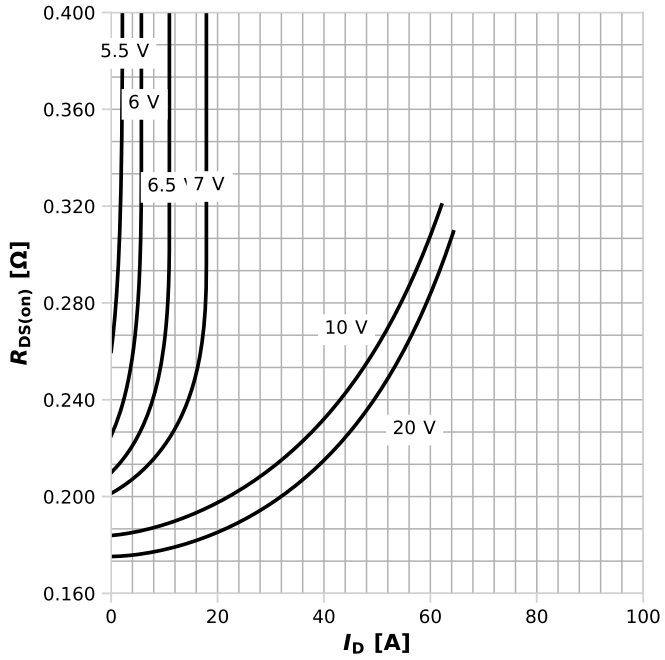
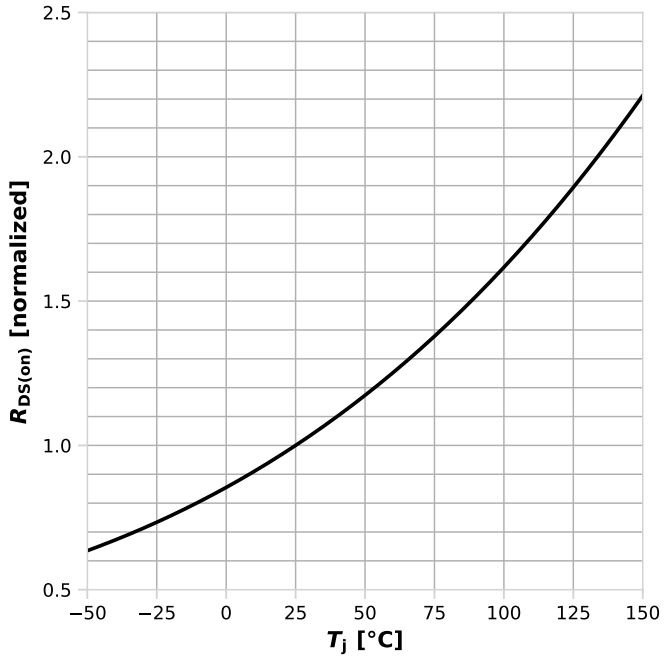
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D)$; T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}=f(T_j)$; I_D=8.3 A; V_{GS}=10 V

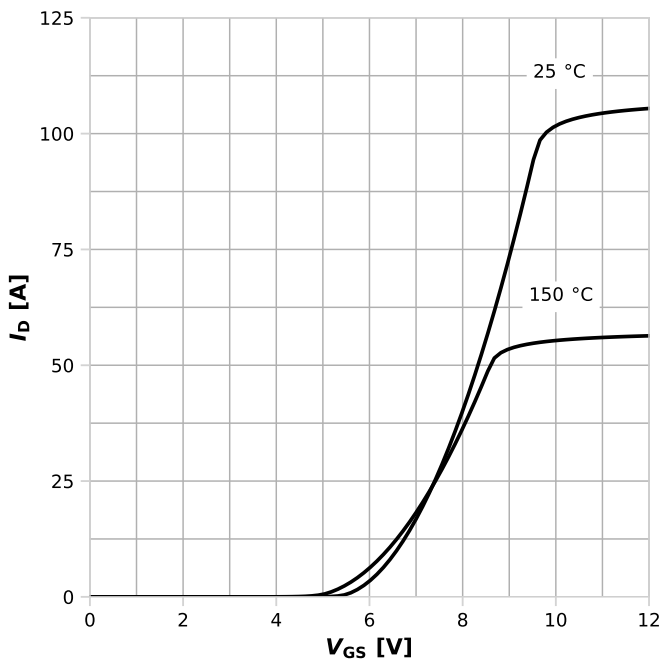
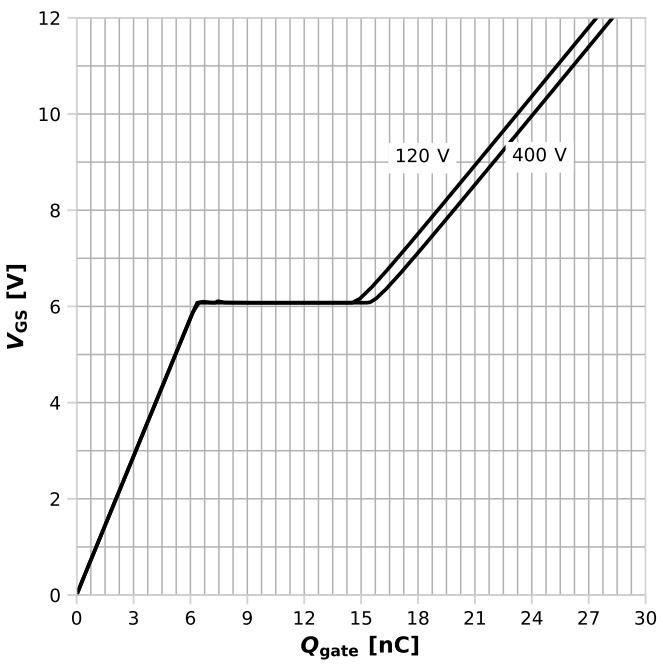
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=4.0 A pulsed; parameter: V_{DD}

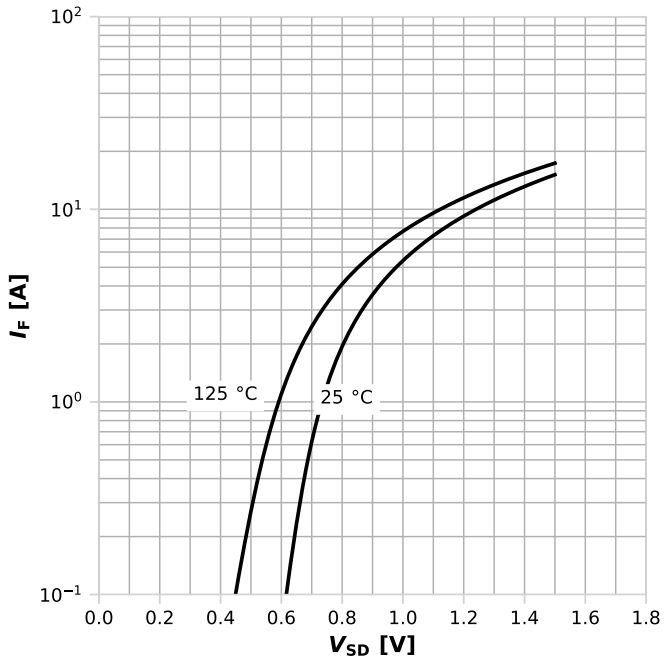
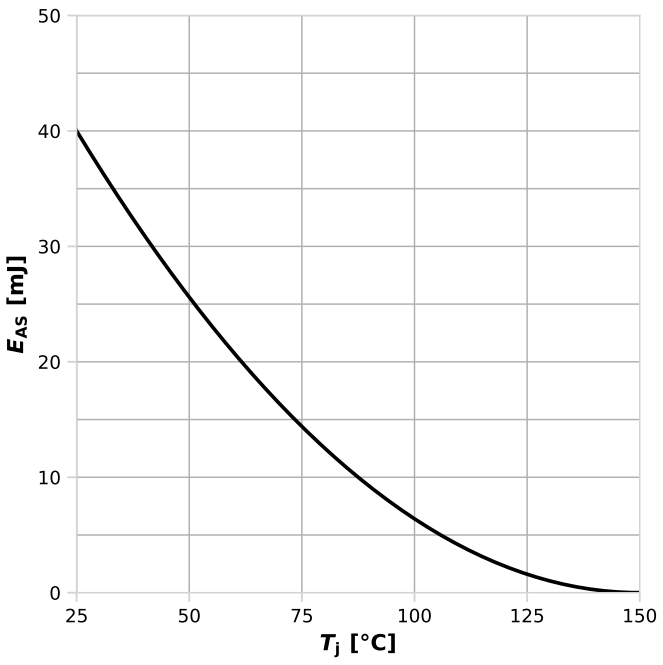
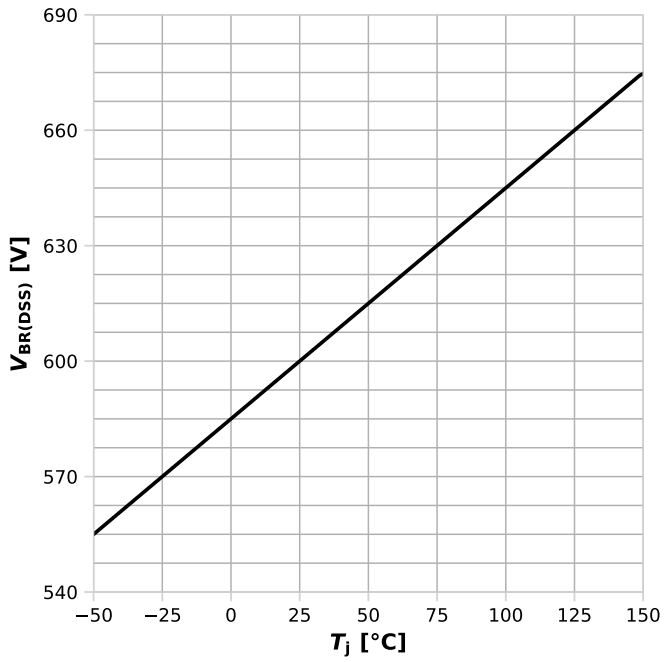
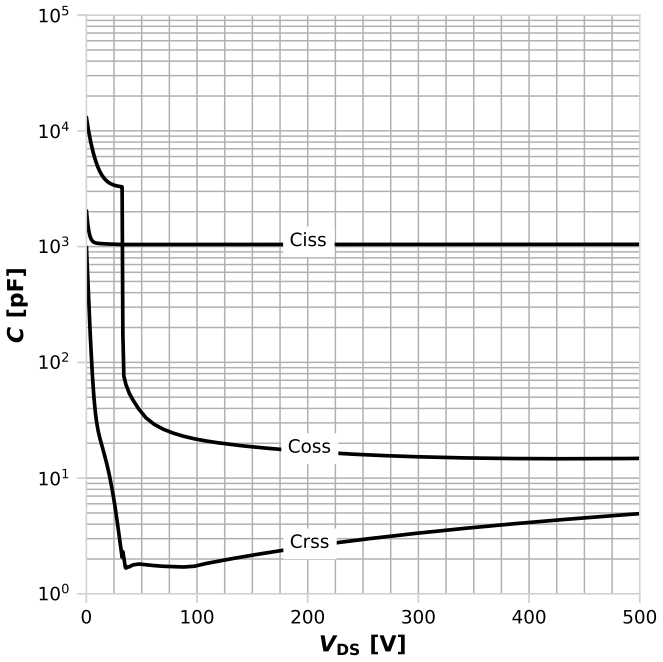
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=2.2 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



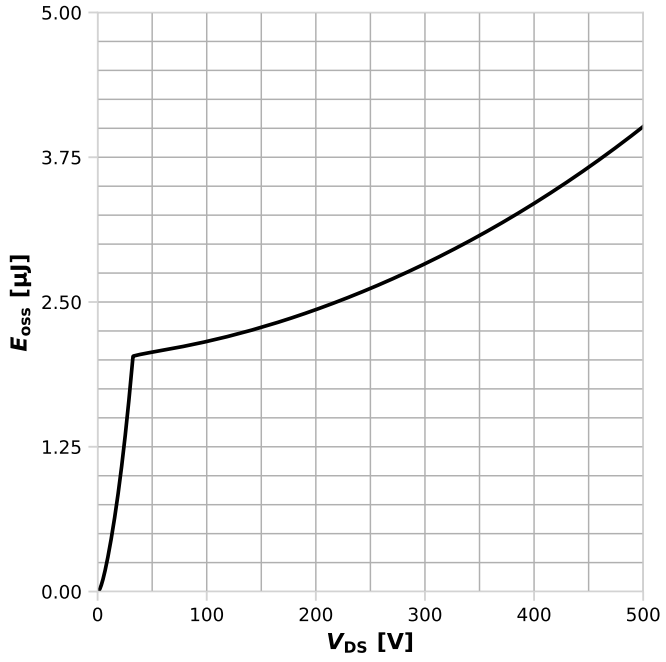
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test circuits

Table 8 Diode characteristics

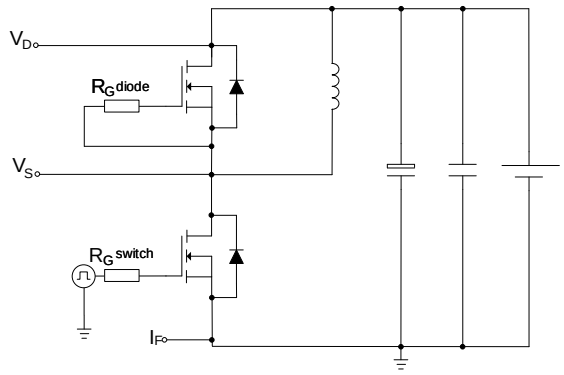
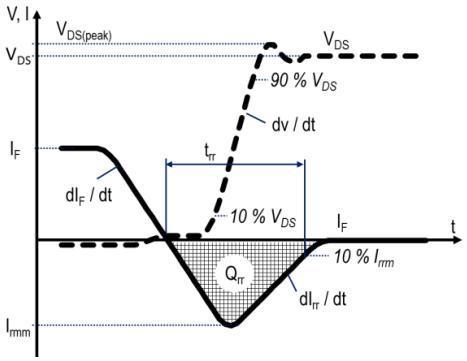
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

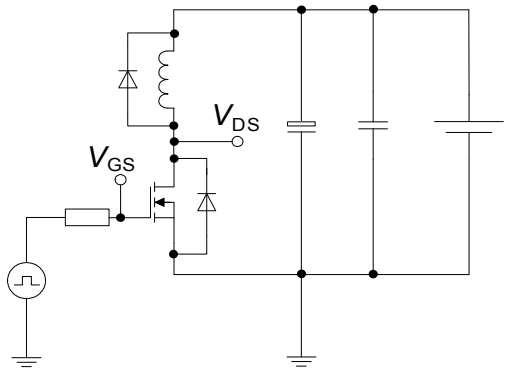
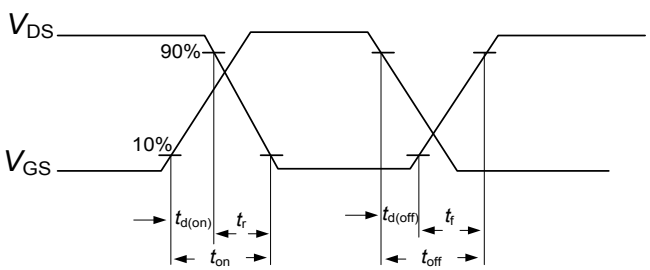
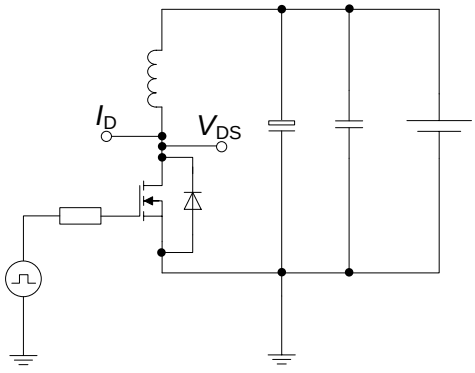
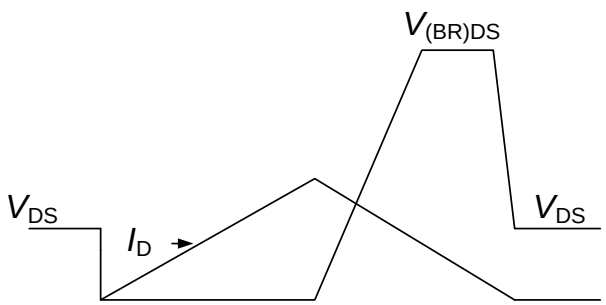
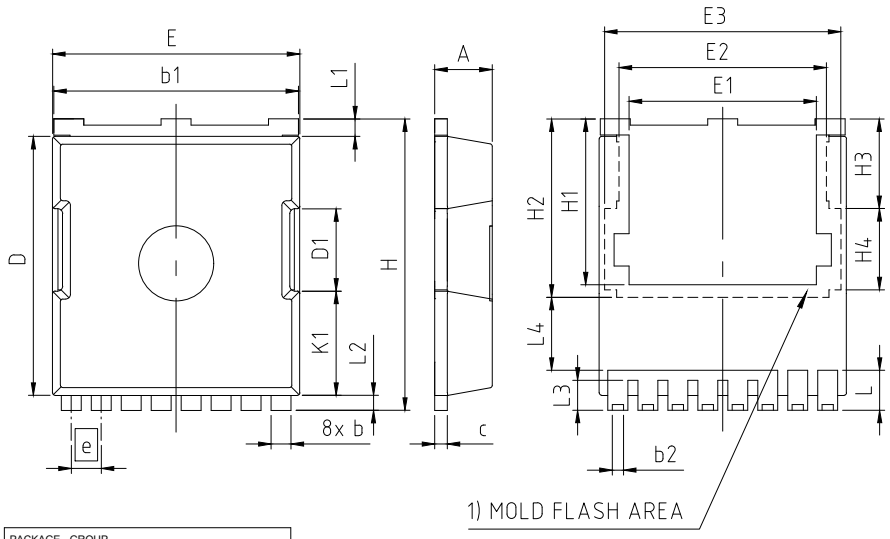
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package outlines



PACKAGE - GROUP NUMBER:	PG-HSOF-8-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	9.70	9.90
b2	0.42	0.50
c	0.40	0.60
D	10.28	10.58
D1	3.30	
E	9.70	10.10
E1	7.50	
E2	8.50	
E3	9.46	
e	1.20 (BSC)	
H	11.48	11.88
H1	6.55	6.95
H2	7.15	
H3	3.59	
H4	3.26	
N	8	
K1	4.18	
L	1.40	1.80
L1	0.50	0.90
L2	0.50	0.70
L3	1.00	1.30
L4	2.62	2.81

1) PARTIALLY COVERED WITH MOLD FLASH

Figure 1 Outline PG-HSOF-8, dimensions in mm

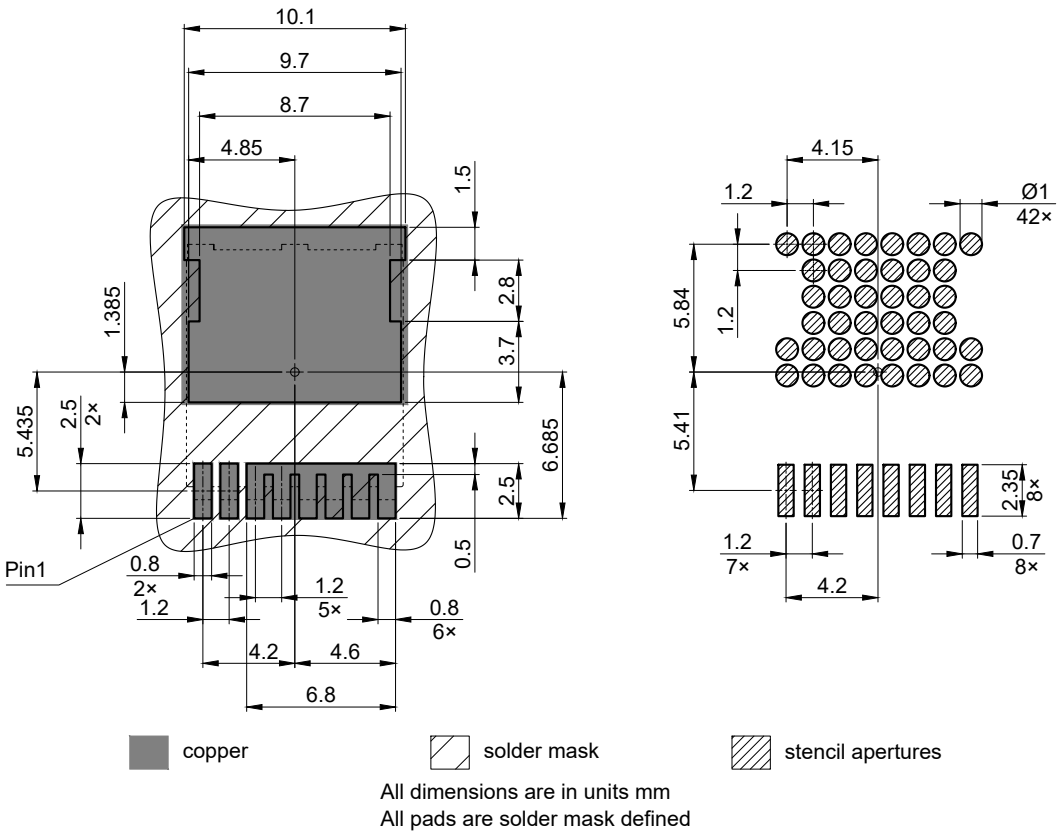


Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm

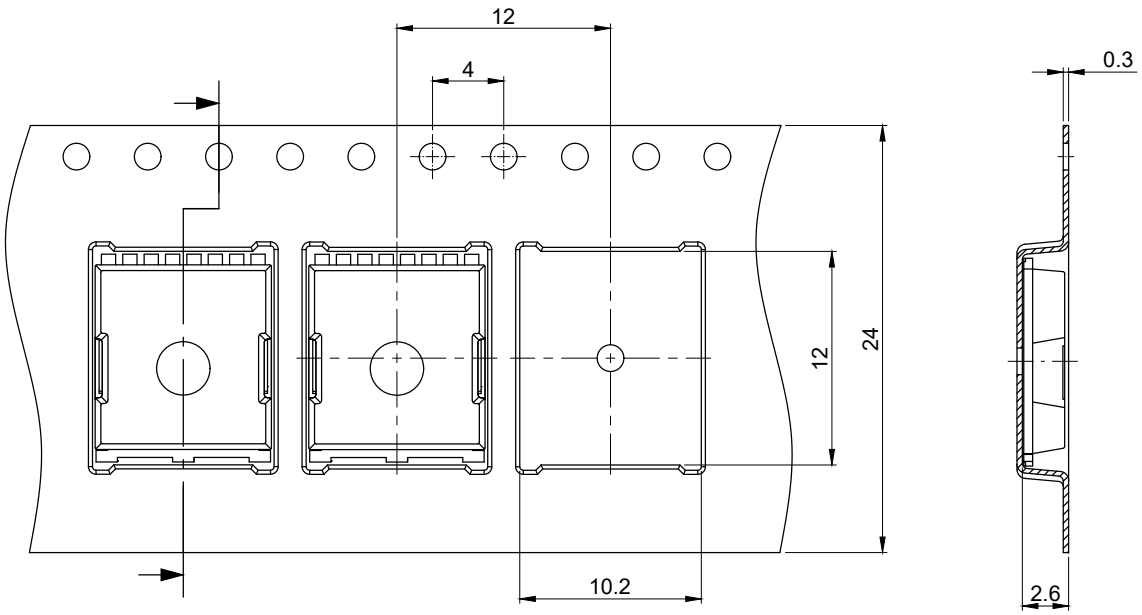


Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 11 Related links

- IFX CoolMOS CM8 Webpage
- IFX CoolMOS CM8 application note
- IFX CoolMOS CM8 simulation model
- IFX Design tools

Revision history

IPT60R120CM8

Revision 2024-12-19, Rev. 2.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2024-12-19	Release of final version

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