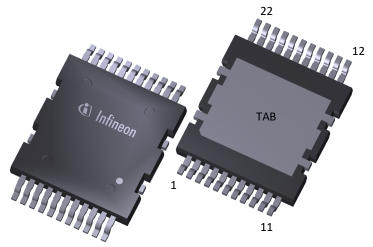
CoolMOS™ S7A

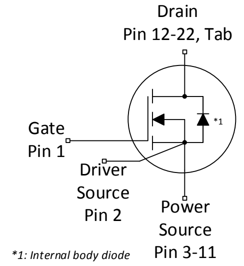
600V CoolMOS™ SJ S7A Power Device

IPQC60R010S7A is a high voltage power MOSFET, designed as static switch according to the superjunction (SJ) principle pioneered by Infineon Technologies.

IPQC60R010S7A combines the experience of the leading SJ MOSFET supplier with high class innovation enabling low $R_{DS(on)}$ in QDPAK package. The S7A series is optimised for low frequency switching and high current application like circuit breakers.

PG-HDSOP-22





Features

- Optimized for low switching frequency in high-end applications (circuit breakers and diode paralleling/replacement in bridge rectifiers).
- S7A technology enables best in class $R_{DS(on)}$ in smallest footprint.
- Kelvin Source pin improves switching performance at high current.
- QDPAK (PG-HDSOP-22-1) package is MSL1 compliant, total Pb-free, has easy visual inspection leads.

Benefits

- S7A enabling low $R_{DS(on)}$ for high constant current.
- Increased performance by using MOSFET instead of diode in the application (e.g. synchronous rectification).
- S7A can reach 10mΩ in QDPAK 315mm^2 footprint.
- Reduced parasitic source inductance by Kelvin Source improves stability for extreme high current handling and ease of use due to less ringing.
- Improved thermals enable SMD QDPAK package to be used in high current designs.

Potential applications

Circuit breakers (HV Battery disconnect switch, DC and AC low frequency switch, HV E-fuse) and diode paralleling/replacement for high power /performance applications.

Product validation

Qualified according to AEC Q101

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate. For production part approval process (PPAP) release we propose to share application related information during an early design phase to avoid delays in PPAP release. Please contact Infineon sales office.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$R_{DS(on),max}$	10	mΩ
$Q_{g,typ}$	318	nC
V_{SD}	0.82	V
Pulsed I_{SD}, I_{DS}	801	A

Type/Ordering Code	Package	Marking	Related Links
IPQC60R010S7A	PG-HDSOP-22	60A010S7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain current rating	I_D	-	-	50	A	T_C=140°C Current is limited by $T_{j\,max}$ = 150°C; Lower case temp does increase current capability
Pulsed drain current [1]	$I_{D,pulse}$	-	-	801	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	616	mJ	I_D=6.3A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	6.3	A	-
MOSFET dv/dt ruggedness [2]	dv/dt	-	-	20	V/ns	V_{DS}= 0V to 300V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	694	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-40	-	150	°C	-
Extended operating junction temperature	T_j	150	-	175	°C	≤50 h in the application lifetime
Mounting torque	-	-	-	n.a.	Ncm	-
Diode forward current rating	I_S	-	-	50	A	T_C=140°C Current is limited by $T_{j\,max}$ = 150°C; Lower case temp does increase current capability
Diode pulse current [1]	$I_{S,pulse}$	-	-	801	A	T_C=25°C
Reverse diode dv/dt [3]	dv/dt	-	-	5	V/ns	V_{DS}=0 to 300V, I_{SD}≤50A, T_j=25°C see table 8
Maximum diode commutation speed	di_f/dt	-	-	1000	A/µs	V_{DS}=0 to 300V, I_{SD}≤50A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

1) Pulse width t_p limited by $T_{j,max}$
2) The dv/dt has to be limited by appropriate gate resistor
3) Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.18	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	45	55	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µ""m thickness) copper area. Tap exposed to air. PCB is vertical without air stream cooling.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

The CoolMOS™ mentioned in this datasheet shall not be operated in linear mode.
For any questions in this regard, please contact Infineon sales office.
For applications with applied blocking voltage >70% of the specified blocking voltage, it is required that the customer
evaluates the impact of cosmic radiation effect in early design phase and contacts the Infineon sales office for the necessary technical support by Infineon

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4.0	4.5	V	V_{DS}=V_{GS}, I_D=3.08mA
Zero gate voltage drain current	I_{DSS}	-	- 80	8 -	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.009 0.022	0.010 -	Ω	V_{GS}=12V, I_D=50A, T_j=25°C V_{GS}=12V, I_D=50A, T_j=150°C
Gate resistance	R_G	-	0.45	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	11986	-	pF	V_{GS}=0V, V_{DS}=300V, f=250kHz
Output capacitance	C_{oss}	-	188	-	pF	V_{GS}=0V, V_{DS}=300V, f=250kHz
Effective output capacitance, energy related [4]	$C_{o(er)}$	-	644	-	pF	V_{GS}=0V, V_{DS}=0 to 300V
Effective output capacitance, time related [5]	$C_{o(tr)}$	-	5717	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0 to 300V
Output charge	Q_{oss}	-	1714	-	nC	V_{GS}=0V, V_{DS}=0 to 300V
Turn-on delay time	$t_{d(on)}$	-	50	-	ns	V_{DD}=300V, V_{GS}=13V, I_D=50A, R_G=3Ω; see table 9
Rise time	t_r	-	5	-	ns	V_{DD}=300V, V_{GS}=13V, I_D=50A, R_G=3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	180	-	ns	V_{DD}=300V, V_{GS}=13V, I_D=50A, R_G=3Ω; see table 9
Fall time	t_f	-	9	-	ns	V_{DD}=300V, V_{GS}=13V, I_D=50A, R_G=3Ω; see table 9

4) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 300V

5) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 300V

Table 6 Gate charge characteristics

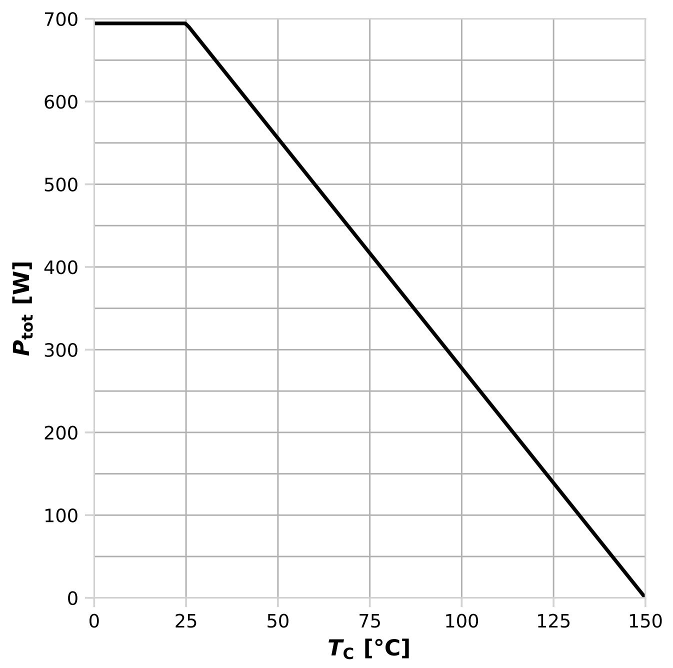
Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	69	-	nC	V_{DD}=300V, I_D=50A, V_{GS}=0 to 12V
Gate to drain charge	Q_{gd}	-	105	-	nC	V_{DD}=300V, I_D=50A, V_{GS}=0 to 12V
Gate charge total	Q_g	-	318	-	nC	V_{DD}=300V, I_D=50A, V_{GS}=0 to 12V
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	V_{DD}=300V, I_D=50A, V_{GS}=0 to 12V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.82	-	V	V_{GS}=0V, I_F=50A, T_j=25°C
Reverse recovery time	t_{rr}	-	600	-	ns	V_R=300V, I_F=50A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	17	-	µC	V_R=300V, I_F=50A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	55	-	A	V_R=300V, I_F=50A, di_F/dt=100A/µs; see table 8

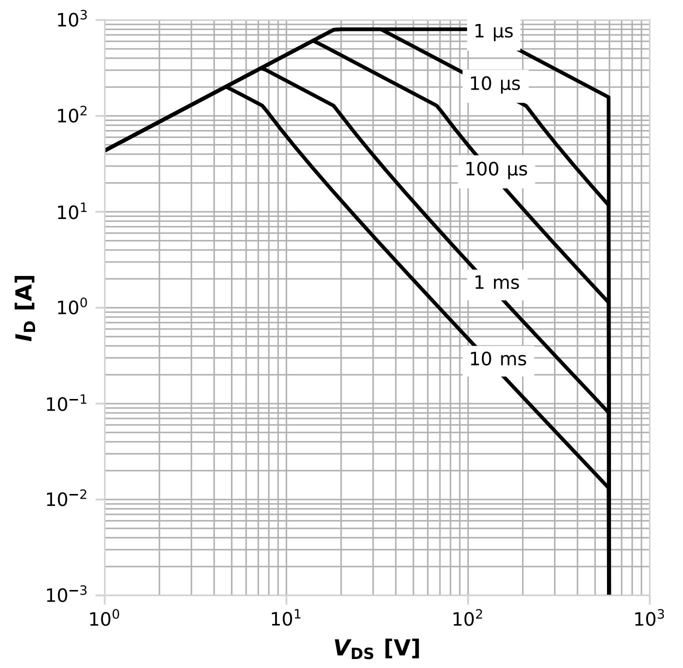
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



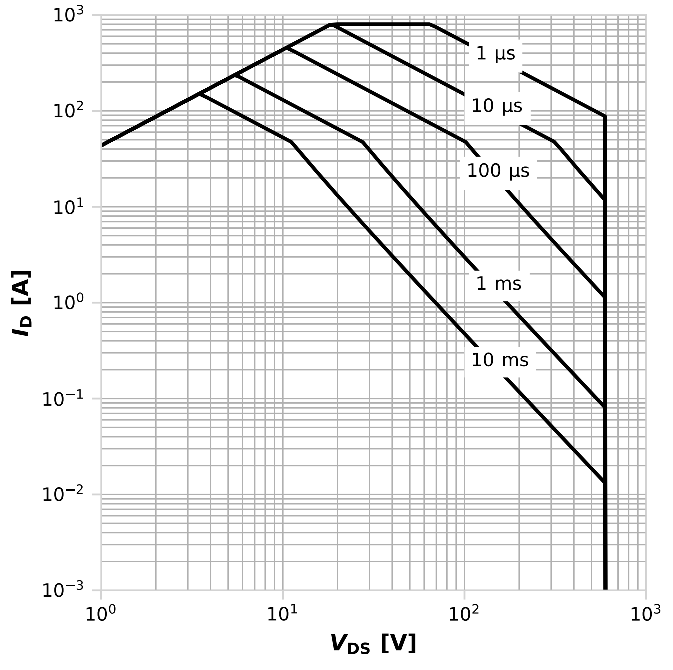
P_{tot}=f(T_C)

Diagram 2: Safe operating area



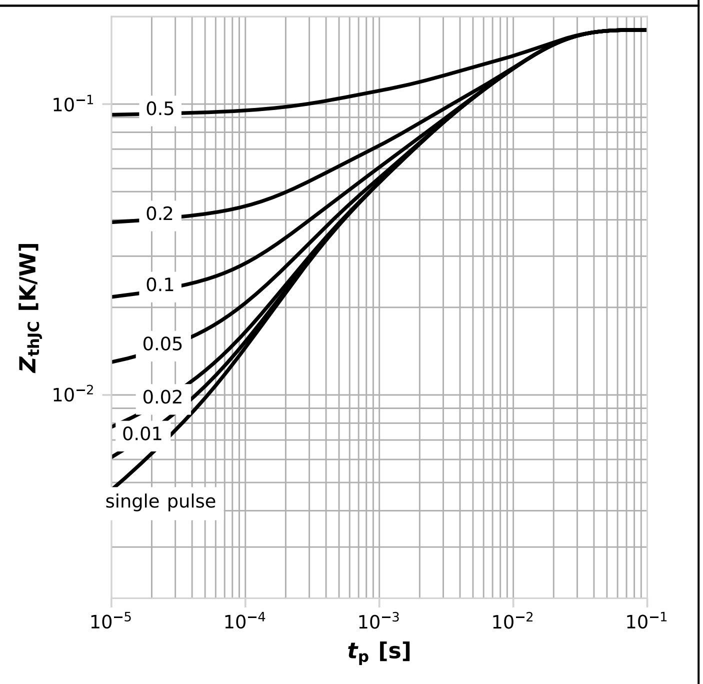
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



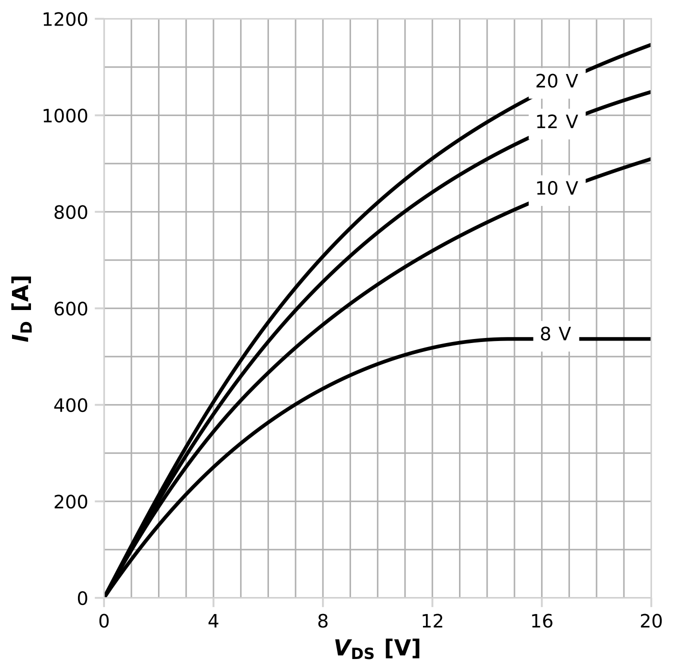
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



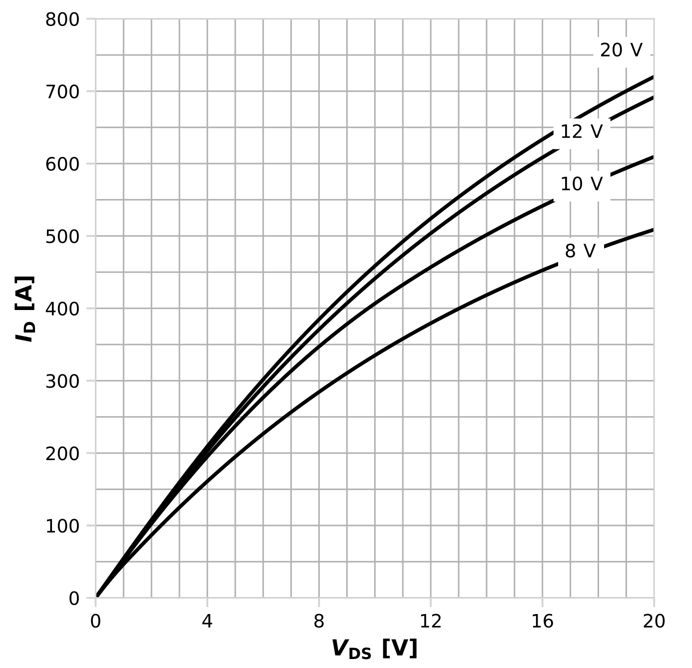
Z_{thJC} =f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



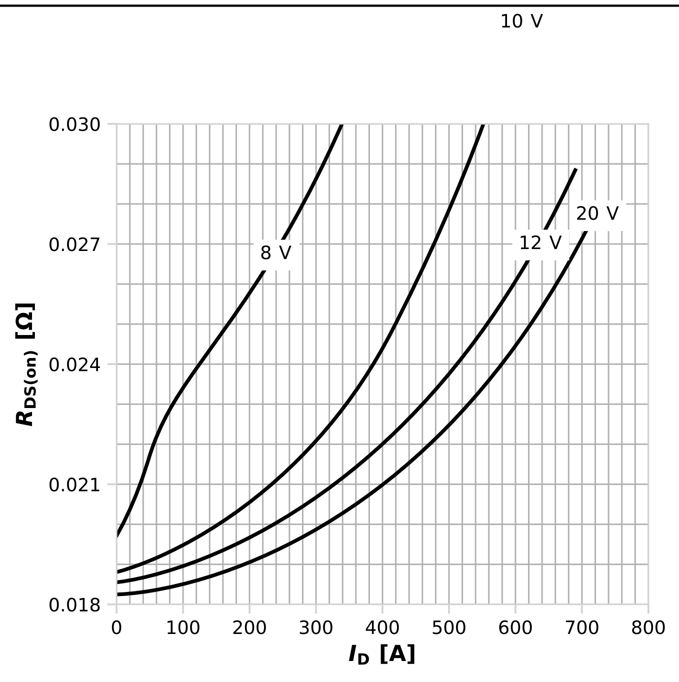
$I_D=f(V_{DS})$; T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



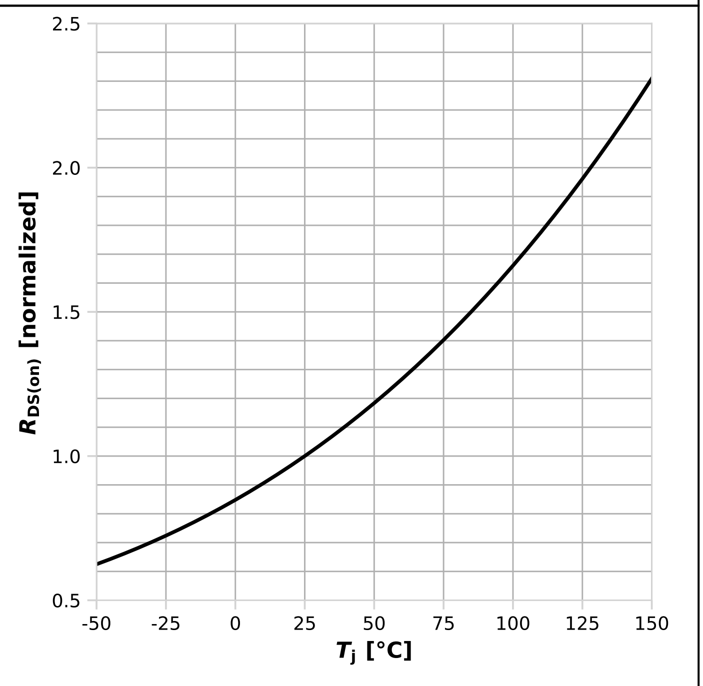
$I_D=f(V_{DS})$; T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D)$; T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}=f(T_j)$; I_D=50 A; V_{GS}=12 V

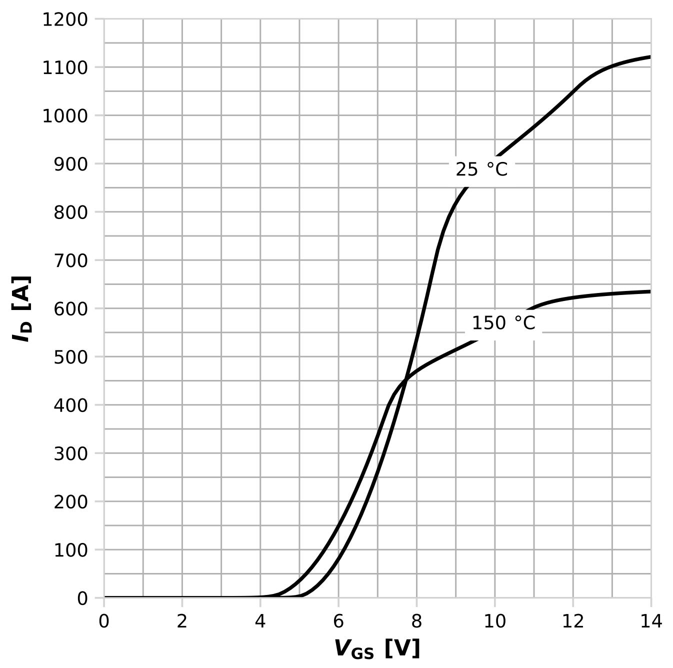
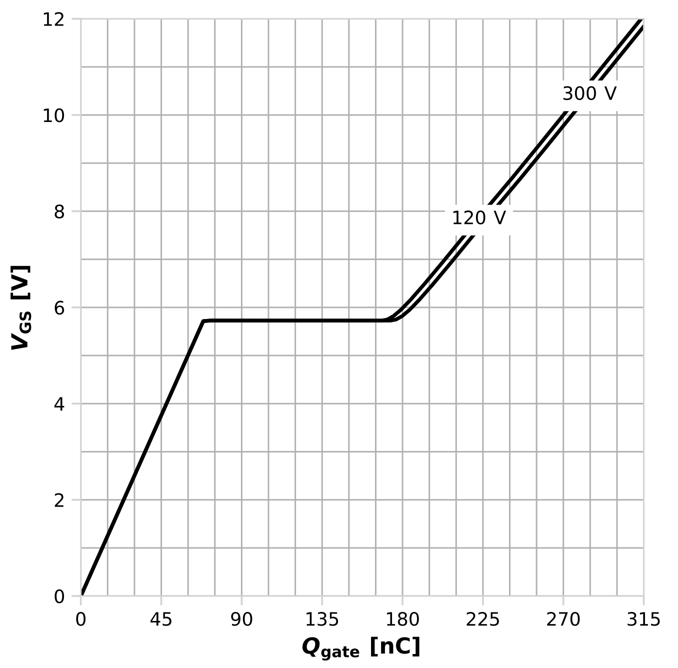
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j	$V_{GS}=f(Q_{gate})$; I_D=50 A pulsed; parameter: V_{DD}

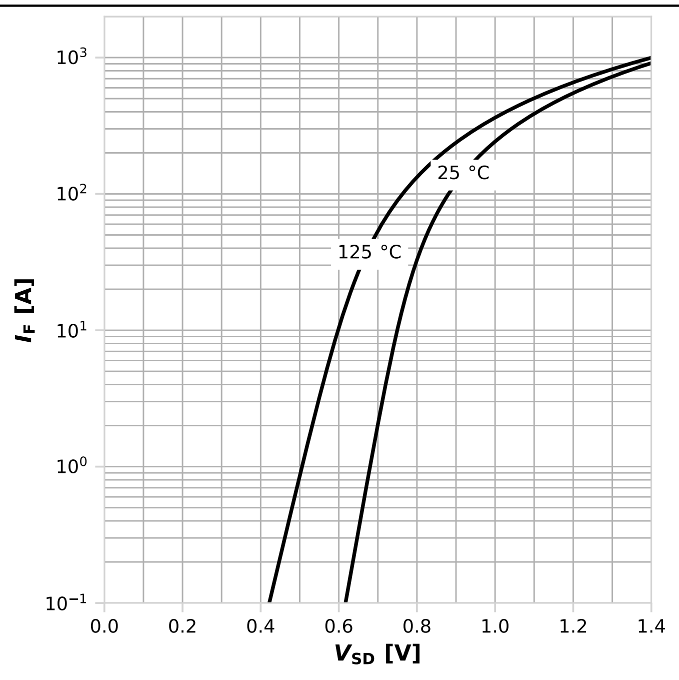
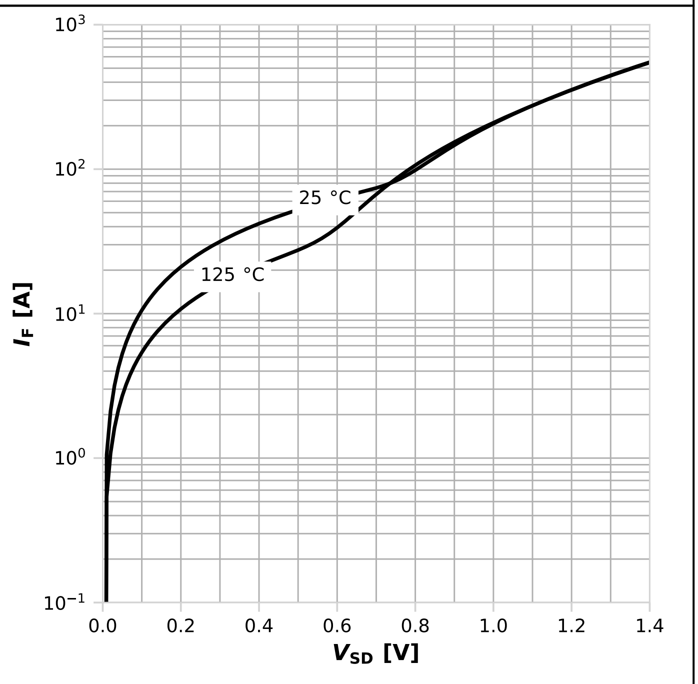
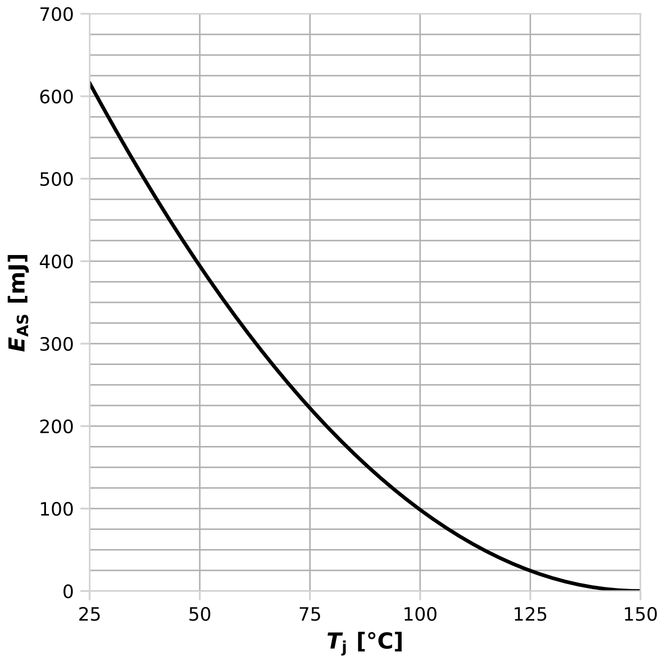
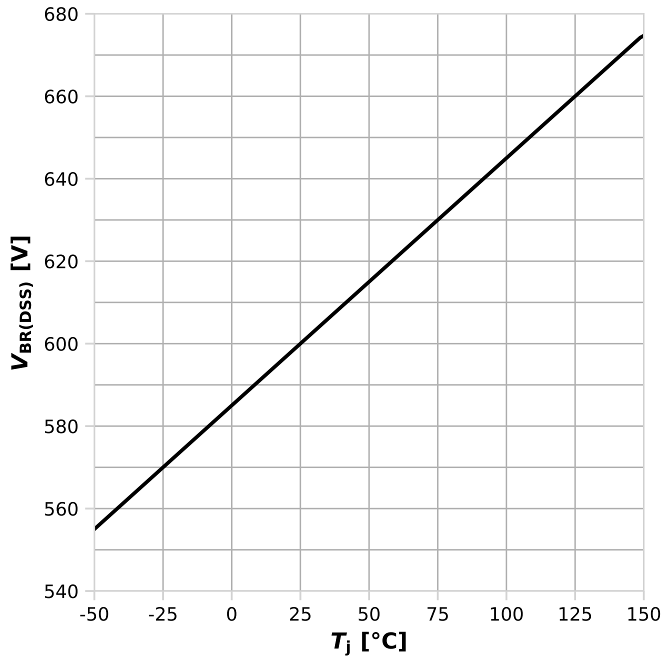
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Forward characteristics of reverse diode
	
$I_F=f(V_{SD})$; V_{GS}=0 V; parameter: T_j	$I_F=f(V_{SD})$; V_{GS}=12 V; parameter: T_j

Diagram 13: Avalanche energy



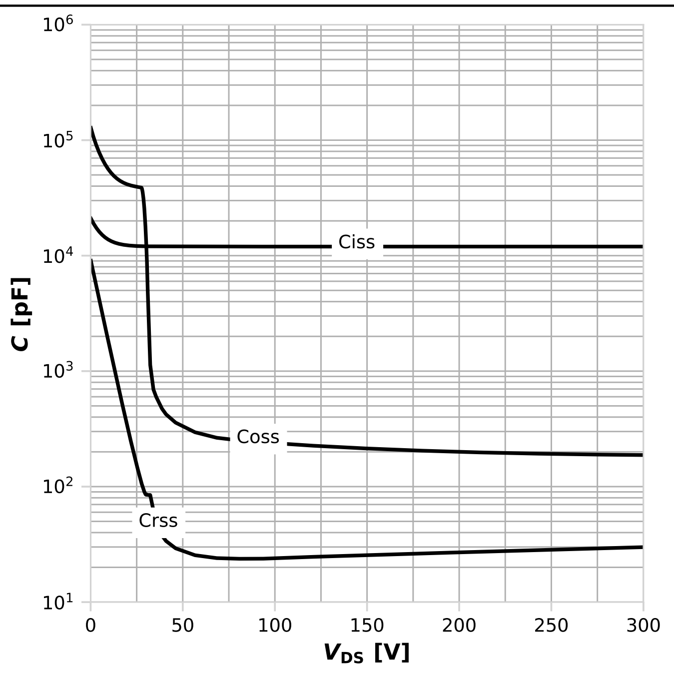
E_{AS}=f(T_j); I_D=6.3 A; V_{DD}=50 V

Diagram 14: Drain-source breakdown voltage



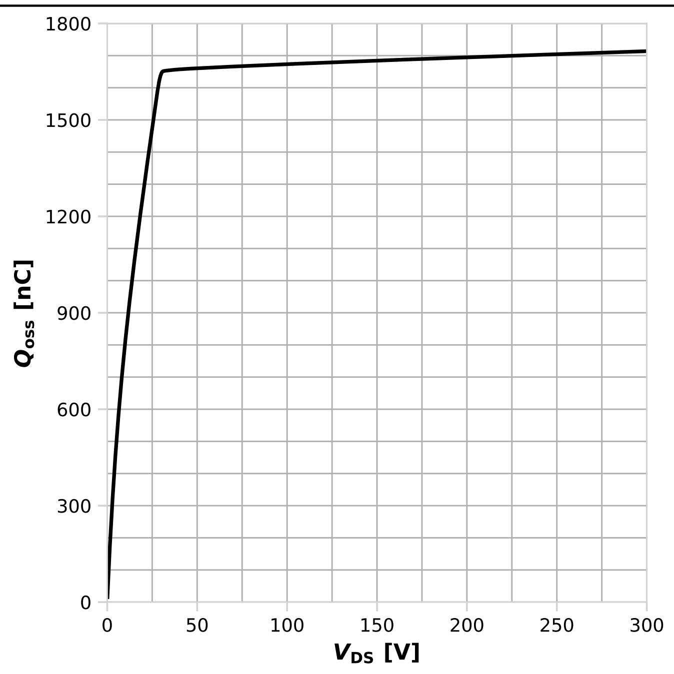
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 15: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 17: Typ. Qoss output charge



Q_{oss}=f(V_{DS}); V_{GS}=0 V

5 Test Circuits

Table 8 Diode characteristics

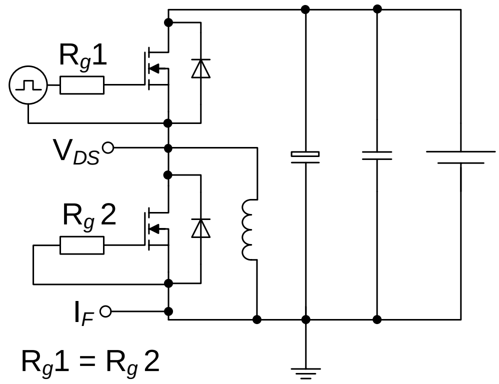
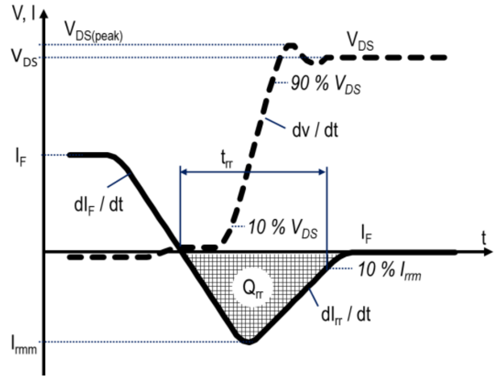
<table>
<tr><th>Test circuit for diode characteristics</th><th>Diode recovery waveform</th></tr>
<tr><td>
</td><td>
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Table 9 Switching times (ss)

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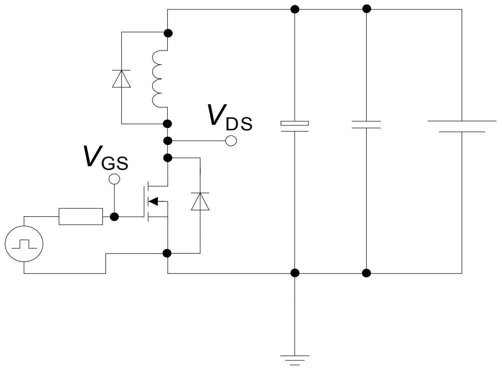
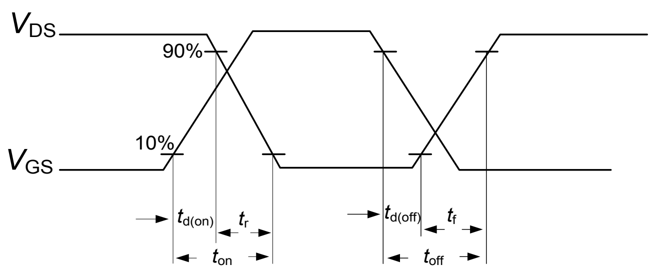
<tr><th>Switching times test circuit for inductive load</th><th>Switching times waveform</th></tr>
<tr><td>
</td><td>
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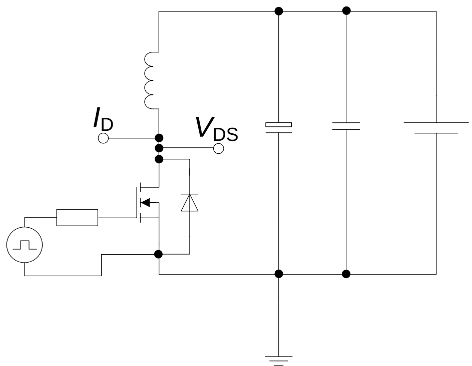
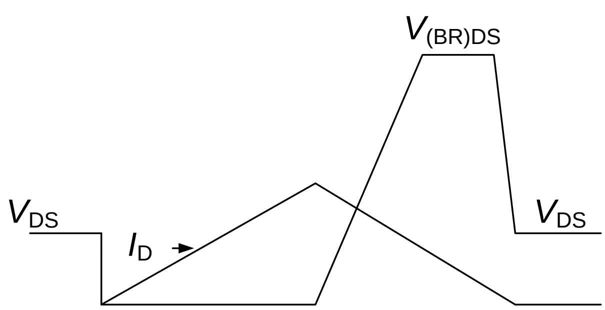
Table 10 Unclamped inductive load (ss)

<table>
<tr><th>Unclamped inductive load test circuit</th><th>Unclamped inductive waveform</th></tr>
<tr><td>
</td><td>
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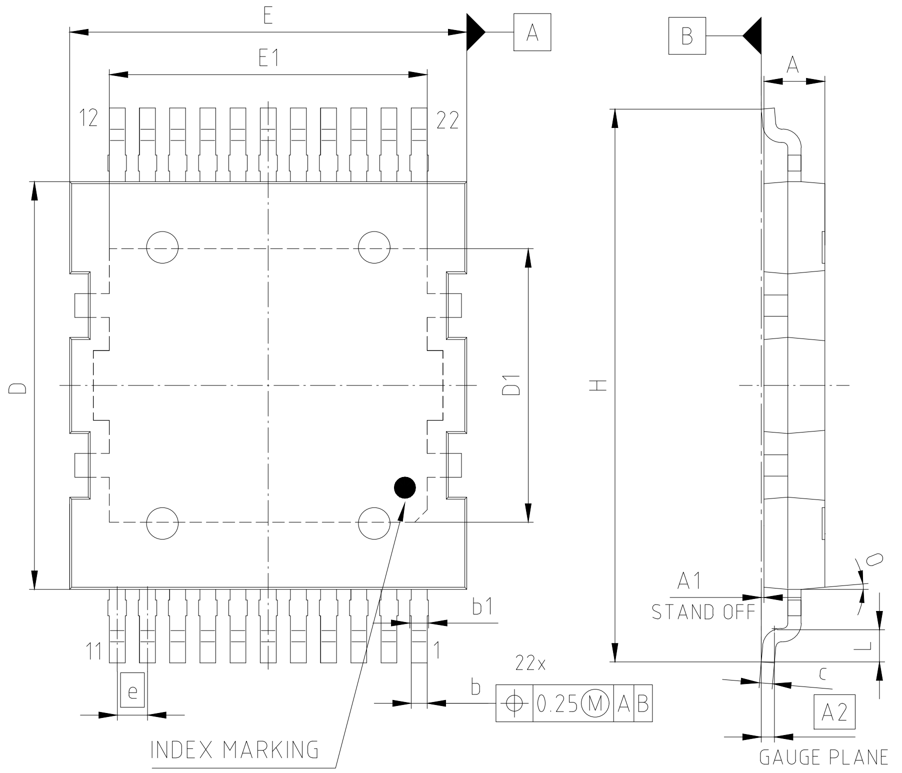
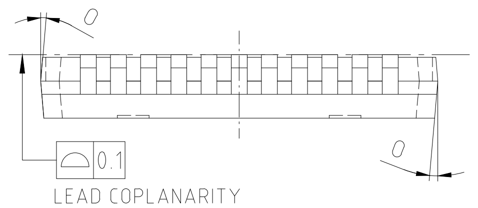
6 Package Outlines





PACKAGE - GROUP NUMBER:	PG-HDSOP-22-U02	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.5	
b	0.50	0.70
b1	0.50	0.90
c	0.46	0.58
D	15.30	15.50
D1	10.23	10.43
E	14.90	15.10
E1	11.91	12.11
e	1.14	
N	22	
H	20.81	21.11
L	1.20	1.40
O	5°	

Figure 1 Outline PG-HDSOP-22, dimensions in mm

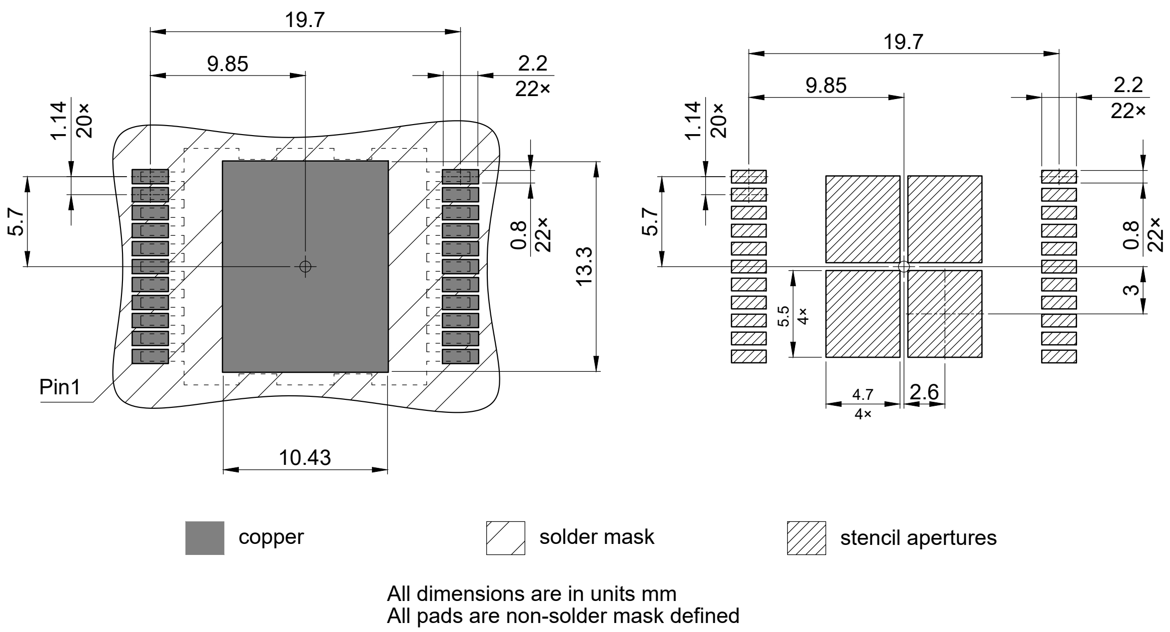
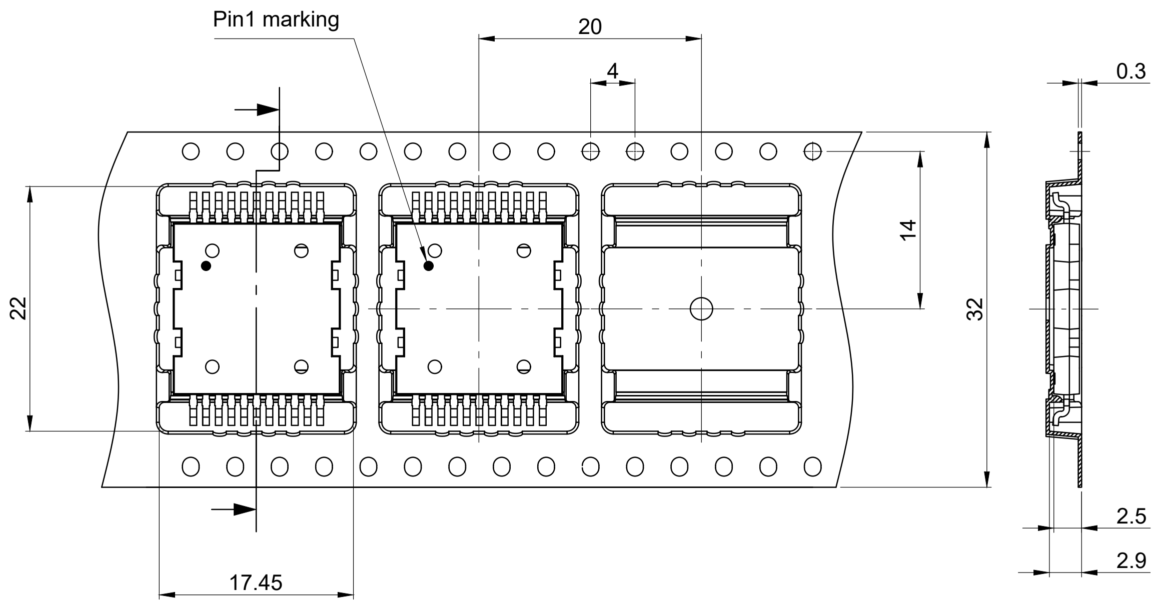


Figure 2 Outline PG-HDSOP-22, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 3 Outline PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS S7 Webpage
- IFX CoolMOS S7 application note
- IFX CoolMOS S7 simulation model
- IFX Design tools

Revision History

IPQC60R010S7A

Revision 2024-05-24, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-11-23	Release of final version
2.1	2023-10-30	Added footnote for pulsed drain current
2.2	2023-11-22	Additional maximum parameter for high current turn off added to datasheet for SSCB, SSR and motor start applications; Removed footmark from pulsed drain current
2.3	2024-05-24	Removed high current turn-off parameter limitation, Adaption of Transfer curve, Output characteristics and drain-source on-state resistance

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