OptiMOS®-T2 Power-Transistor

Product Summary

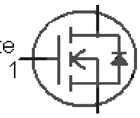
V_{DS}	40	V
$R_{DS(on),max}$ (SMD version)	2.1	mΩ
I_D	90	A

PG-TO263-3-2	PG-TO262-3-1	PG-TO220-3-1
		

Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Type	Package	Marking
IPB90N04S4-02	PG-TO263-3-2	4N0402
IPI90N04S4-02	PG-TO262-3-1	4N0402
IPP90N04S4-02	PG-TO220-3-1	4N0402



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1)]	I_D	T_C=25 °C, V_{GS}=10 V	90	A
		T_C=100°C, V_{GS}=10V[2)]	90	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25°C	360	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=45A	475	mJ
Avalanche current, single pulse	I_{AS}	-	90	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25°C	150	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[2]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	1.0	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[3]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=95µA	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	0.04	1	µA
		V_{DS}=18V, V_{GS}=0V, T_j=85°C[2]	-	1	20	
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=90A	-	2.3	2.5	mΩ
		V_{GS}=10V, I_D=90A, SMD version	-	1.9	2.1	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	7250	9430	pF
Output capacitance	C_{oss}		-	1630	2120	
Reverse transfer capacitance	C_{rss}		-	55	127	
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, V_{GS}=10V, I_D=90A, R_G=3.5Ω	-	23	-	ns
Rise time	t_r		-	13	-	
Turn-off delay time	$t_{d(off)}$		-	27	-	
Fall time	t_f		-	26	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=32V, I_D=90A, V_{GS}=0 to 10V	-	39	51	nC
Gate to drain charge	Q_{gd}		-	12	28	
Gate charge total	Q_g		-	91	118	
Gate plateau voltage	$V_{plateau}$		-	5.8	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25°C	-	-	90	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=90A, T_j=25°C	-	0.9	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=20V, I_F=50A, di_F/dt=100A/µs	-	53	-	ns
Reverse recovery charge[2]	Q_{rr}		-	65	-	nC

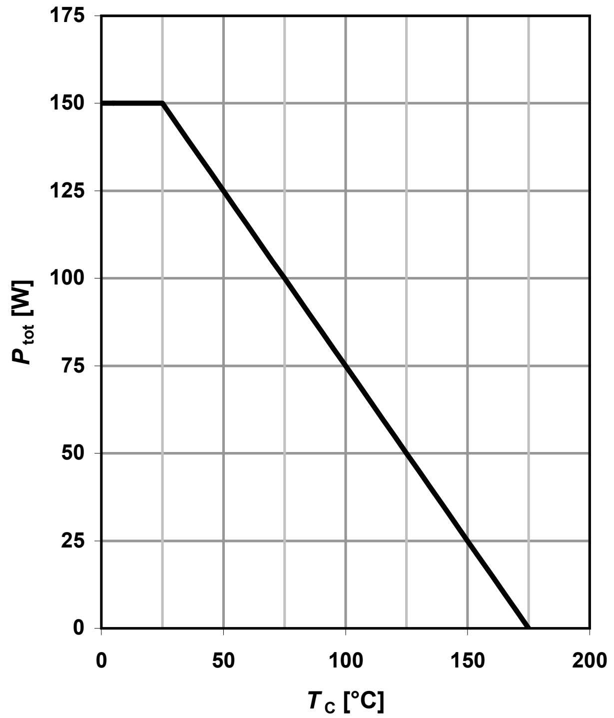
[1] Current is limited by bondwire; with an R_{thJC} = 1K/W the chip is able to carry 200A at 25°C.

[2] Defined by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

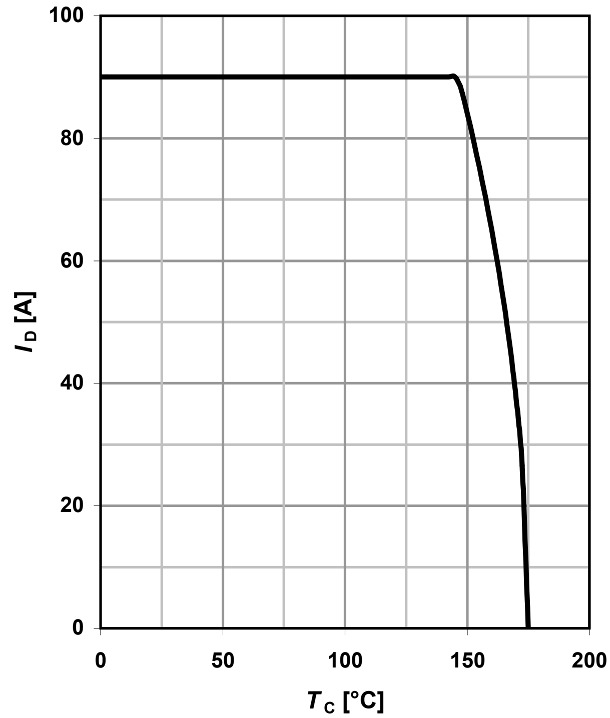
1 Power dissipation

P_{tot} = f(T_C); $V_{GS} \geq 6$ V



2 Drain current

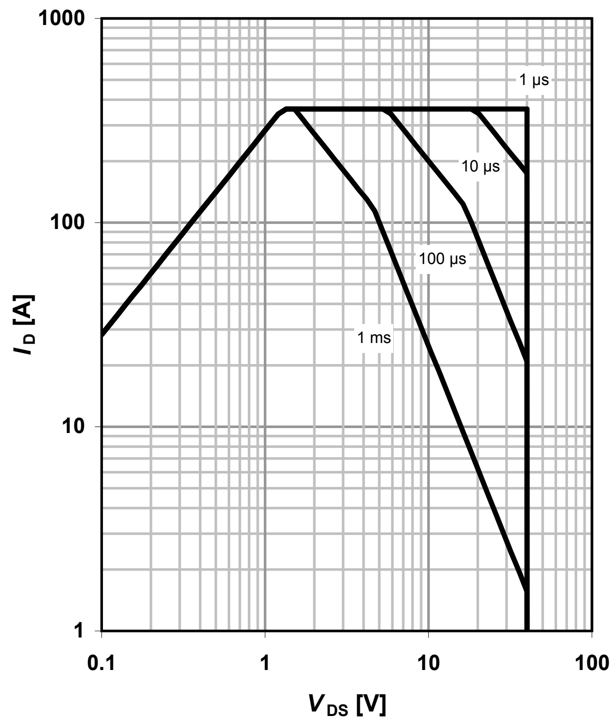
I_D = f(T_C); $V_{GS} \geq 6$ V; SMD



3 Safe operating area

I_D = f(V_{DS}); T_C = 25 °C; D = 0; SMD

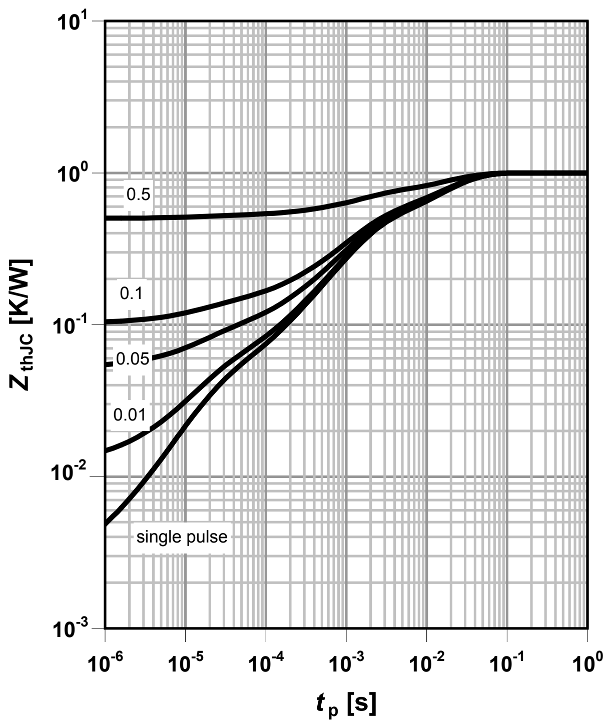
parameter: t_p



4 Max. transient thermal impedance

Z_{thJC} = f(t_p)

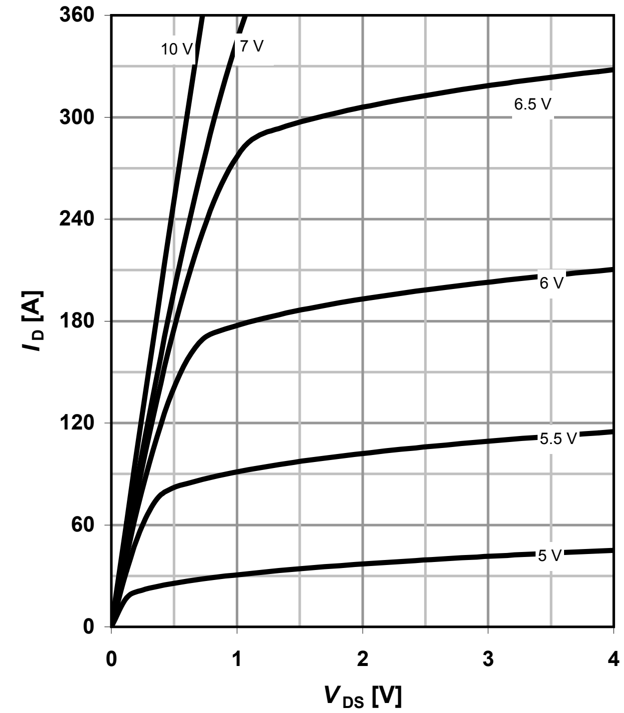
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; SMD

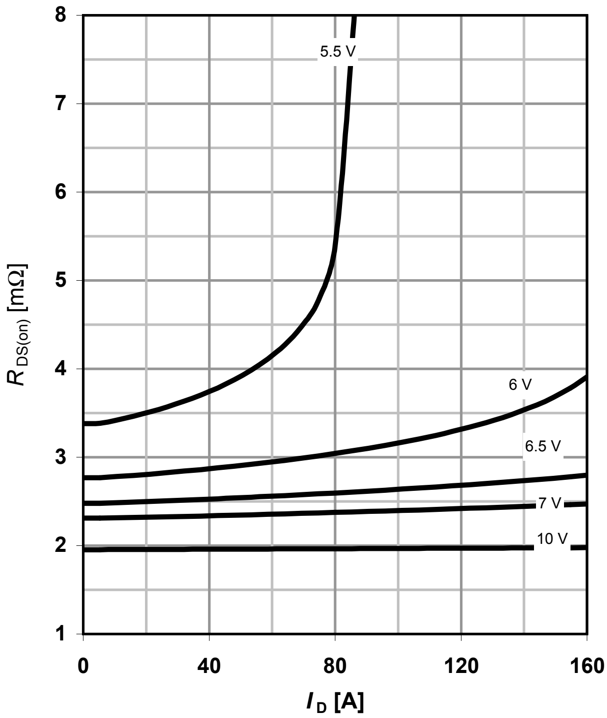
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; SMD

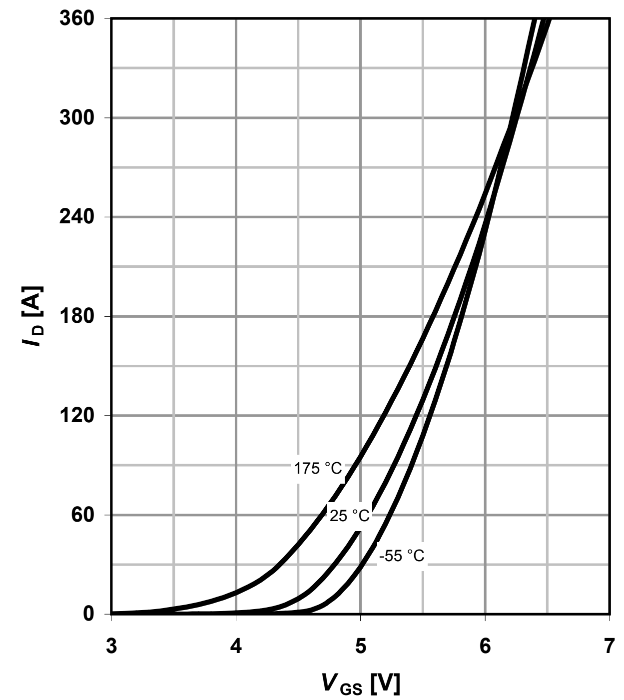
parameter: V_{GS}



7 Typ. transfer characteristics

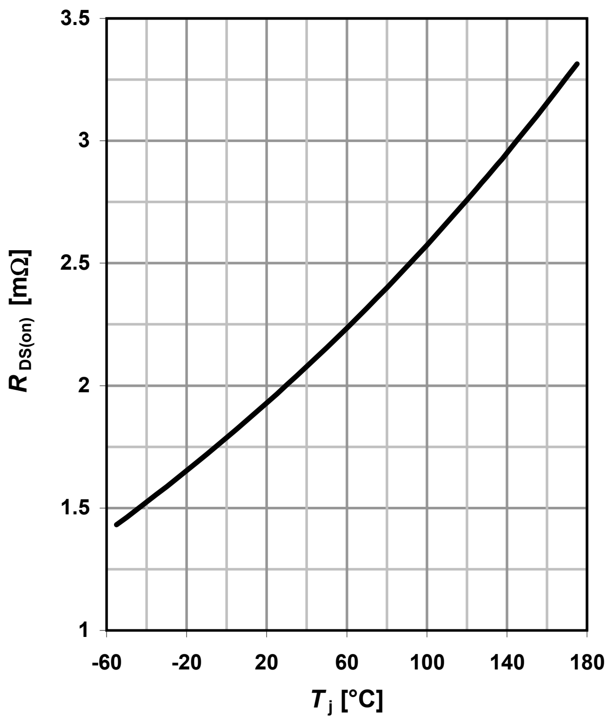
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

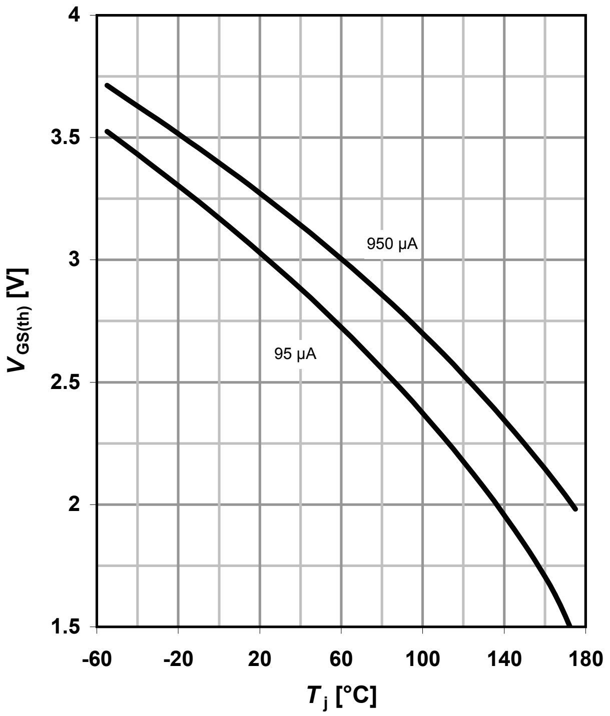
$R_{DS(on)} = f(T_j)$; $I_D = 90$ A; $V_{GS} = 10$ V; SMD



9 Typ. gate threshold voltage

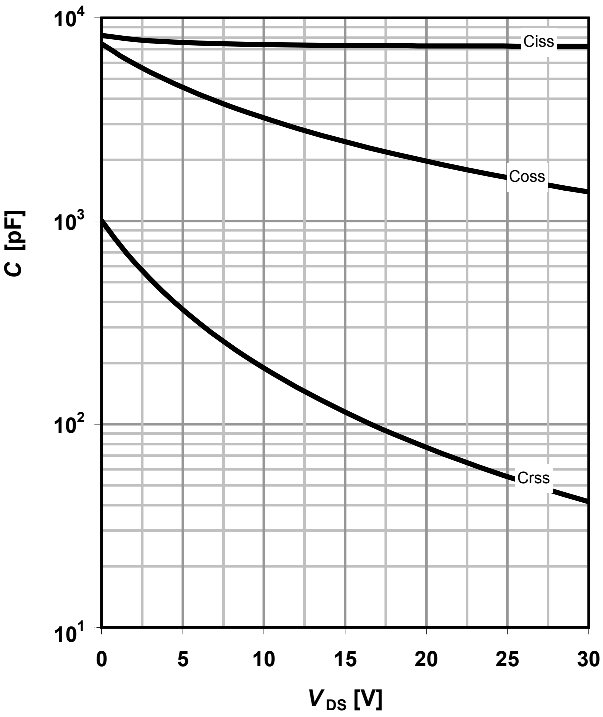
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

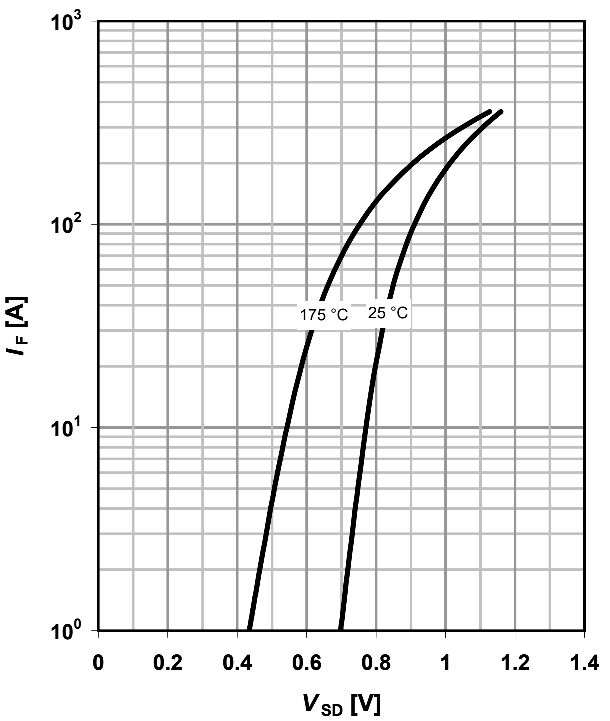
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = $f(V_{SD})$

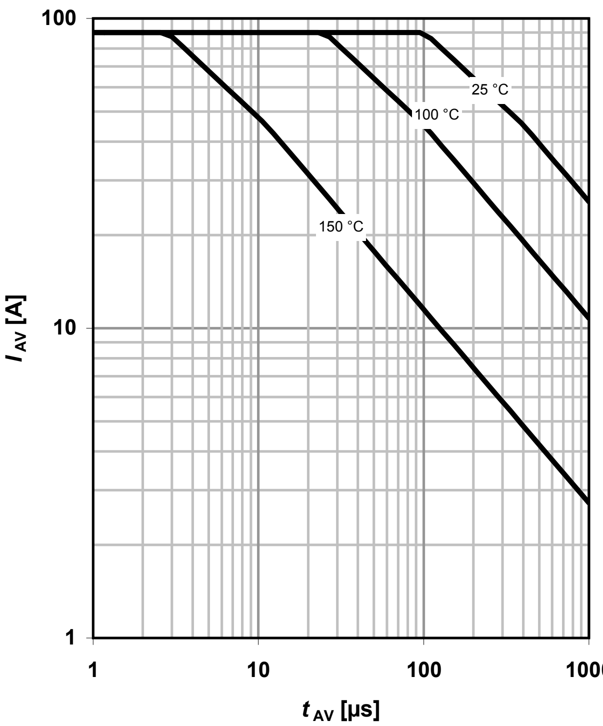
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

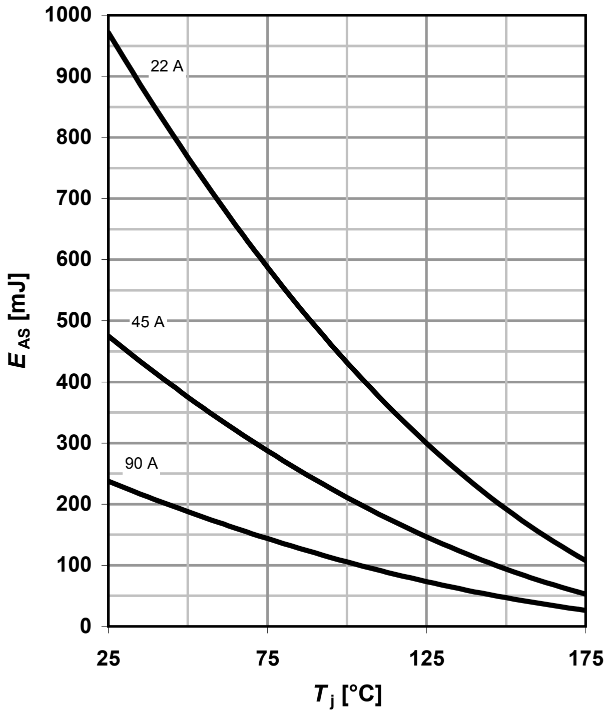
parameter: $T_{j(start)}$



13 Avalanche energy

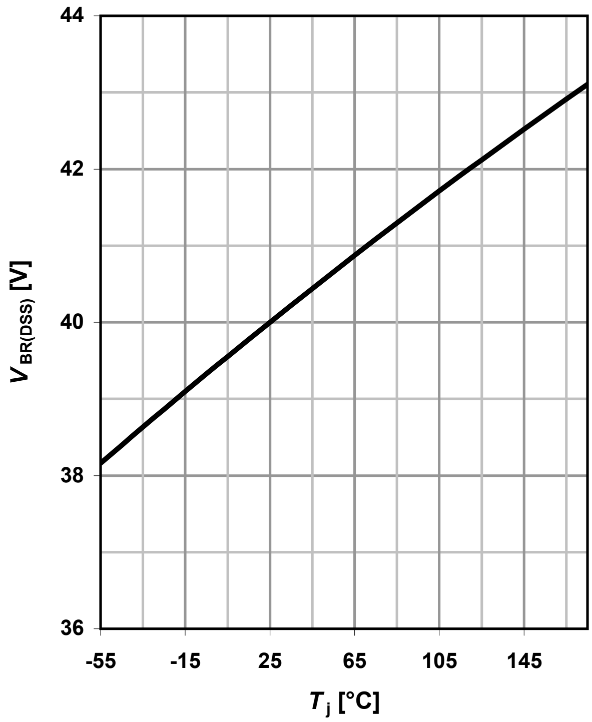
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

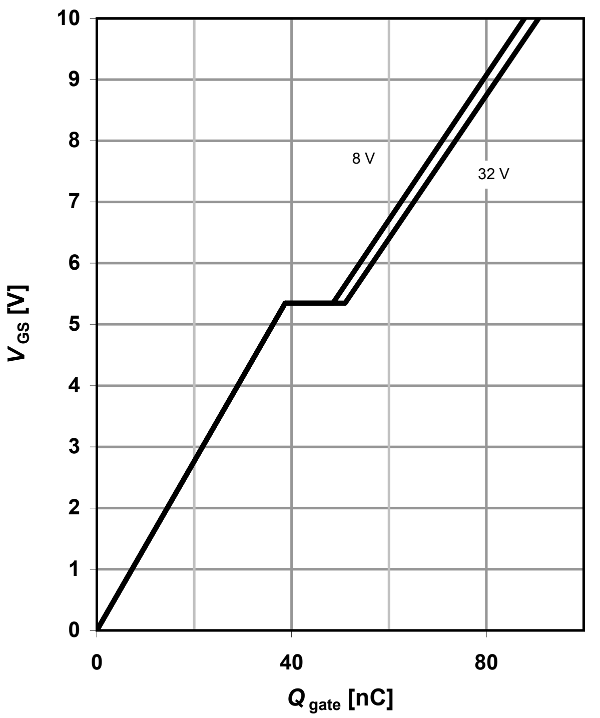
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



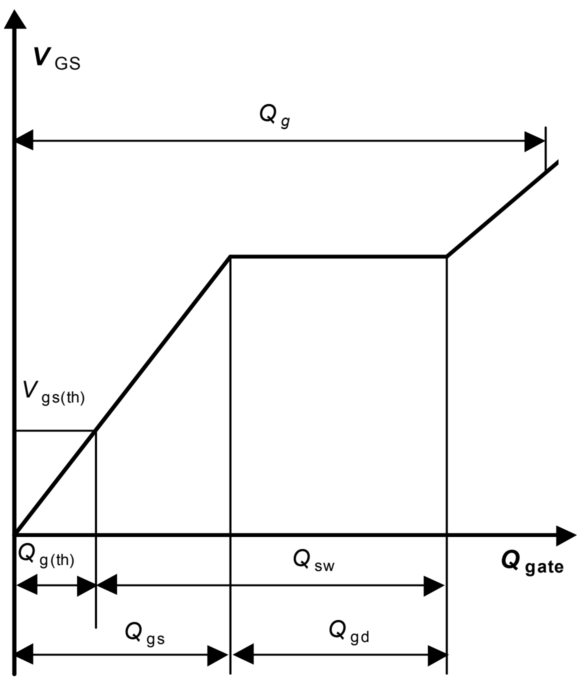
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 90$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	17.05.2010	Final Data Sheet
Revision 1.1	01.07.2010	Update of diagram 5, 6, 8