MOSFET

StrongIRFET™ 2 Power-Transistor

Features
- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation
Qualified according to JEDEC Standard

Table 1  Key Performance Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>80</td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on),max}$</td>
<td>5.5</td>
<td>mΩ</td>
</tr>
<tr>
<td>$I_D$</td>
<td>99</td>
<td>A</td>
</tr>
<tr>
<td>$Q_{GSS}$</td>
<td>43</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_G$</td>
<td>36</td>
<td>nC</td>
</tr>
</tbody>
</table>

Type / Ordering Code  | Package    | Marking  | Related Links |
----------------------|------------|----------|---------------|
IPP055N08NF2S         | PG-TO220-3 | 055N08NS | -             |
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1 Maximum ratings
at $T_A=25$ °C, unless otherwise specified

Table 2 Maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous drain current&lt;sup&gt;1&lt;/sup&gt;</td>
<td>$I_D$</td>
<td>-</td>
<td>-</td>
<td>99</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>58</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>18.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{GS}=10$ V, $T_C=25$ °C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{GS}=10$ V, $T_C=100$ °C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{GS}=6$ V, $T_C=100$ °C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{GS}=10$ V, $T_A=25$ °C, $R_{thJA}=40$ °C/W&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>Pulsed drain current&lt;sup&gt;3&lt;/sup&gt;</td>
<td>$I_{D,pulse}$</td>
<td>-</td>
<td>-</td>
<td>396</td>
</tr>
<tr>
<td>Avalanche energy, single pulse&lt;sup&gt;4&lt;/sup&gt;</td>
<td>$E_{AS}$</td>
<td>-</td>
<td>-</td>
<td>58</td>
</tr>
<tr>
<td>Gate source voltage</td>
<td>$V_{GS}$</td>
<td>-20</td>
<td>-</td>
<td>20</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>$P_{tot}$</td>
<td>-</td>
<td>-</td>
<td>107</td>
</tr>
<tr>
<td>Operating and storage temperature</td>
<td>$T_J, T_{stg}$</td>
<td>-55</td>
<td>-</td>
<td>175</td>
</tr>
</tbody>
</table>

2 Thermal characteristics

Table 3 Thermal characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal resistance, junction - case</td>
<td>$R_{thJC}$</td>
<td>-</td>
<td>-</td>
<td>1.4</td>
</tr>
<tr>
<td>Thermal resistance, junction - ambient, 6 cm&lt;sup&gt;2&lt;/sup&gt; cooling area&lt;sup&gt;2&lt;/sup&gt;</td>
<td>$R_{thJA}$</td>
<td>-</td>
<td>-</td>
<td>40</td>
</tr>
<tr>
<td>Thermal resistance, junction - ambient, minimal footprint</td>
<td>$R_{thJA}$</td>
<td>-</td>
<td>-</td>
<td>62</td>
</tr>
</tbody>
</table>

<sup>1</sup> Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

<sup>2</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3</sup> See Diagram 3 for more detailed information

<sup>4</sup> See Diagram 13 for more detailed information
# 3 Electrical characteristics

at \( T_j=25 \, ^\circ\text{C} \), unless otherwise specified

## Table 4  Static characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Drain-source breakdown voltage</td>
<td>( V_{(BR)DSS} )</td>
<td>80</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Gate threshold voltage</td>
<td>( V_{GS(th)} )</td>
<td>2.2</td>
<td>3</td>
<td>3.8</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>( I_{DSS} )</td>
<td>-</td>
<td>0.1</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>Gate-source leakage current</td>
<td>( I_{GS} )</td>
<td>-</td>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>Drain-source on-state resistance</td>
<td>( R_{DS(on)} )</td>
<td>-</td>
<td>4.8</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>6.3</td>
<td>7.9</td>
</tr>
<tr>
<td>Gate resistance</td>
<td>( R_G )</td>
<td>-</td>
<td>1.3</td>
<td>-</td>
</tr>
<tr>
<td>Transconductance (^2)</td>
<td>( g_{fs} )</td>
<td>46</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

## Table 5  Dynamic characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>( C_{iss} )</td>
<td>-</td>
<td>2500</td>
<td>-</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>( C_{oss} )</td>
<td>-</td>
<td>420</td>
<td>-</td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>( C_{rss} )</td>
<td>-</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>( t_{d(on)} )</td>
<td>-</td>
<td>14</td>
<td>-</td>
</tr>
<tr>
<td>Rise time</td>
<td>( t_r )</td>
<td>-</td>
<td>37</td>
<td>-</td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>( t_{d(off)} )</td>
<td>-</td>
<td>21</td>
<td>-</td>
</tr>
<tr>
<td>Fall time</td>
<td>( t_f )</td>
<td>-</td>
<td>7</td>
<td>-</td>
</tr>
</tbody>
</table>

## Table 6  Gate charge characteristics \(^3\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Gate to source charge</td>
<td>( Q_{gs} )</td>
<td>-</td>
<td>12</td>
<td>-</td>
</tr>
<tr>
<td>Gate charge at threshold</td>
<td>( Q_{g(th)} )</td>
<td>-</td>
<td>7.4</td>
<td>-</td>
</tr>
<tr>
<td>Gate to drain charge</td>
<td>( Q_{gd} )</td>
<td>-</td>
<td>8</td>
<td>-</td>
</tr>
<tr>
<td>Switching charge</td>
<td>( Q_{sw} )</td>
<td>-</td>
<td>13</td>
<td>-</td>
</tr>
<tr>
<td>Gate charge total (^2)</td>
<td>( Q_g )</td>
<td>-</td>
<td>36</td>
<td>54</td>
</tr>
<tr>
<td>Gate plateau voltage</td>
<td>( V_{plateau} )</td>
<td>-</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>Output charge</td>
<td>( Q_{oss} )</td>
<td>-</td>
<td>43</td>
<td>-</td>
</tr>
</tbody>
</table>

1) \( R_{DS(on)} \) is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 m\text{Ohm}\/mm per leg.

2) Defined by design. Not subject to production test.

3) See “Gate charge waveforms” for parameter definition.
## Table 7  Reverse diode

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode continuous forward current</td>
<td>$I_S$</td>
<td>-</td>
<td>-</td>
<td>82</td>
<td>A</td>
<td>$T_C=25 , ^\circ C$</td>
</tr>
<tr>
<td>Diode pulse current</td>
<td>$I_{S,\text{pulse}}$</td>
<td>-</td>
<td>-</td>
<td>396</td>
<td>A</td>
<td>$T_C=25 , ^\circ C$</td>
</tr>
<tr>
<td>Diode forward voltage</td>
<td>$V_{SD}$</td>
<td>-</td>
<td>0.94</td>
<td>1.2</td>
<td>V</td>
<td>$V_{GS}=0 , V, , I_F=60 , A, , T_J=25 , ^\circ C$</td>
</tr>
<tr>
<td>Reverse recovery time</td>
<td>$t_r$</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>ns</td>
<td>$V_R=40 , V, , I_R=60 , A, , \frac{dI_R}{dt}=500 , \text{A/µs}$</td>
</tr>
<tr>
<td>Reverse recovery charge</td>
<td>$Q_{rr}$</td>
<td>-</td>
<td>154</td>
<td>-</td>
<td>nC</td>
<td>$V_R=40 , V, , I_R=60 , A, , \frac{dI_R}{dt}=500 , \text{A/µs}$</td>
</tr>
</tbody>
</table>
4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**

![Power dissipation diagram](image)

\[ P_{\text{tot}} = f(T_C) \]

**Diagram 2: Drain current**

![Drain current diagram](image)

\[ I_D = f(T_C); \quad V_{GS} \geq 10 \text{ V} \]

**Diagram 3: Safe operating area**

![Safe operating area diagram](image)

\[ I_D = f(V_{DS}); \quad T_C = 25 ^\circ \text{C}; \quad D = 0; \quad \text{parameter: } t_p \]

**Diagram 4: Max. transient thermal impedance**

![Max. transient thermal impedance diagram](image)

\[ Z_{\text{thJC}} = f(t_p); \quad \text{parameter: } D = t_p/T \]
Diagram 5: Typ. output characteristics

\[ I_D = f(V_{DS}), \ T_j=25 \, ^\circ C; \text{parameter: } V_{GS} \]

Diagram 6: Typ. drain-source on resistance

\[ R_{DS(on)} = f(I_D), \ T_j=25 \, ^\circ C; \text{parameter: } V_{GS} \]

Diagram 7: Typ. transfer characteristics

\[ I_D = f(V_{GS}), \ |V_{DS}|>2|I_D|R_{DS(on)\text{max}}; \text{parameter: } T_j \]

Diagram 8: Typ. drain-source on resistance

\[ R_{DS(on)} = f(V_{GS}), \ I_D=60 \, A; \text{parameter: } T_j \]
**Diagram 9: Normalized drain-source on resistance**

\[ R_{\text{DS(on)}}(\text{normalized to } 25^\circ C) = f(T_j) \]

\[ I_D = 60 \text{ A}, \ V_{GS} = 10 \text{ V} \]

**Diagram 10: Typ. gate threshold voltage**

\[ V_{\text{GS(th)}} = f(T_j), \ V_{GS} = V_{DS}; \ \text{parameter: } I_D \]

**Diagram 11: Typ. capacitances**

\[ C = f(V_{DS}); \ V_{SS} = 0 \text{ V}; \ f = 1 \text{ MHz} \]

**Diagram 12: Typ. forward characteristic of reverse diode**

\[ I_F = f(V_{SD}); \ \text{parameter: } T_j \]
Diagram 13: Avalanche characteristics

\[ I_{AV} [\mu A] \]

\[ t_{AV} [\mu s] \]

\[ 10^{-1} \]

\[ 10^{0} \]

\[ 10^{1} \]

\[ 10^{2} \]

\[ 10^{3} \]

\[ 150 ^\circ C \]

\[ 100 ^\circ C \]

\[ 25 ^\circ C \]

\( I_{AS} = f(t_{AV}) \); \( R_{GS} = 25 \Omega \); parameter: \( T_{j, start} \)

Diagram 14: Typ. gate charge

\[ Q_{gate} [nC] \]

\[ V_{GS} [V] \]

\[ 0 \]

\[ 5 \]

\[ 10 \]

\[ 15 \]

\[ 20 \]

\[ 25 \]

\[ 30 \]

\[ 35 \]

\[ 40 \]

\[ 4 \]

\[ 2 \]

\[ 6 \]

\[ 8 \]

\[ 10 \]

\[ 16 \ V \]

\[ 40 \ V \]

\[ 64 \ V \]

\( V_{GS} = f(Q_{gate}) \), \( I_{D} = 60 \ A \) pulsed, \( T_{j} = 25 ^\circ C \); parameter: \( V_{DD} \)

Diagram 15: Drain-source breakdown voltage

\[ V_{BR(DSS)} [V] \]

\[ T_{j} [^\circ C] \]

\[ -75 \]

\[ -50 \]

\[ -25 \]

\[ 0 \]

\[ 25 \]

\[ 50 \]

\[ 75 \]

\[ 100 \]

\[ 125 \]

\[ 150 \]

\[ 175 \]

\[ 200 \]

\[ 76 \]

\[ 78 \]

\[ 80 \]

\[ 82 \]

\[ 84 \]

\[ 86 \]

\[ 88 \]

\( V_{BR(DSS)} = f(T_{j}) \); \( I_{D} = 1 \ mA \)

Diagram Gate charge waveforms

\( V_{GS} \)

\( Q_{g} \)

\( V_{g(t)} \)

\( Q_{g(t)} \)

\( Q_{sw} \)

\( Q_{gd} \)

\( Q_{gs} \)

Final Data Sheet 9

Rev. 2.1, 2022-06-15
5 Package Outlines

NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

Figure 1 Outline PG-TO220-3, dimensions in mm
Revision History

IPP055N08NF2S

Revision: 2022-06-15, Rev. 2.1

Previous Revision

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Subjects (major changes since last revision)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0</td>
<td>2020-12-18</td>
<td>Release of final version</td>
</tr>
<tr>
<td>2.1</td>
<td>2022-06-15</td>
<td>Skip condition &quot;Operating and storage tempt.&quot;, update trr and Qrr, footnotes and Diagram 12</td>
</tr>
</tbody>
</table>

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