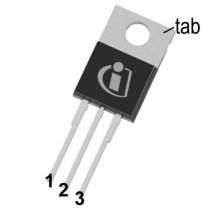
MOSFET

PG-TO220-3

StrongIRFET™ 2 Power-Transistor, 100 V



Features

- Optimized for a wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

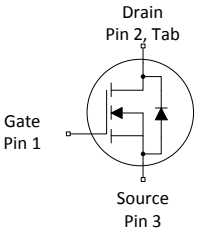
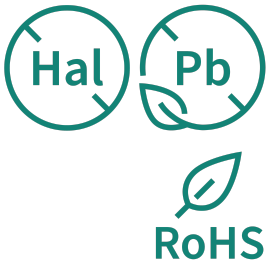


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	3.0	mΩ
I_D	179	A
Q_{oss}	109	nC
Q_G	85	nC



Part number	Package	Marking	Related links
IPP030N10NF2S	PG-TO220-3	030N10NS	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	179 137 129 25	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=6 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA}=40 °C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	716	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	367	mJ	I_D=80 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	250 3.8	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.6	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5]	R_{thJA}	-	-	40	°C/W	
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	

[5] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	V_{DS}=V_{GS}, I_D=140 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance [6]	$R_{DS(on)}$	-	2.5 3.1	3.0 3.7	mΩ	V_{GS}=10 V, I_D=80 A V_{GS}=6 V, I_D=40 A
Gate resistance	R_G	-	2.0	-	Ω	-
Transconductance [7]	g_{fs}	85	170	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=80 A

[6] $R_{DS(on)}$ is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.

[7] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	6000	-	pF	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz
Output capacitance	C_{oss}	-	930	-	pF	
Reverse transfer capacitance	C_{rss}	-	41	-	pF	
Turn-on delay time	$t_{d(on)}$	-	19	-	ns	V_{DD}=50 V, V_{GS}=10 V, I_D=80 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	20	-	ns	
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	
Fall time	t_f	-	17	-	ns	

Table 6 Gate charge characteristics [8]

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	28	-	nC	V_{DD}=50 V, I_D=80 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	18.1	-	nC	
Gate to drain charge	Q_{gd}	-	17.4	-	nC	
Switching charge	Q_{sw}	-	27	-	nC	
Gate charge total [9]	Q_g	-	85	127	nC	
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	
Output charge	Q_{oss}	-	109	-	nC	V_{DS}=50 V, V_{GS}=0 V

[8] See "Gate charge waveforms" for parameter definition

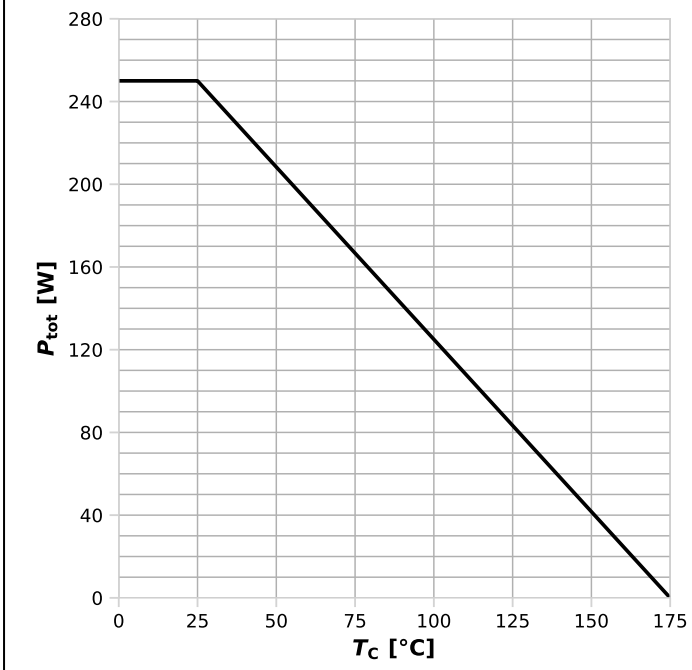
[9] Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	151	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	716	A	
Diode forward voltage	V_{SD}	-	0.88	1.2	V	V_{GS}=0 V, I_F=80 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	37	-	ns	V_R=50 V, I_F=80 A, di_F/dt=500 A/µs
Reverse recovery charge	Q_{rr}	-	257	-	nC	

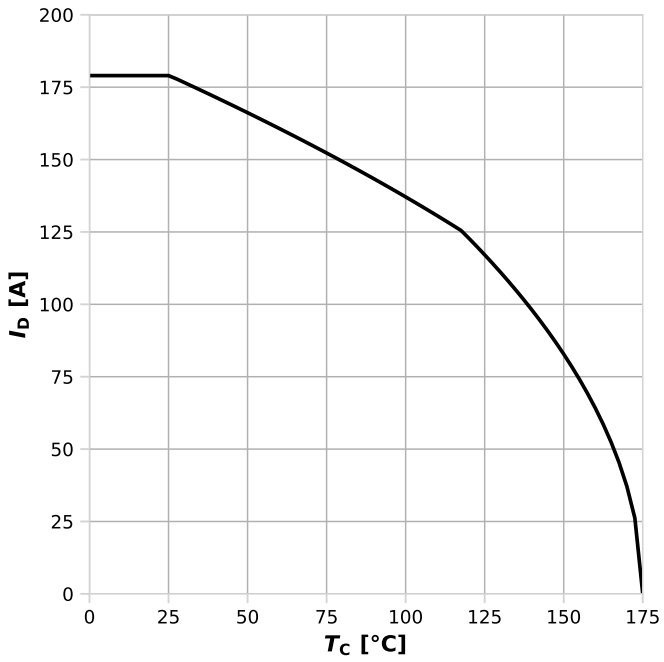
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



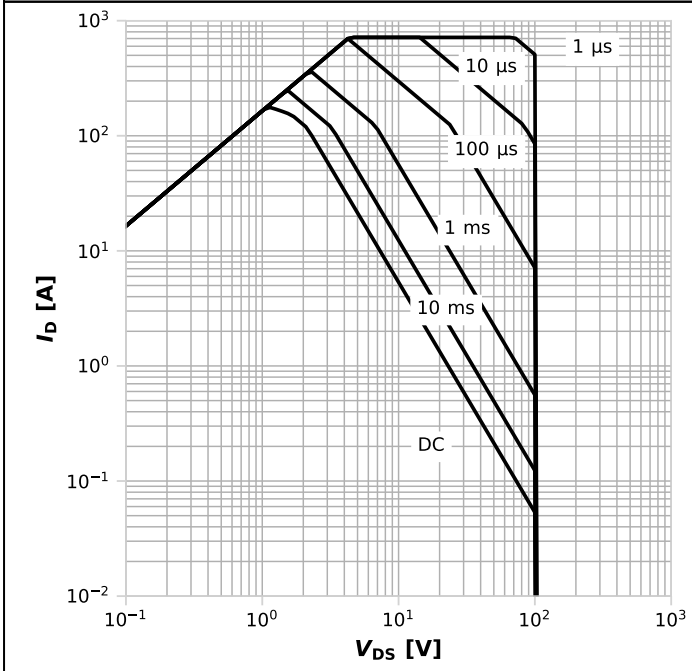
P_{tot}=f(T_C)

Diagram 2: Drain current



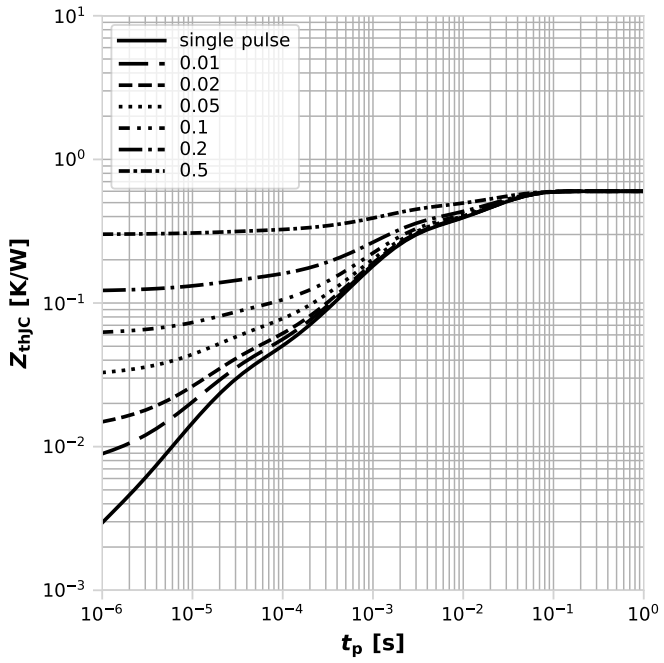
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC}=f(t_p); parameter: D=t_p/T

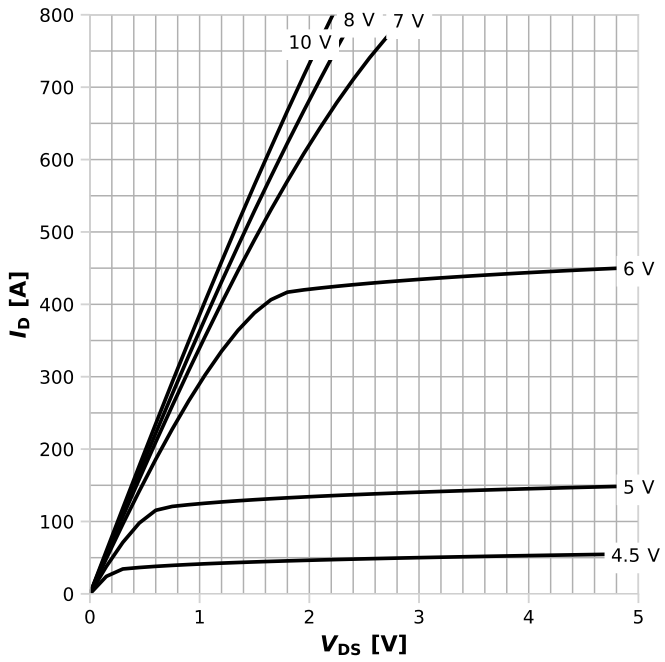
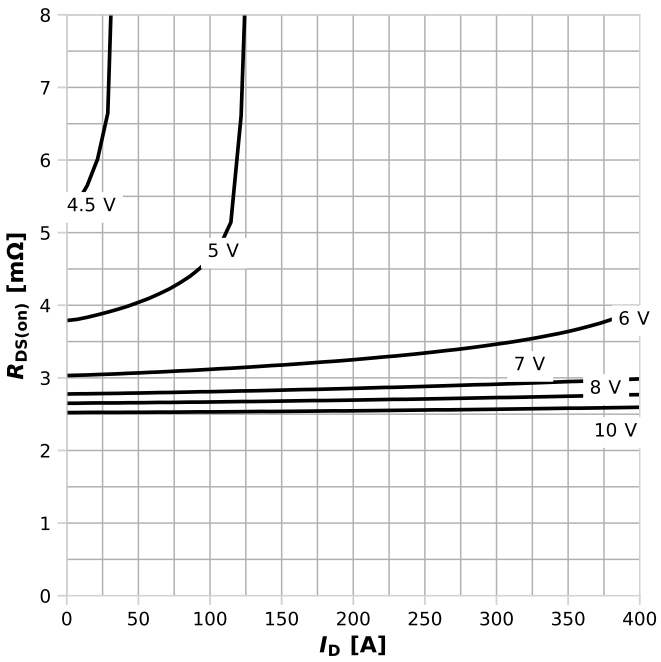
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

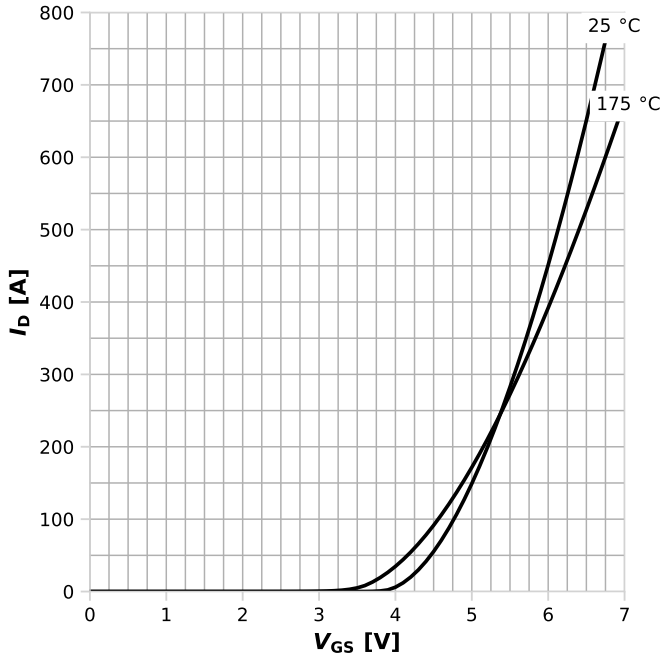
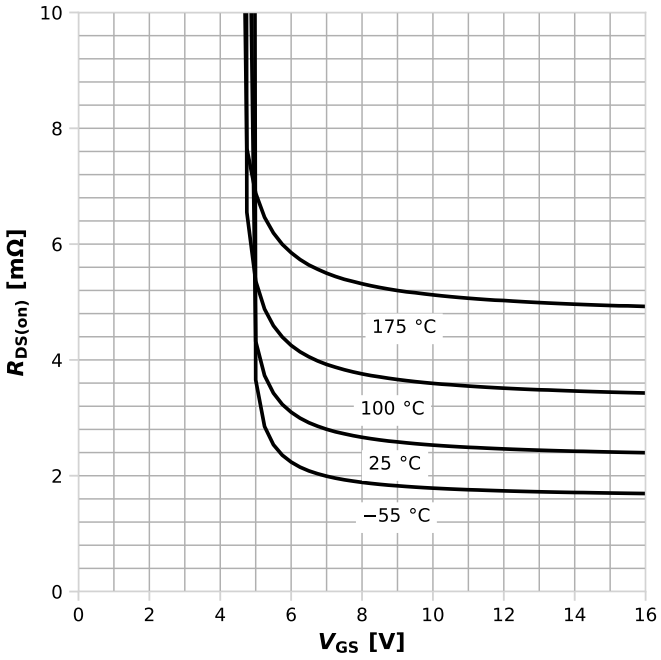
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on resistance
	
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j	$R_{DS(on)}$=f(V_{GS}), I_D=80 A; parameter: T_j

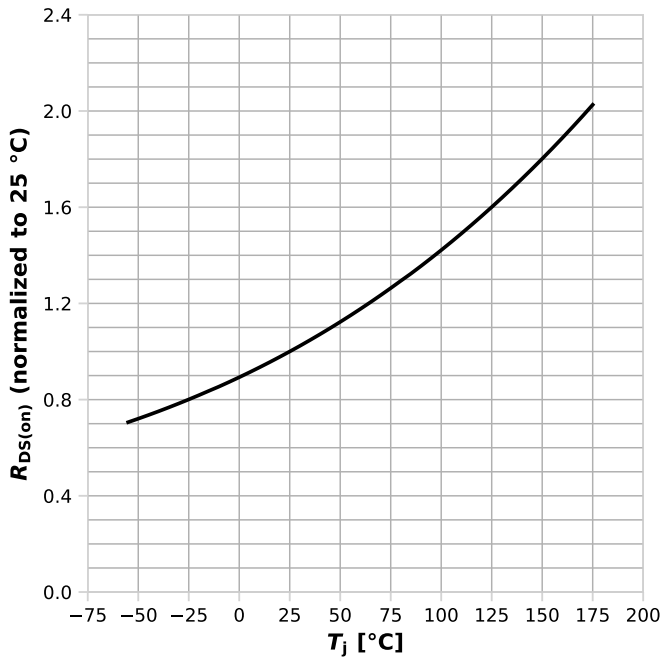
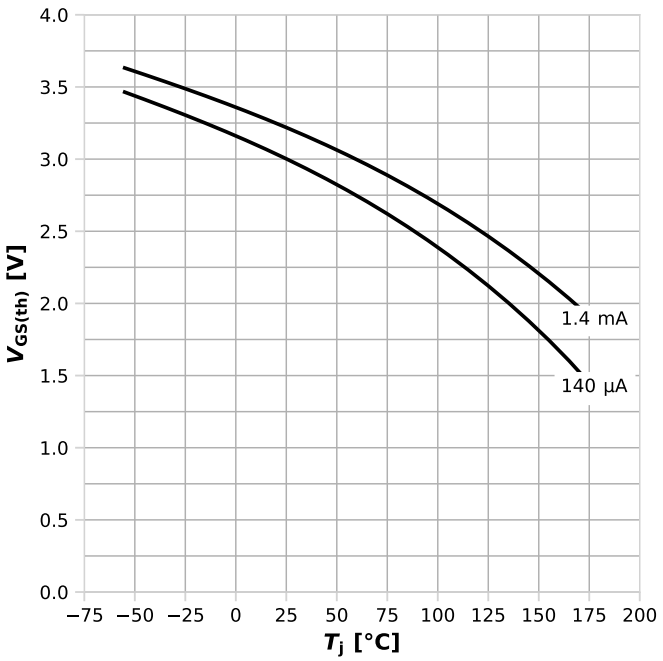
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=80 A, V_{GS}=10 V	$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

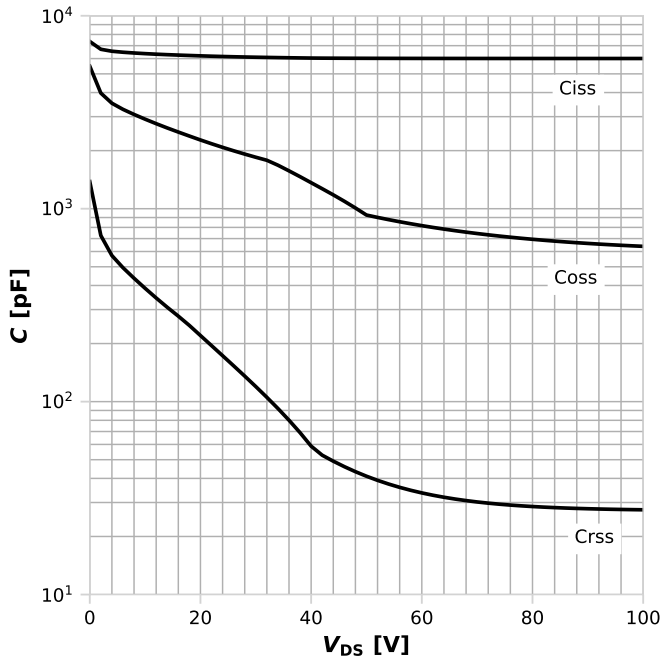
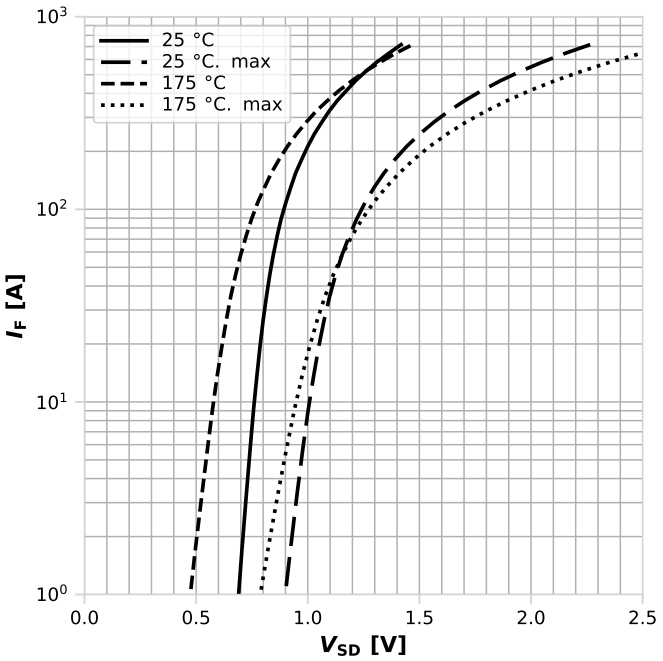
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

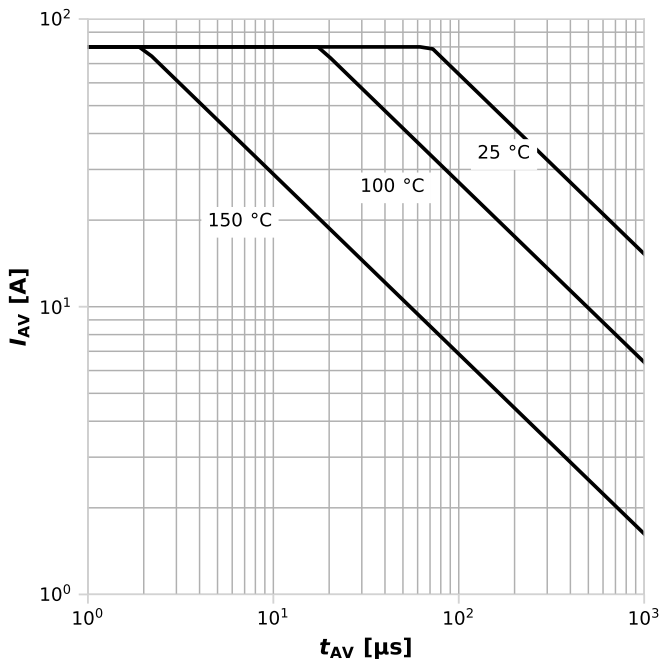
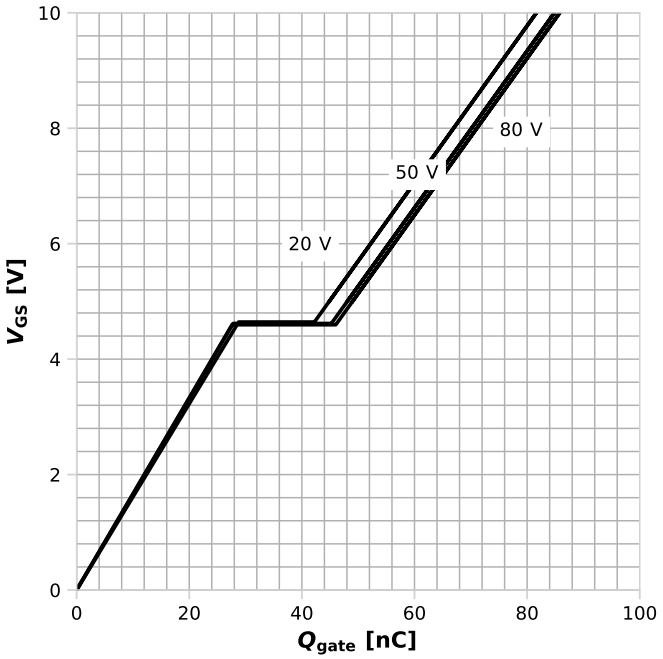
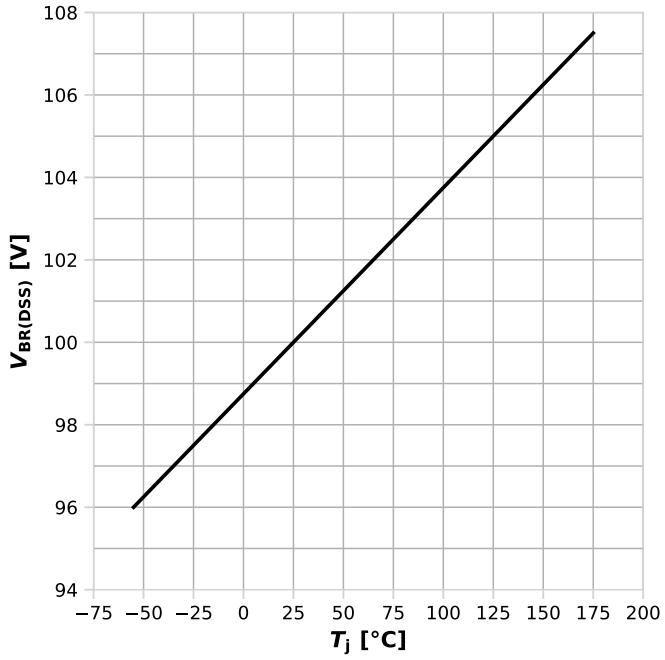
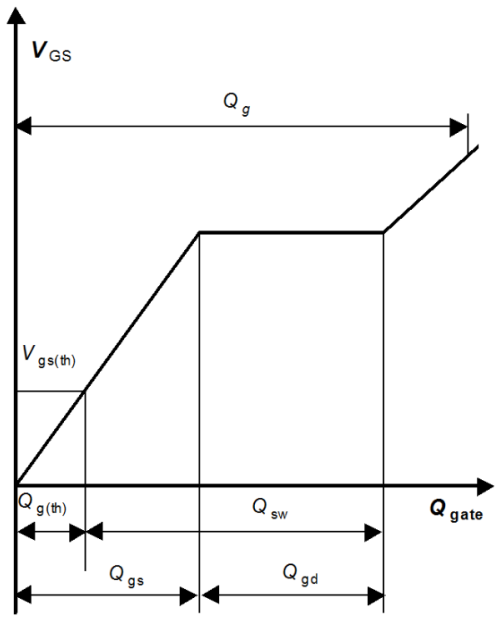
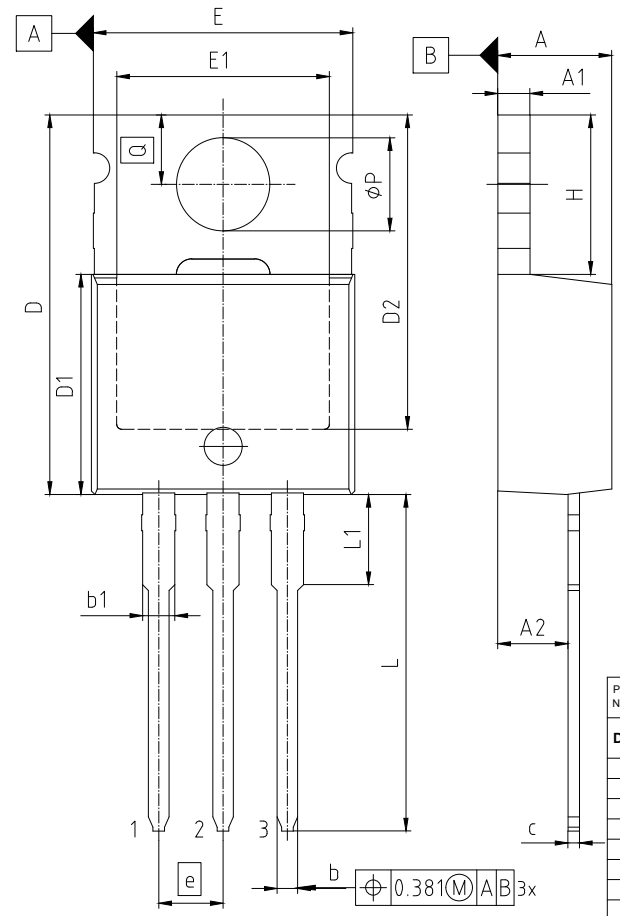
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=80 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.25	4.75
A1	1.14	1.40
A2	2.47	2.92
b	0.71	0.97
b1	1.14	1.78
c	0.36	0.61
D	14.32	15.80
D1	8.39	9.20
D2	11.89	12.80
E	9.90	10.67
E1	8.10	8.74
e	2.54	
N	3	
H	6.00	6.70
L	13.00	14.40
L1	3.56	4.06
øP	3.54	3.90
Q	2.54	2.94

NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

Figure 1 Outline PG-TO220-3, dimensions in mm

Revision history

IPP030N10NF2S

Revision 2025-01-20, Rev. 1.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2025-01-20	Release of final datasheet

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