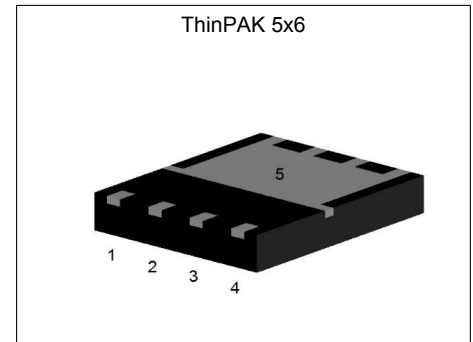


## MOSFET

### 700V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target applications in Charger and Adapter markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.

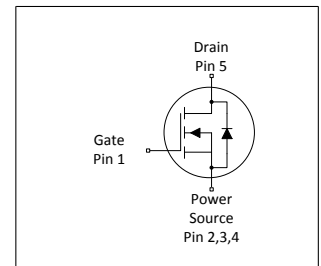


### Features

- Extremely low losses due to very low FOM  $R_{DS(on)} \cdot Q_g$  and  $E_{oss}$
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound

### Applications

(QR) Flyback in low power chargers for mobile devices and power tools



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	750	V
$R_{DS(on),max}$	2100	m $\Omega$
$Q_{g,typ}$	7.8	nC
$I_{D,pulse}$	6.3	A
$E_{oss}@400V$	0.85	$\mu$ J
Body diode di/dt	500	A/ $\mu$ s



Type / Ordering Code	Package	Marking	Related Links
IPL70R2K1CES	ThinPAK 5x6 SMD	7R2K1CE	see Appendix A

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	4
Electrical characteristics .....	5
Electrical characteristics diagrams .....	7
Test Circuits .....	11
Package Outlines .....	12
Appendix A .....	13
Revision History .....	14
Trademarks .....	14
Disclaimer .....	14

## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	2.3 1.5	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	6.3	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	11	mJ	$I_D=0.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	0.07	mJ	$I_D=0.4\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, repetitive	$I_{AR}$	-	-	0.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	50	V/ns	$V_{DS}=0\dots480\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	22	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Continuous diode forward current	$I_S$	-	-	2.0	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	6.3	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	15	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>f</sub> /dt	-	-	500	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq I_S$ , $T_j=25^\circ\text{C}$ see table 8

<sup>1)</sup> Limited by  $T_{j,max}$ . Maximum duty cycle  $D=0.75$

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	5.6	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave & reflow soldering allowed	$T_{sold}$	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	700	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	2.5	3.0	3.5	V	$V_{DS}=V_{GS}, I_D=0.07mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=700V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=700V, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.9	2.1	$\Omega$	$V_{GS}=10V, I_D=1.0A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=1.0A, T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	6.5	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	163	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Output capacitance	$C_{oss}$	-	14	-	pF	$V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	10	-	pF	$V_{GS}=0V, V_{DS}=0\dots480V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	33	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots480V$
Turn-on delay time	$t_{d(on)}$	-	5.3	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$ ; see table 9
Rise time	$t_r$	-	3.7	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$ ; see table 9
Turn-off delay time	$t_{d(off)}$	-	24	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$ ; see table 9
Fall time	$t_f$	-	18	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=1.1A,$ $R_G=10.2\Omega$ ; see table 9

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	0.9	-	nC	$V_{DD}=480V, I_D=1.1A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	4.3	-	nC	$V_{DD}=480V, I_D=1.1A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	7.8	-	nC	$V_{DD}=480V, I_D=1.1A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=480V, I_D=1.1A, V_{GS}=0$ to 10V

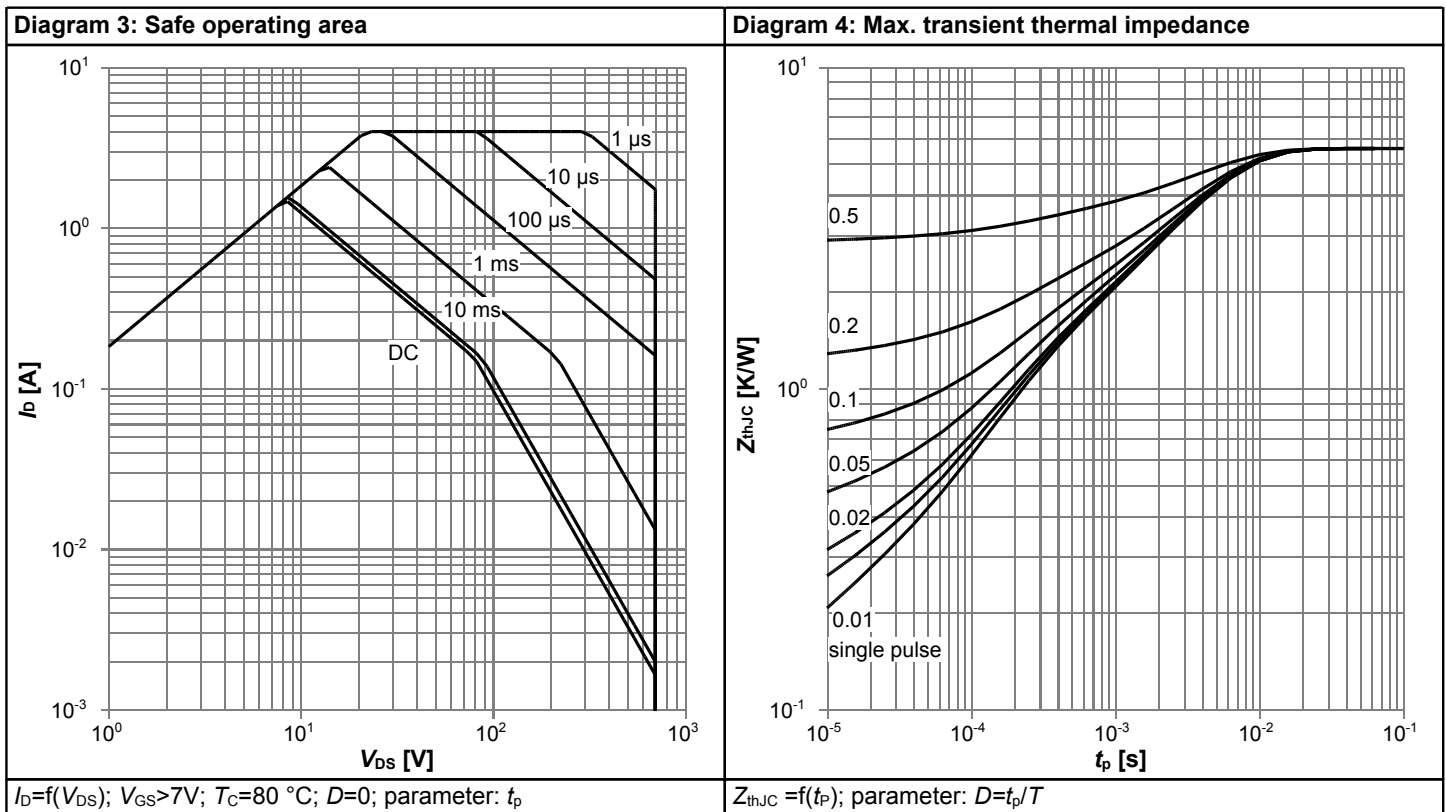
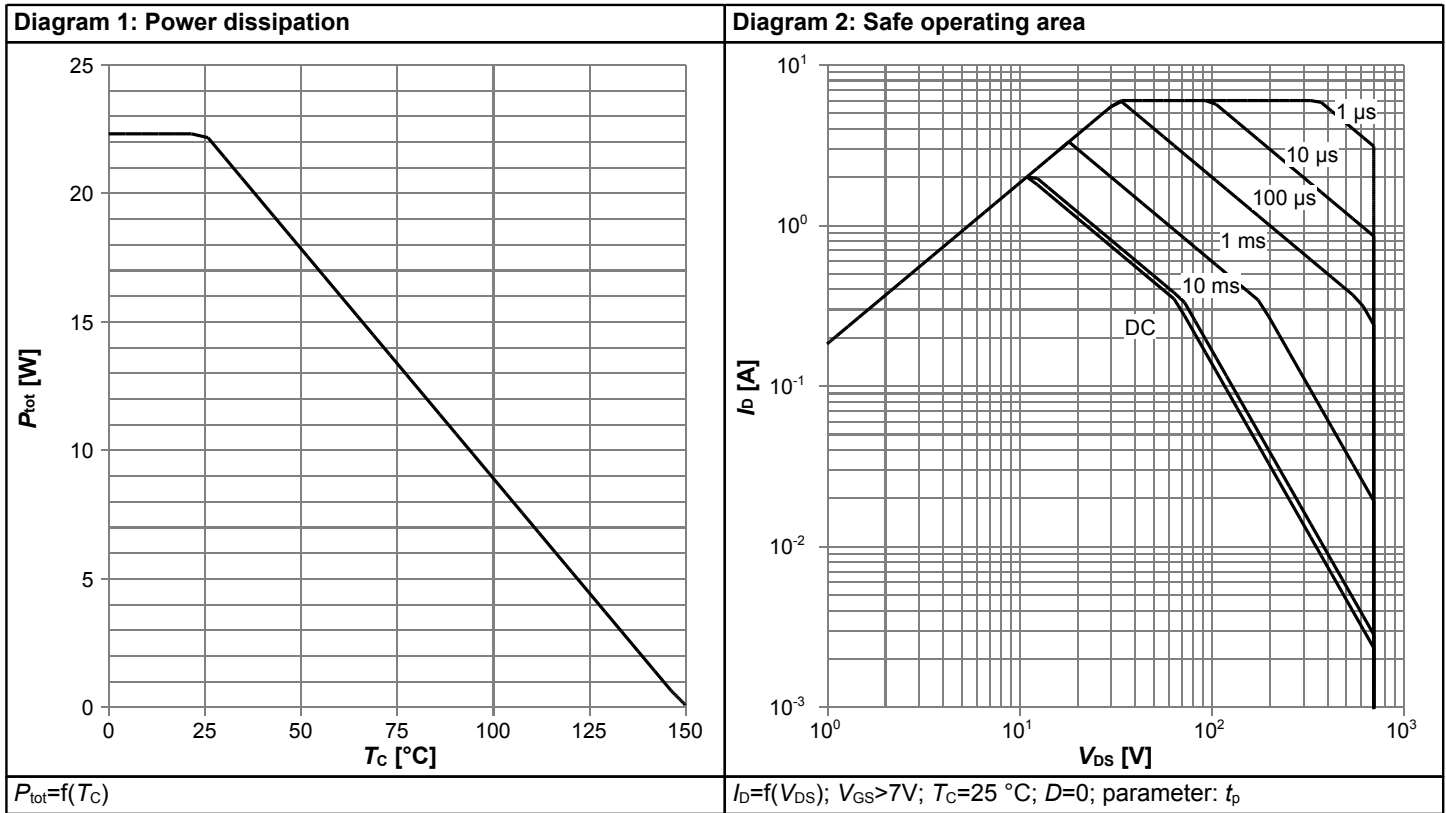
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 480V

**Table 7 Reverse diode characteristics**

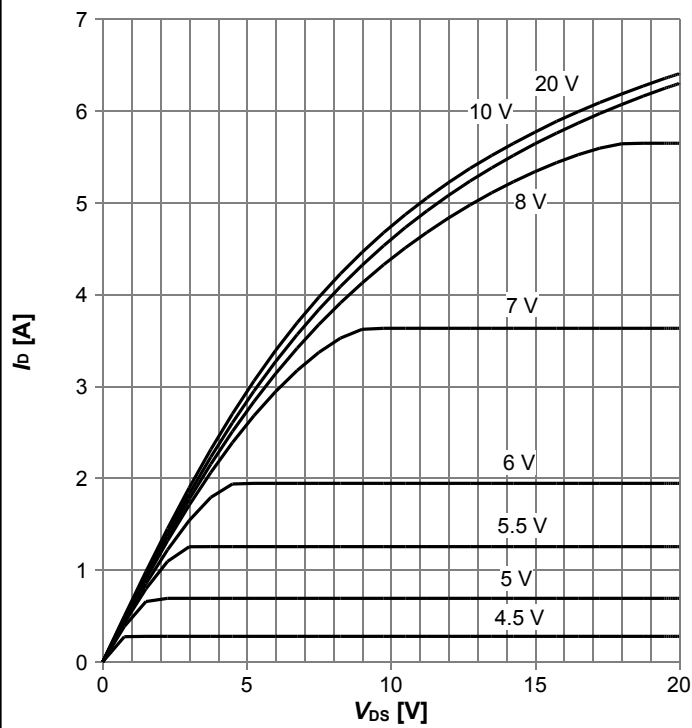
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.9	-	V	$V_{GS}=0V, I_F=1.1A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	194	-	ns	$V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	1.1	-	$\mu C$	$V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	11	-	A	$V_R=400V, I_F=1.1A, di_F/dt=100A/\mu s$ ; see table 8

### 4 Electrical characteristics diagrams



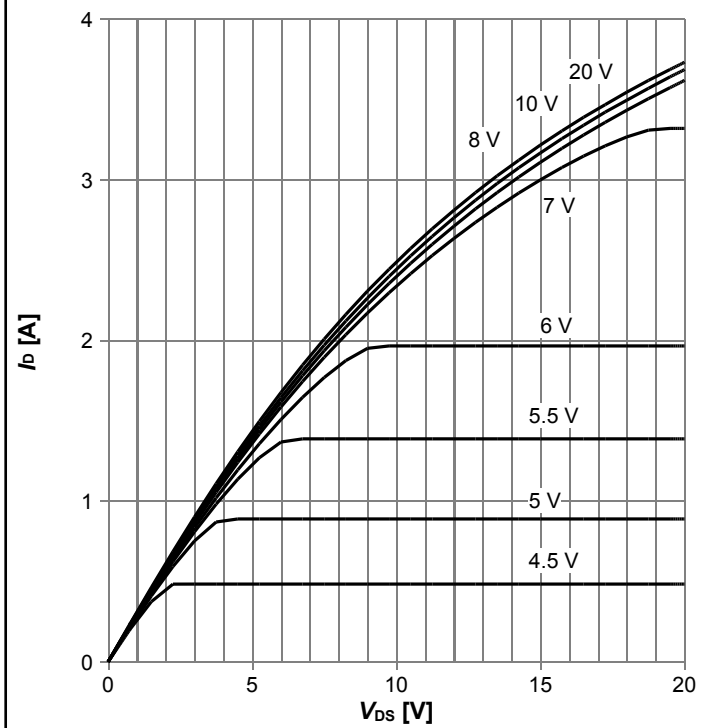
# 700V CoolMOS™ CE Power Transistor IPL70R2K1CES

Diagram 5: Typ. output characteristics



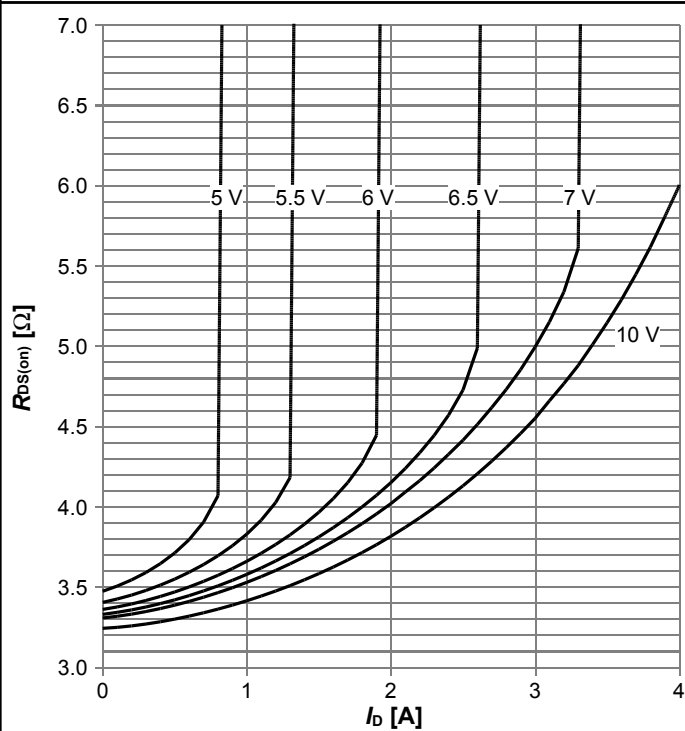
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 6: Typ. output characteristics



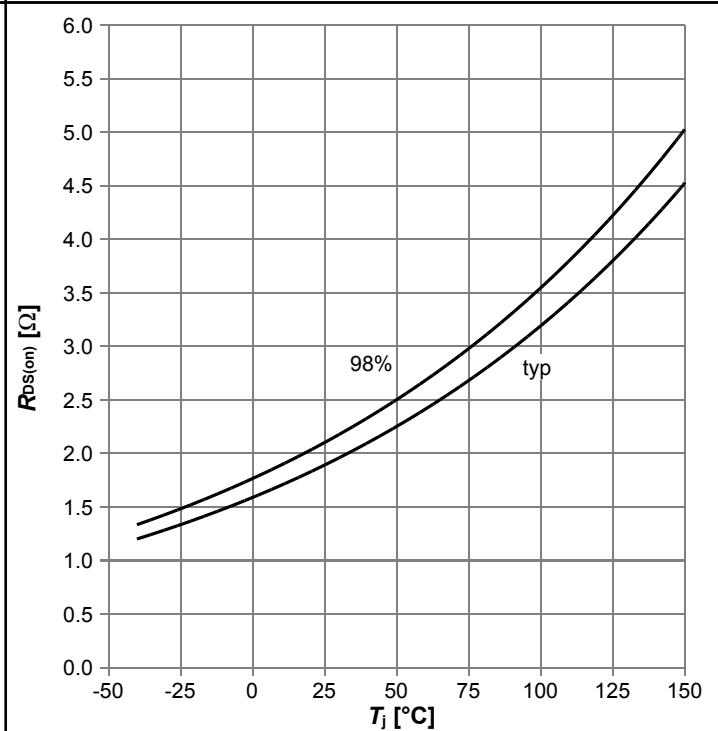
$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

Diagram 8: Drain-source on-state resistance

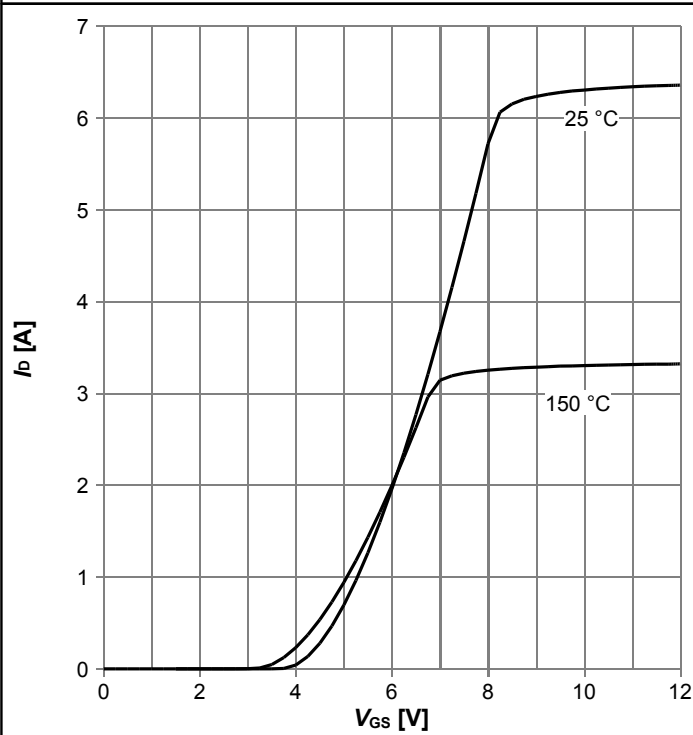


$R_{DS(on)}=f(T_j); I_D=1.0\text{ A}; V_{GS}=10\text{ V}$



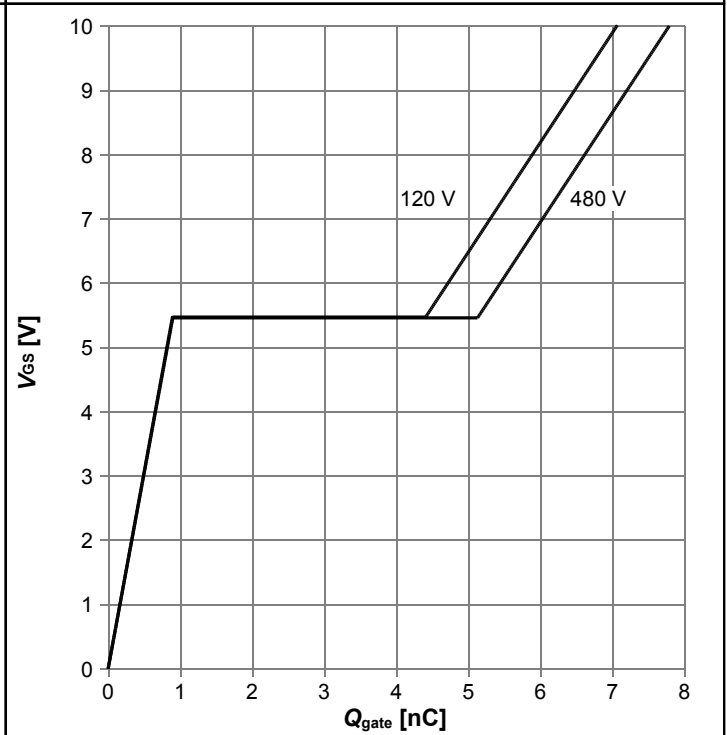
# 700V CoolMOS™ CE Power Transistor IPL70R2K1CES

**Diagram 9: Typ. transfer characteristics**



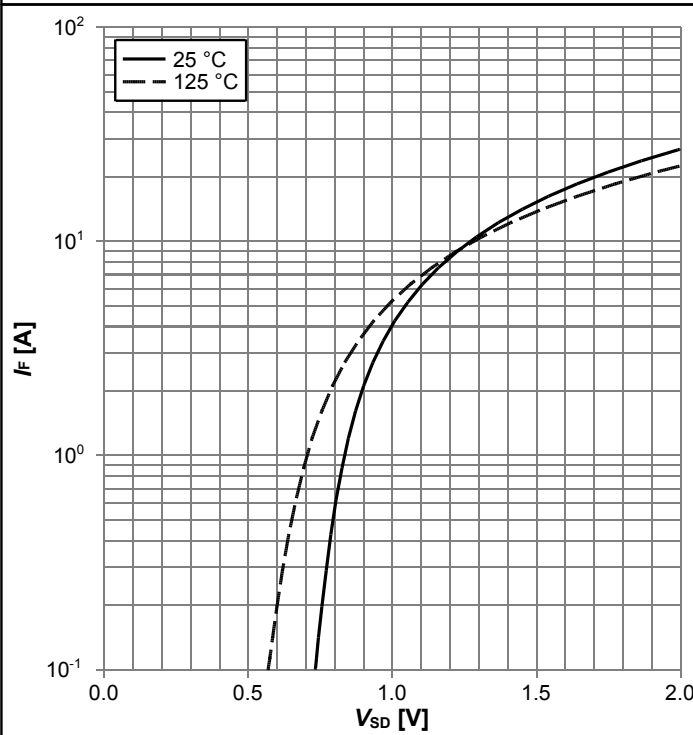
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

**Diagram 10: Typ. gate charge**



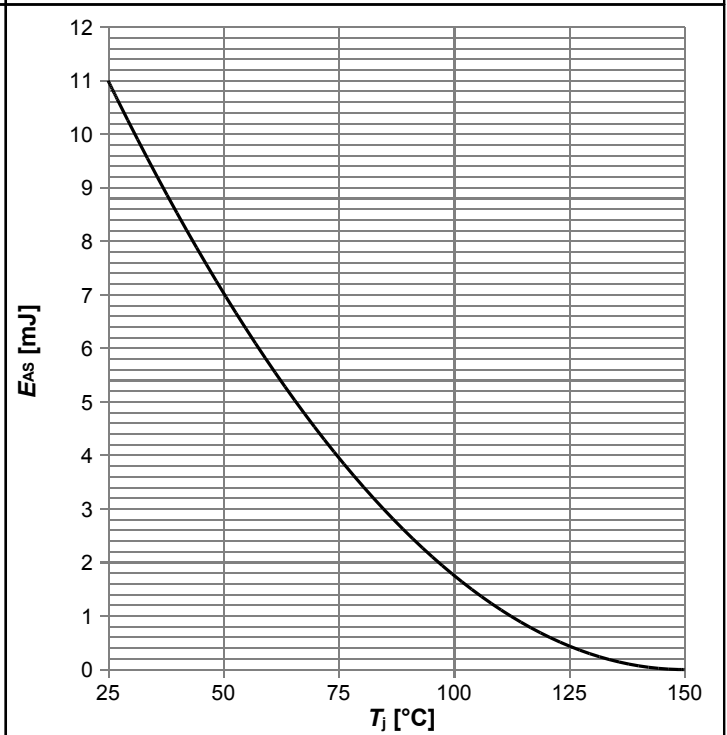
$V_{GS} = f(Q_{gate})$ ;  $I_D = 1.1 A$  pulsed; parameter:  $V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



$I_F = f(V_{SD})$ ; parameter:  $T_j$

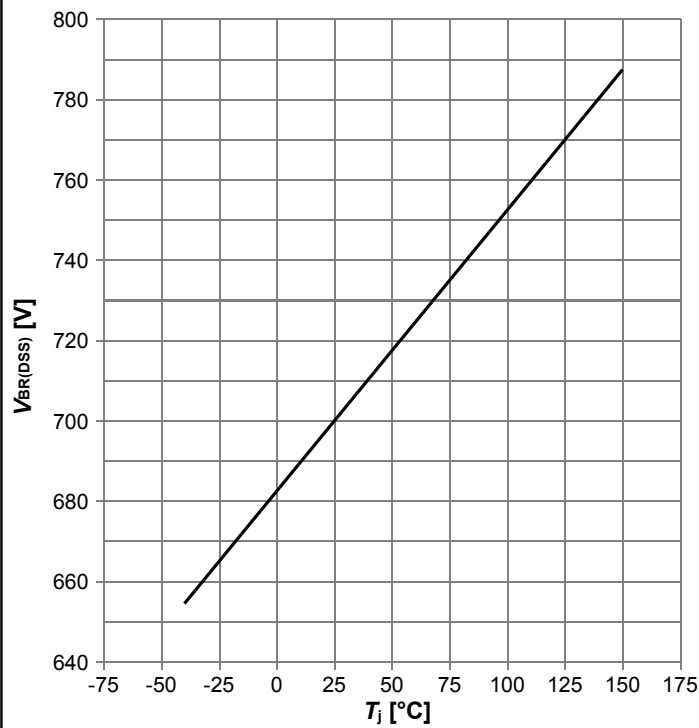
**Diagram 12: Avalanche energy**



$E_{AS} = f(T_j)$ ;  $I_D = 0.4 A$ ;  $V_{DD} = 50 V$

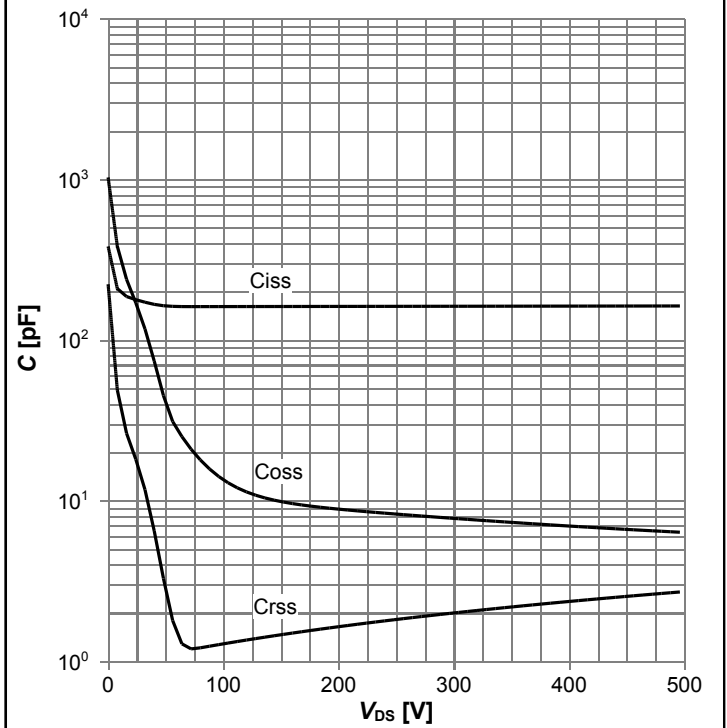
# 700V CoolMOS™ CE Power Transistor IPL70R2K1CES

**Diagram 13: Drain-source breakdown voltage**



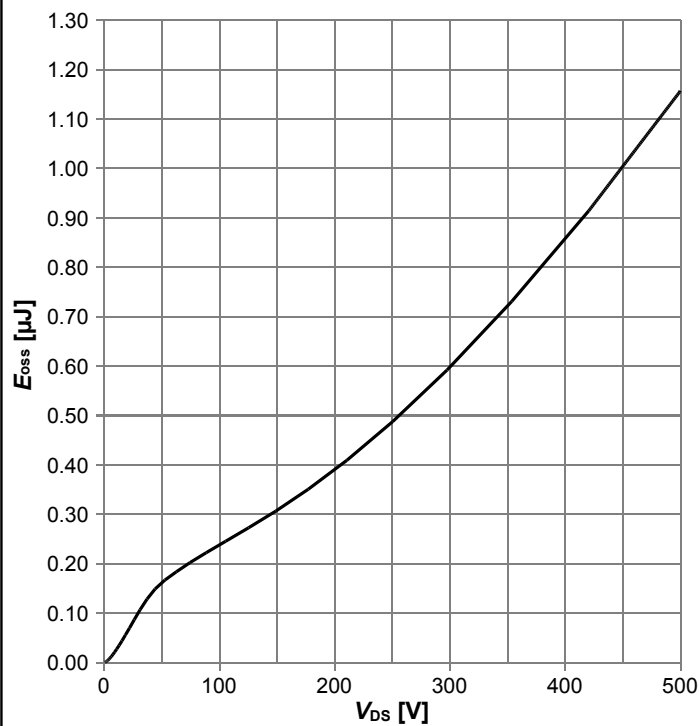
$V_{BR(DSS)}=f(T_j); I_D=1.0 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=1 \text{ MHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

**Table 8 Diode characteristics**

Test circuit for diode characteristics	Diode recovery waveform
<p><math>R_{g1} = R_{g2}</math></p>	<p><math>t_{rr} = t_F + t_S</math> <math>Q_{rr} = Q_F + Q_S</math></p>

**Table 9 switching times (ss)**

Switching times test circuit for inductive load	Switching times waveform

**Table 10 Unclamped inductive load (ss)**

Unclamped inductive load test circuit	Unclamped inductive waveform

## 6 Package Outlines

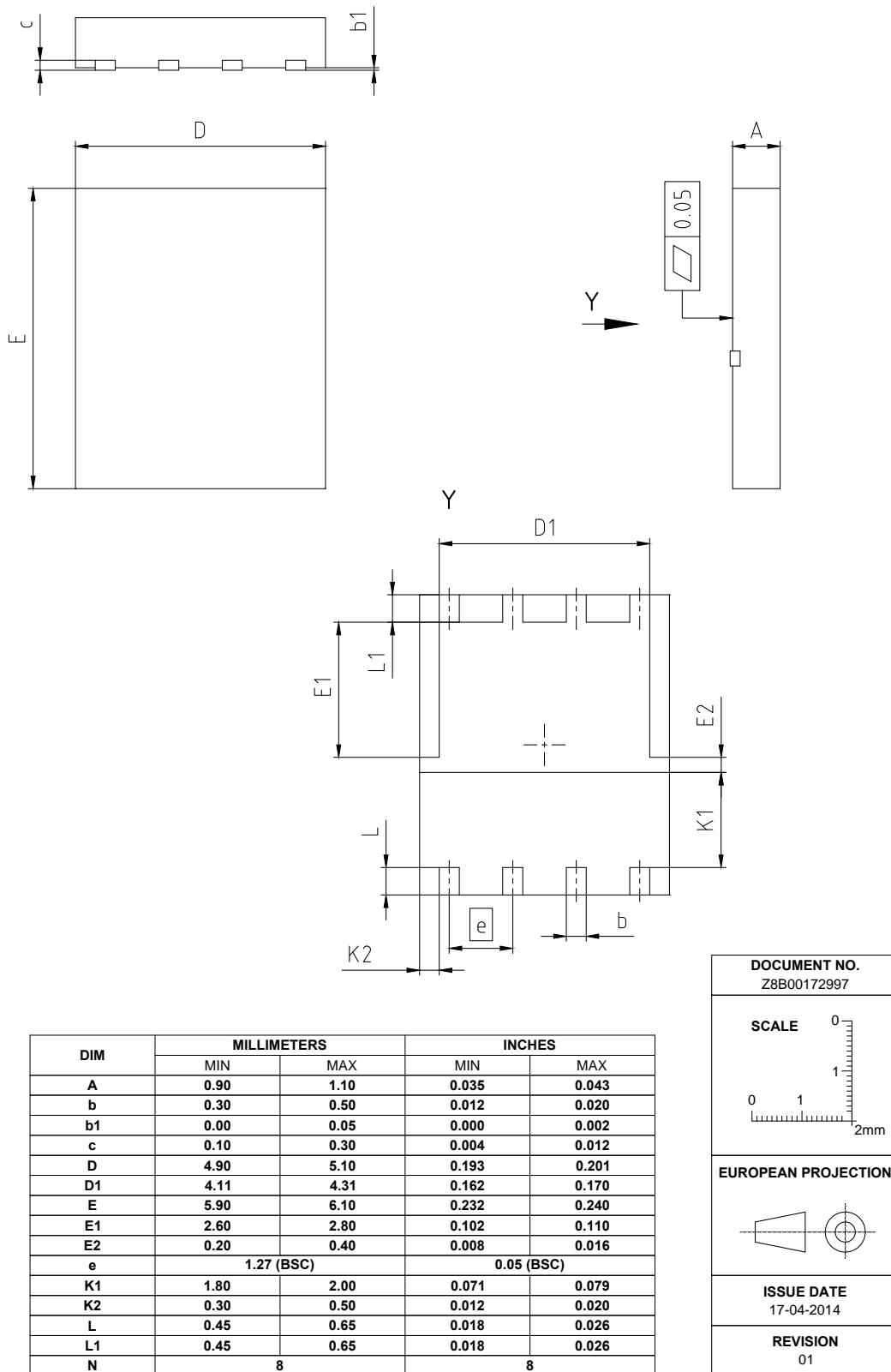


Figure 1 Outline ThinPAK 5x6 SMD, dimensions in mm/inches

## **7 Appendix A**

### **Table 11 Related Links**

- **IFX CoolMOS™ CE Webpage:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS™ CE application note:** [www.infineon.com](http://www.infineon.com)
- **IFX CoolMOS™ CE simulation model:** [www.infineon.com](http://www.infineon.com)
- **IFX Design tools:** [www.infineon.com](http://www.infineon.com)

## Revision History

IPL70R2K1CES

**Revision: 2016-04-15, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-04-15	Release of final version

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