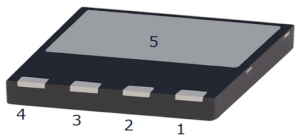
MOSFET

600V CoolMOS™ C7 Power Transistor

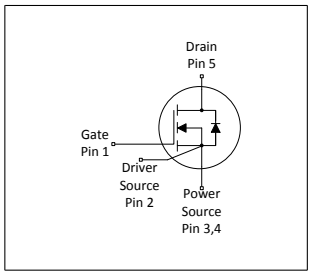
ThinPAK 8x8



CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)}$*A below 1Ohm*mm².



Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)}$*E_{oss} and $R_{DS(on)}$*Q_g
- Best in class $R_{DS(on)}$ /package
- SMD package with very low parasitic inductance for easy device control
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)
- 4pin kelvin source concept

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Optimized PCB assembly and layout solutions
- Suitable for applications such as server, telecom and solar
- Up to 0.5% better full load efficiency @100kHz compared to conventional 3pin package

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	65	mΩ
$Q_{g,typ}$	68	nC
$I_{D,pulse}$	135	A
$I_{D,continuous}$ @ T_j<150°C	51	A
E_{oss} @ 400V	8.1	µJ
Body diode di_F/dt	370	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPL60R065C7	PG-VSON-4	60C7065	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1)]	I_D	- -	- -	29 22	A	T_C=25°C T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	135	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	159	mJ	I_D=6.4A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.80	mJ	I_D=6.4A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	6.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	180	W	T_C=25°C
Storage temperature	T_{stg}	-40	-	150	°C	-
Operating junction temperature	T_j	-40	-	150	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	29	A	T_C=25°C
Diode pulse current[2)]	$I_{S,pulse}$	-	-	135	A	T_C=25°C
Reverse diode dv/dt[3)]	dv/dt	-	-	20	V/ns	V_{DS}=0...400V, I_{SD}<=9.9A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	370	A/µs	V_{DS}=0...400V, I_{SD}<=9.9A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1)] Limited by $T_{j\,max}$.
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.696	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL2a

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	V_{DS}=V_{GS}, I_D=0.8mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600, V_{GS}=0V, T_j=25°C V_{DS}=600, V_{GS}=0V, T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.056 0.125	0.065 -	Ω	V_{GS}=10V, I_D=15.9A, T_j=25°C V_{GS}=10V, I_D=15.9A, T_j=150°C
Gate resistance	R_G	-	0.8	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2850	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	54	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[1)]	$C_{o(er)}$	-	101	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[2)]	$C_{o(tr)}$	-	1050	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=15.9A, R_G=3.3Ω; see table 9
Rise time	t_r	-	5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=15.9A, R_G=3.3Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	57	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=15.9A, R_G=3.3Ω; see table 9
Fall time	t_f	-	3.5	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=15.9A, R_G=3.3Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	14	-	nC	V_{DD}=400V, I_D=15.9A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	23	-	nC	V_{DD}=400V, I_D=15.9A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	68	-	nC	V_{DD}=400V, I_D=15.9A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	V_{DD}=400V, I_D=15.9A, V_{GS}=0 to 10V

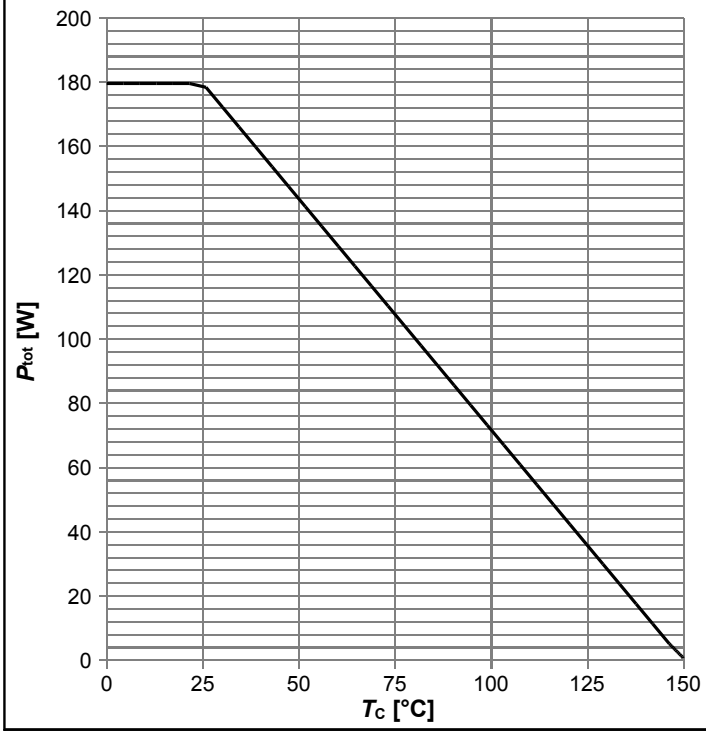
[1)] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2)] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=15.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	390	-	ns	V_R=400V, I_F=15.9A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	6	-	µC	V_R=400V, I_F=15.9A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	32	-	A	V_R=400V, I_F=15.9A, di_F/dt=100A/µs; see table 8

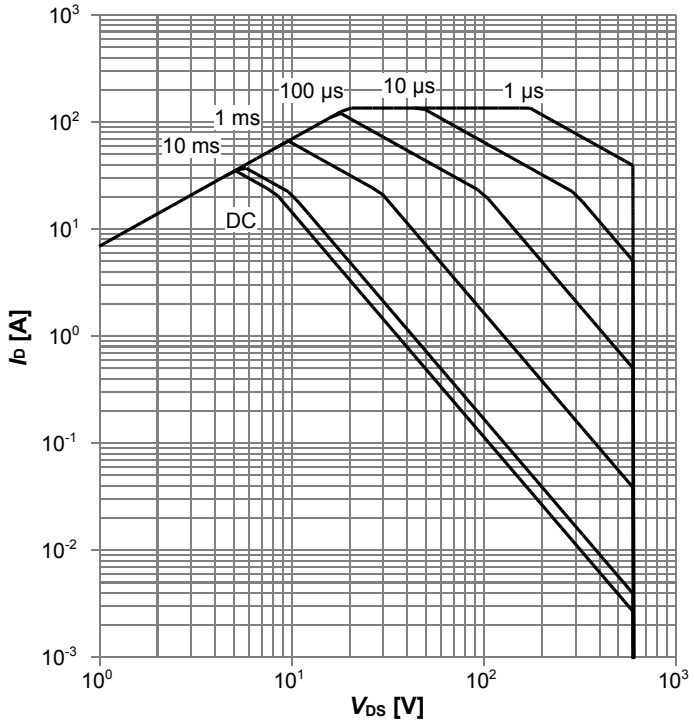
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



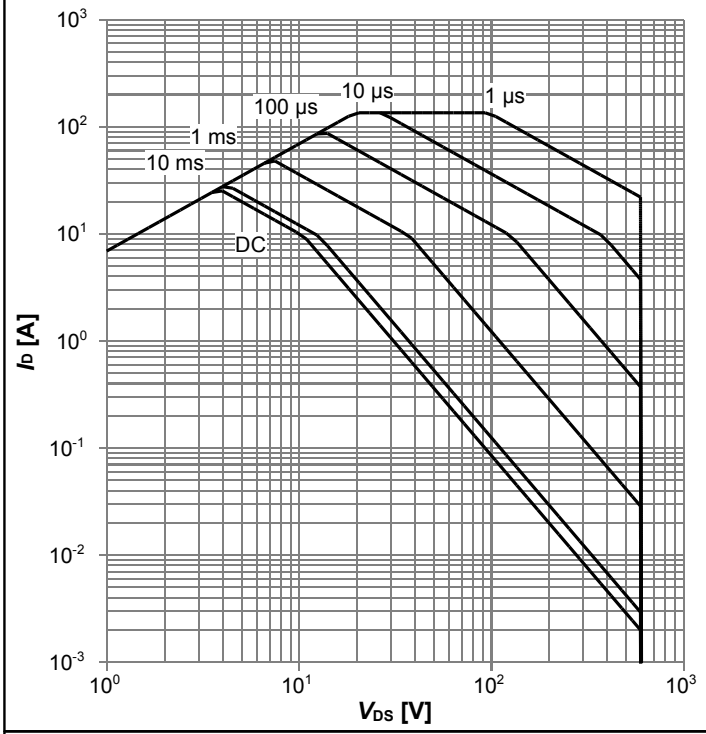
$P_{tot}=f(T_C)$

Diagram 2: Safe operating area



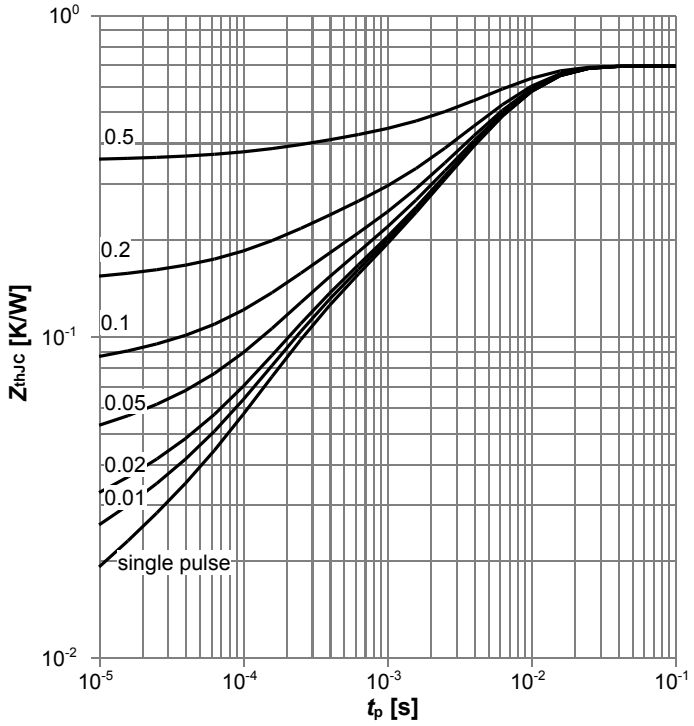
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 3: Safe operating area



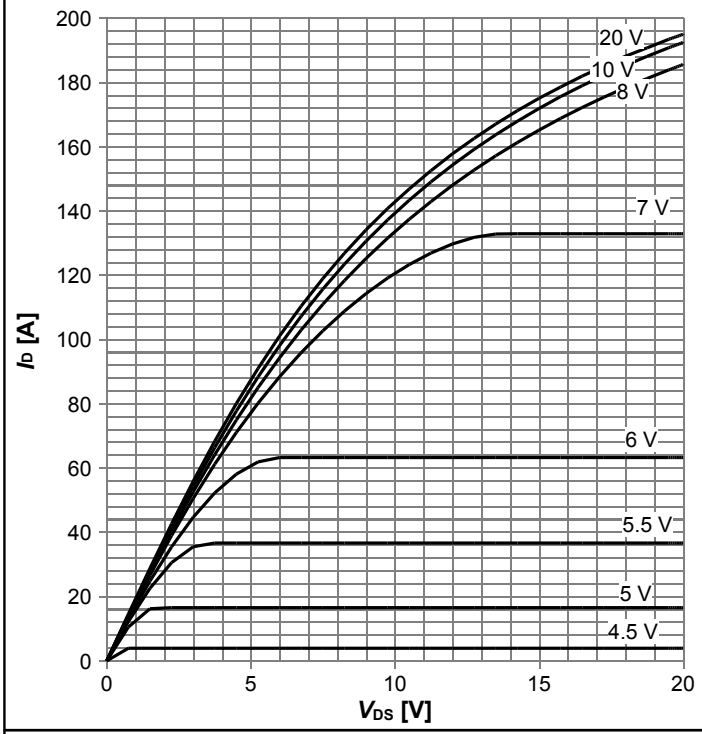
$I_D=f(V_{DS})$; $T_C=80$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



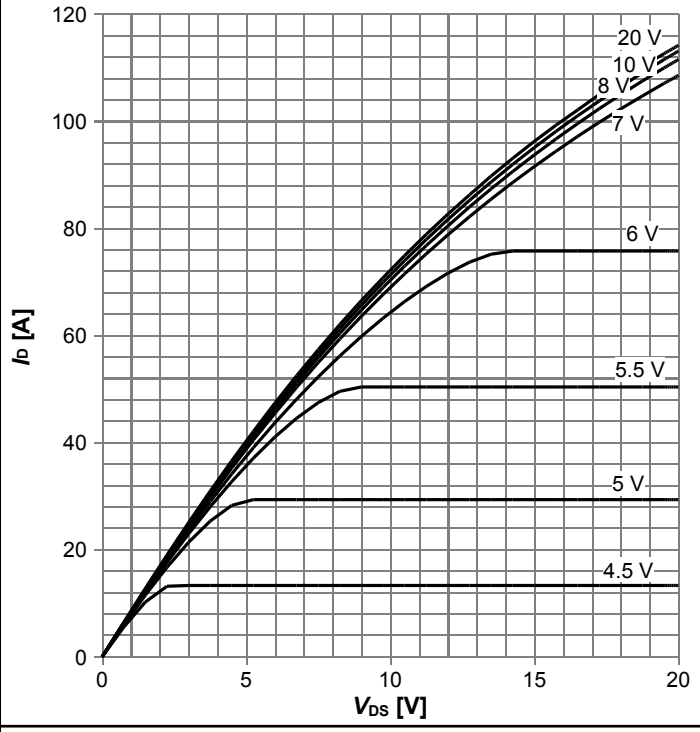
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



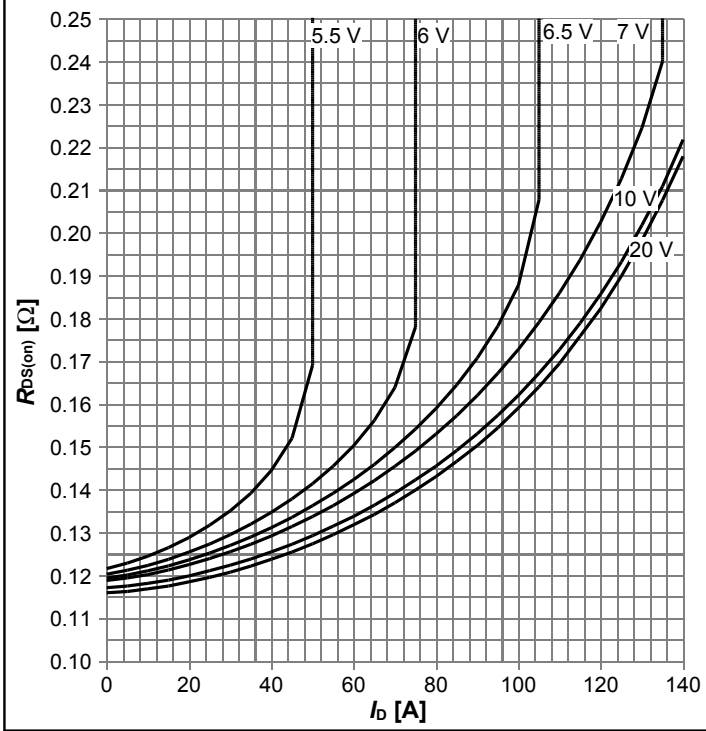
$I_D=f(V_{DS})$; $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



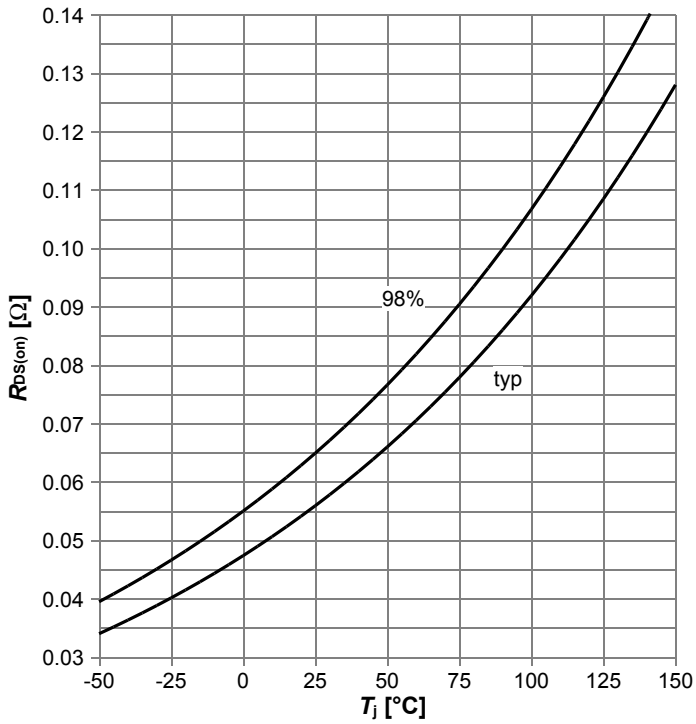
$I_D=f(V_{DS})$; $T_j=125$ °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



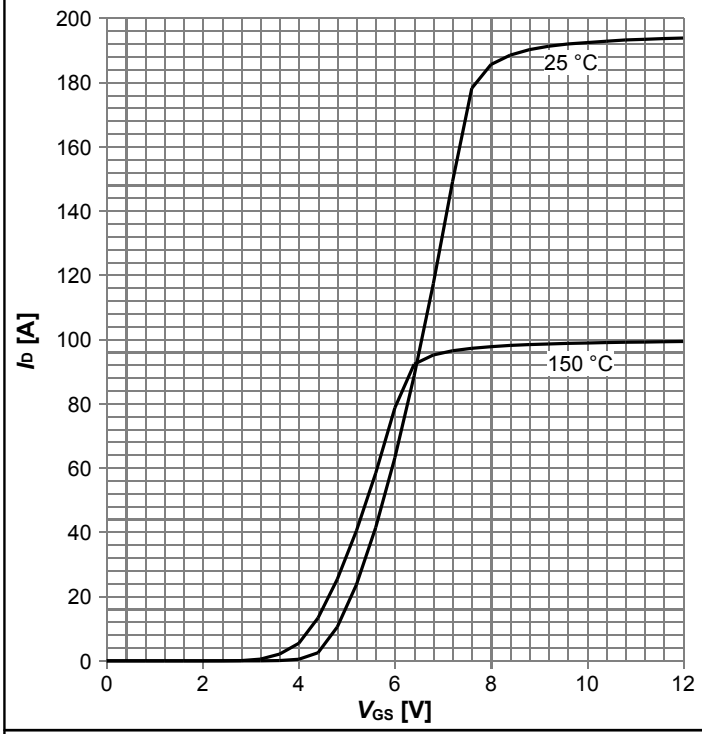
$R_{DS(on)}=f(I_D)$; $T_j=125$ °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



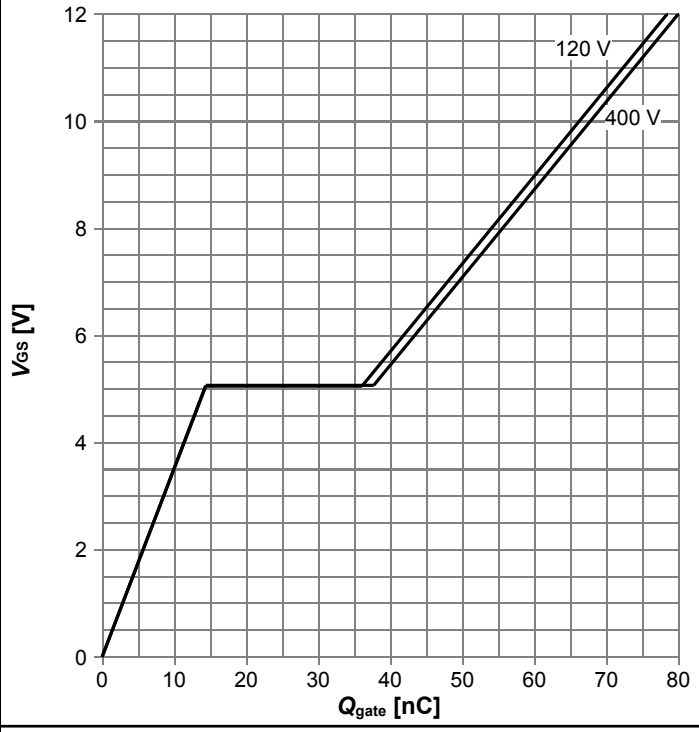
$R_{DS(on)}=f(T_j)$; $I_D=15.9$ A; $V_{GS}=10$ V

Diagram 9: Typ. transfer characteristics



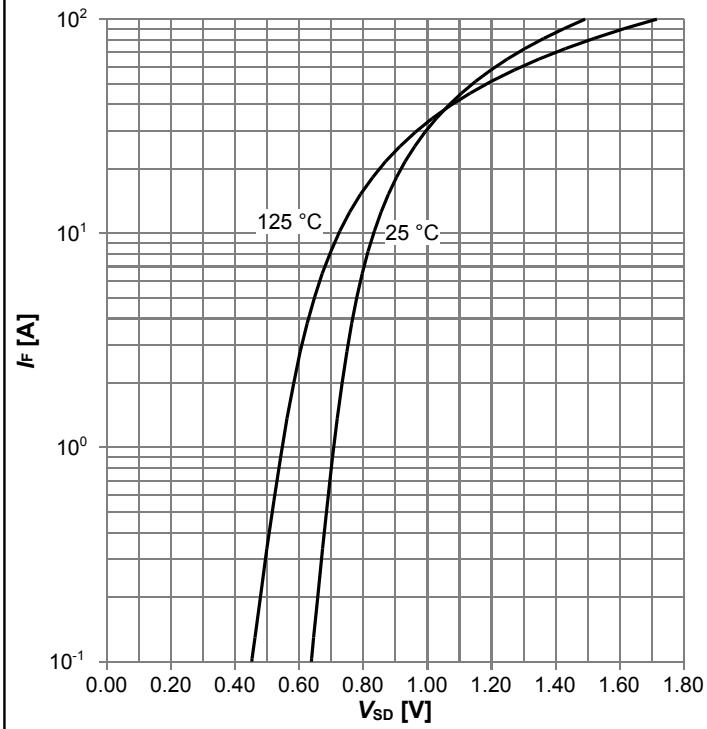
$I_D=f(V_{GS})$; V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



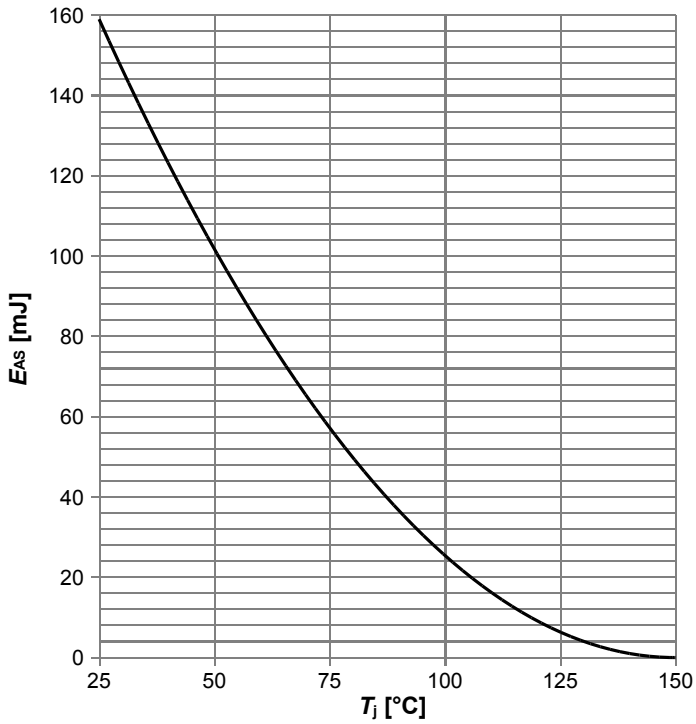
$V_{GS}=f(Q_{gate})$; I_D=15.9 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



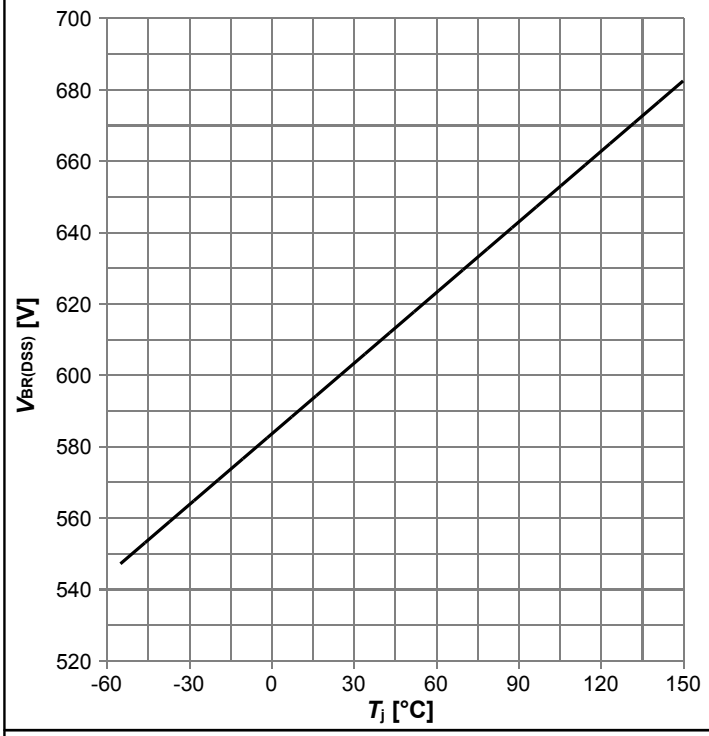
$I_F=f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



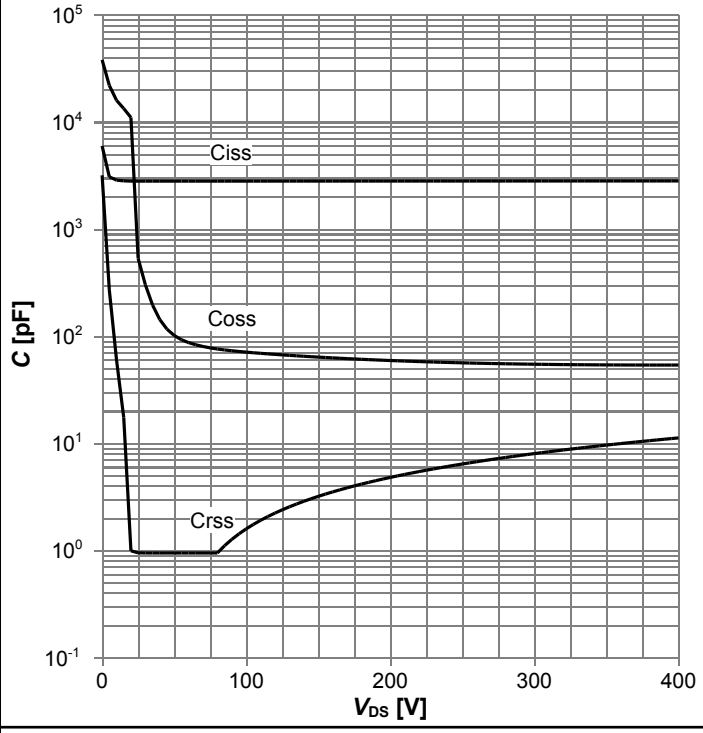
$E_{AS}=f(T_j)$; I_D=6.4 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



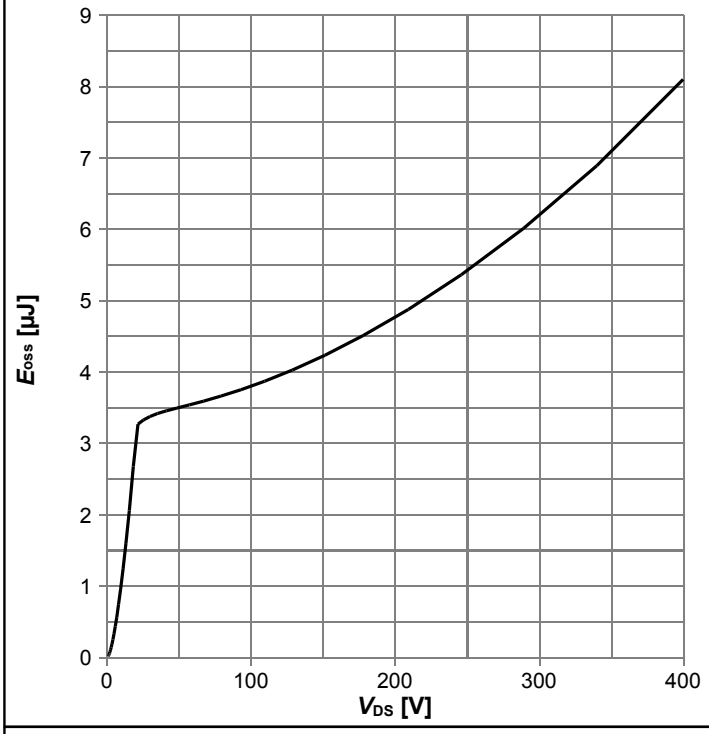
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

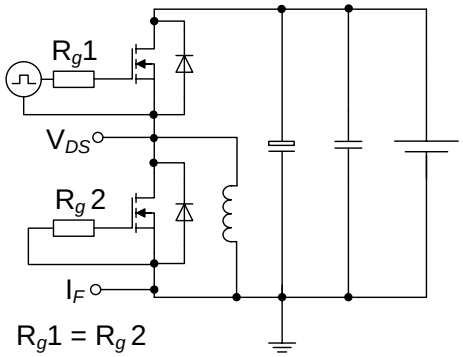
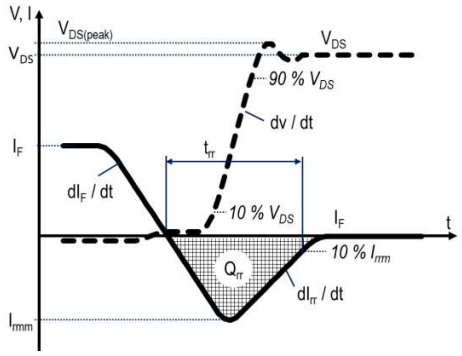
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 switching times (ss)

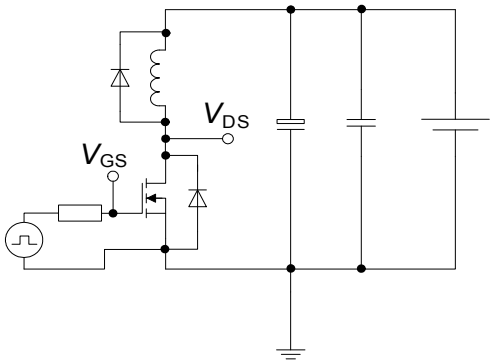
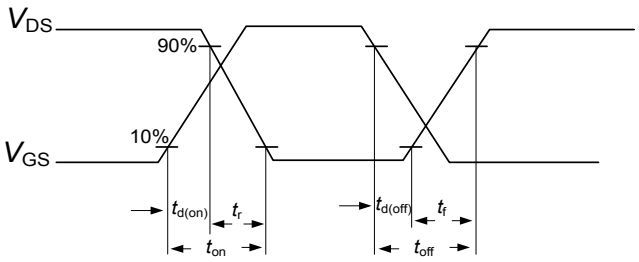
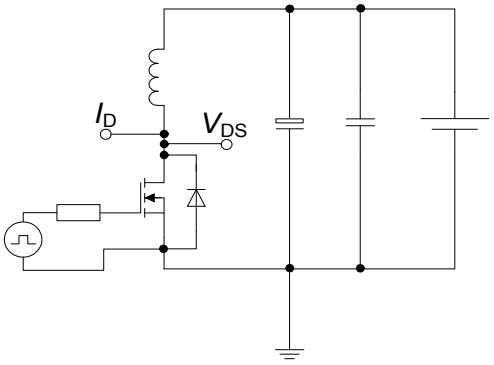
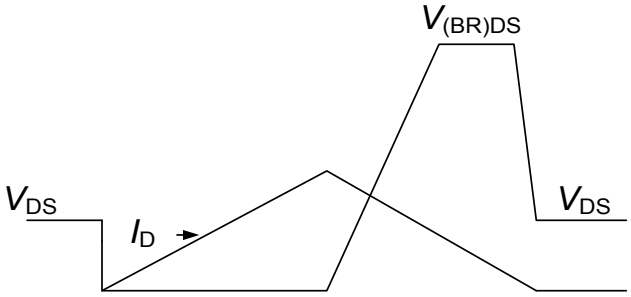
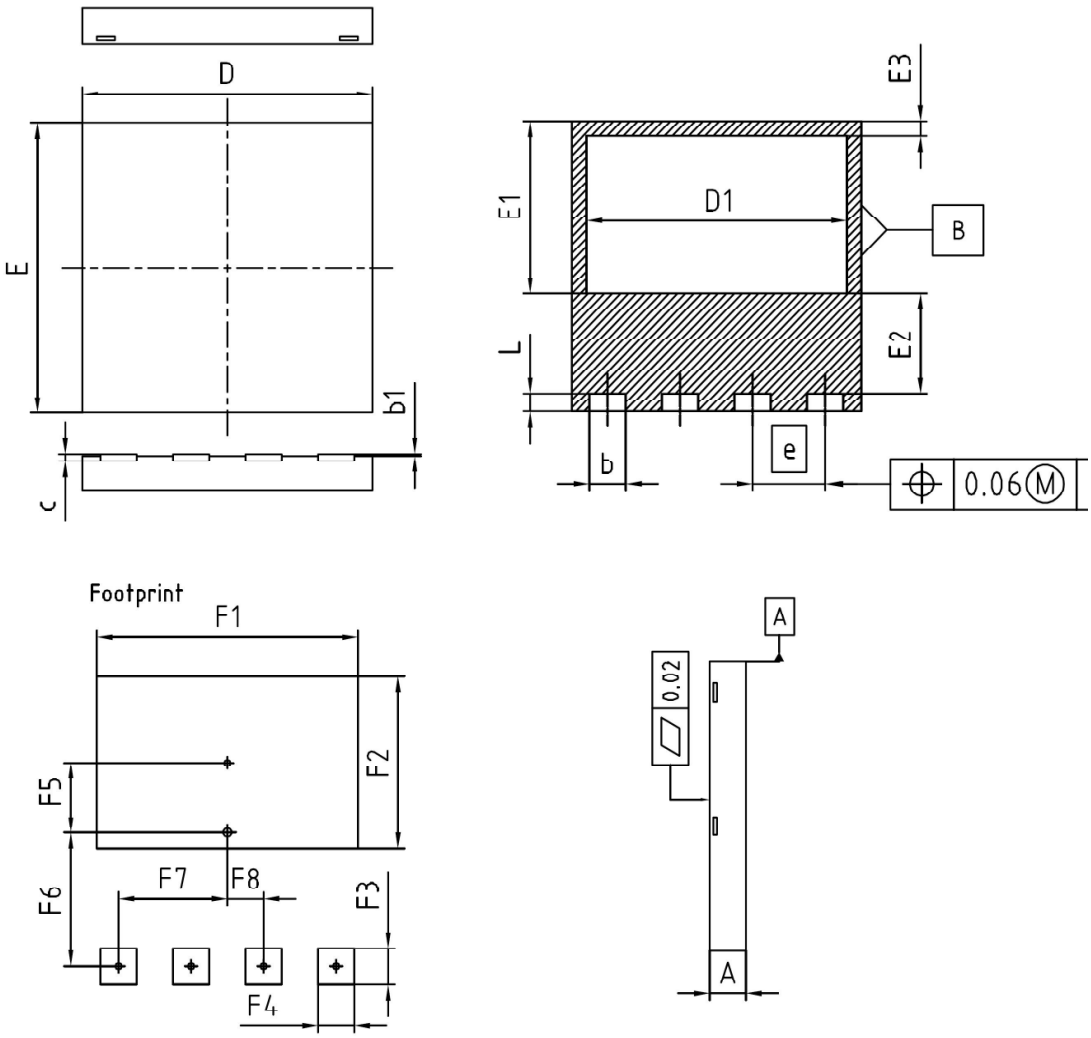
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.90	1.10	0.035	0.043
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
D1	7.10	7.30	0.280	0.287
E	7.90	8.10	0.311	0.319
E1	4.65	4.85	0.183	0.191
E2	2.65	2.85	0.104	0.112
E3	0.30	0.50	0.012	0.020
e	2.00 (BSC)		0.079 (BSC)	
L	0.40	0.60	0.016	0.024
N	4		4	
F1	7.20		0.283	
F2	4.75		0.187	
F3	1.00		0.039	
F4	1.00		0.039	
F5	1.43		0.056	
F6	4.20		0.165	
F7	3.00		0.118	
F8	1.00		0.039	

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SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-04-2010

REVISION
01

Figure 1 Outline PG-VSON-4, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS™ C7 Webpage:** www.infineon.com
- **IFX CoolMOS™ C7 application note:** www.infineon.com
- **IFX CoolMOS™ C7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R065C7

Revision: 2017-08-30, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2015-12-11	Release of final version
2.1	2017-08-30	Updated MSL

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