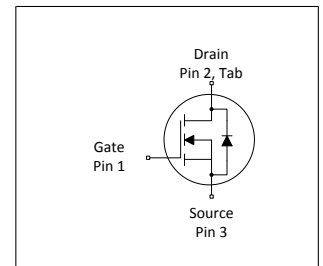
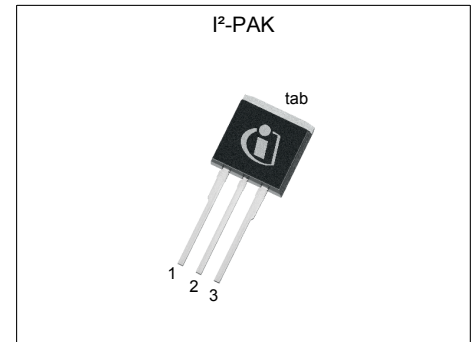


# MOSFET

## OptiMOS™ 3 Power-Transistor, 60 V

### Features

- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Very low on-resistance  $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	2.4	mΩ
$I_D$	169	A

Type / Ordering Code	Package	Marking	Related Links
IPI024N06N3 G	PG-TO 262-3	024N06N	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_A=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	169 130	A	$T_C=25\text{ °C}^{1)}$ $T_C=100\text{ °C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	676	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>3)</sup>	$E_{AS}$	-	-	634	mJ	$I_D=100\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	250	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.6	K/W	-
Thermal resistance, junction - ambient, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Thermal resistance, junction - ambient, 6 cm <sup>2</sup> cooling area <sup>4)</sup>	$R_{thJA}$	-	-	40	K/W	-

## 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4	V	$V_{DS}=V_{GS}$ , $I_D=196\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1 30	3 300	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	1	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.1	2.4	m $\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$
Gate resistance	$R_G$	-	1.3	-	$\Omega$	-
Transconductance	$g_{fs}$	92	184	-	S	$ V_{DS} >2 I_D /R_{DS(on)max}$ , $I_D=100\text{ A}$

<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC}=0.6\text{ K/W}$  the chip is able to carry 256A.

<sup>2)</sup> See Diagram 3 for more detailed information

<sup>3)</sup> See Diagram 13 for more detailed information

<sup>4)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	17000	23000	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	3700	4900	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	120	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	41	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_G=1.6\ \Omega$
Rise time	$t_r$	-	80	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_G=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	79	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_G=1.6\ \Omega$
Fall time	$t_f$	-	24	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$ , $R_G=1.6\ \Omega$

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	83	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	17	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	$Q_{sw}$	-	50	-	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	$Q_g$	-	206	275	nC	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=30\text{ V}$ , $I_D=100\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge	$Q_{oss}$	-	167	222	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	142	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	676	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.94	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=100\text{ A}$ , $T_J=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	67	-	ns	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	83	-	nC	$V_R=30\text{ V}$ , $I_F=100\text{ A}$ , $di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> See "Gate charge waveforms" for parameter definition

## 4 Electrical characteristics diagrams

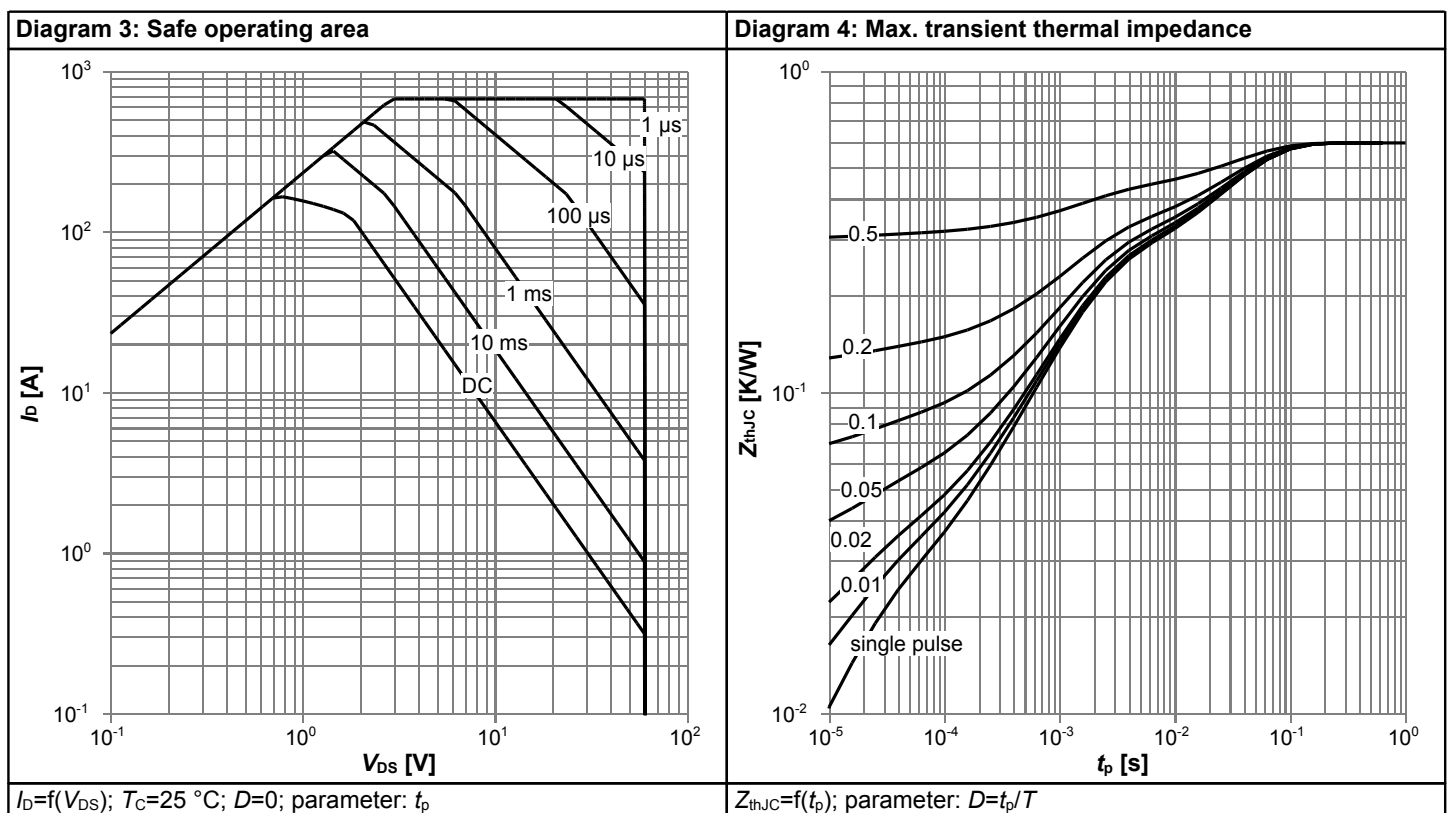
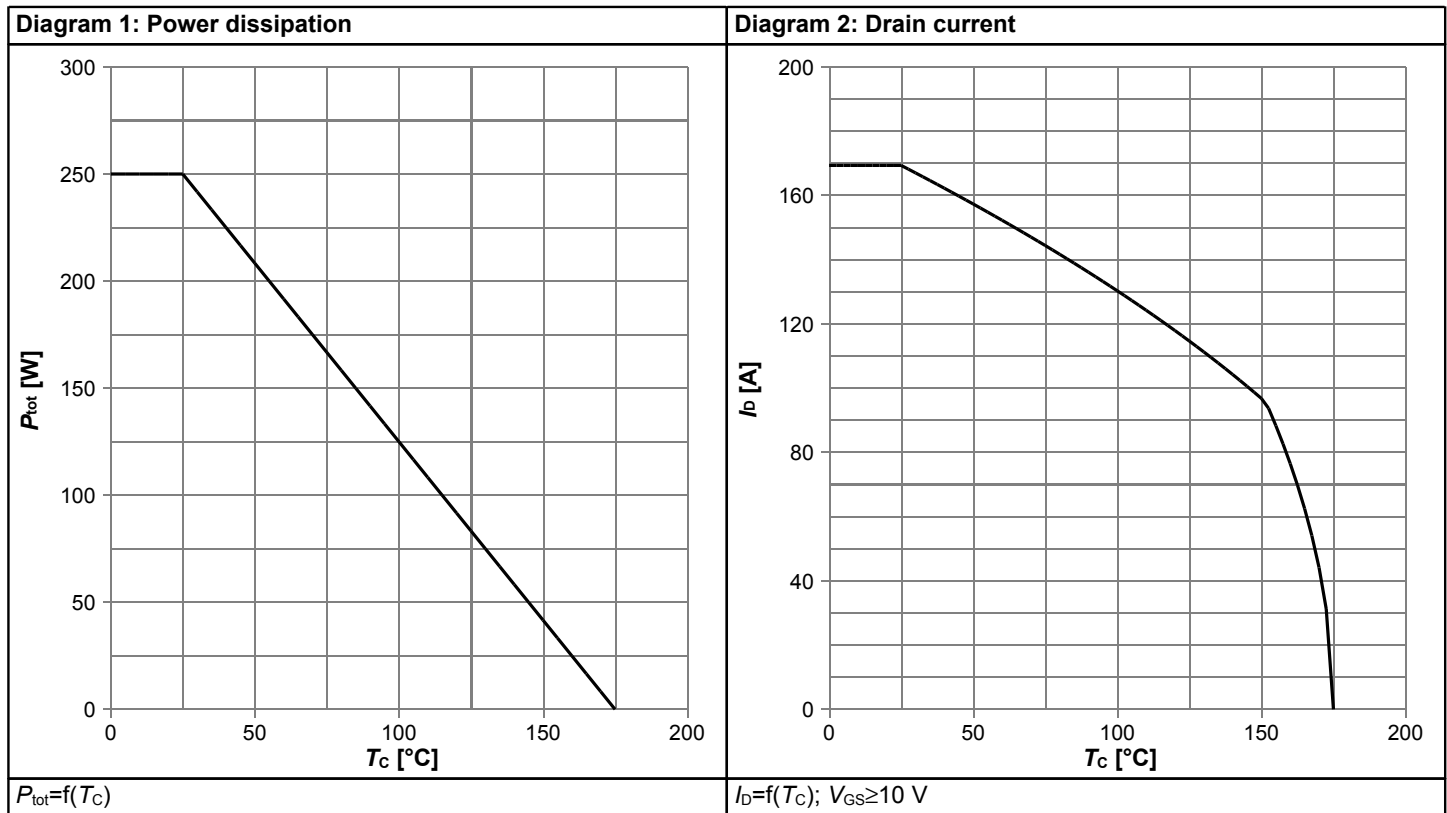
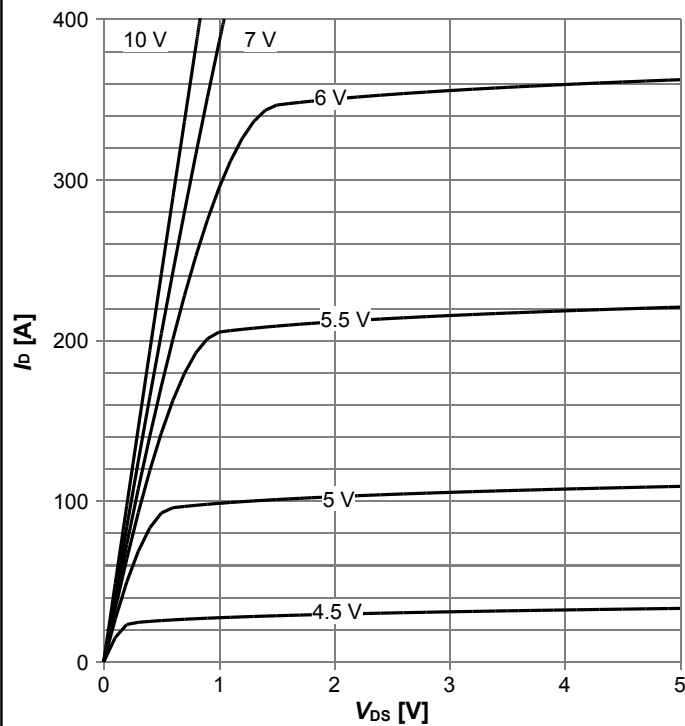
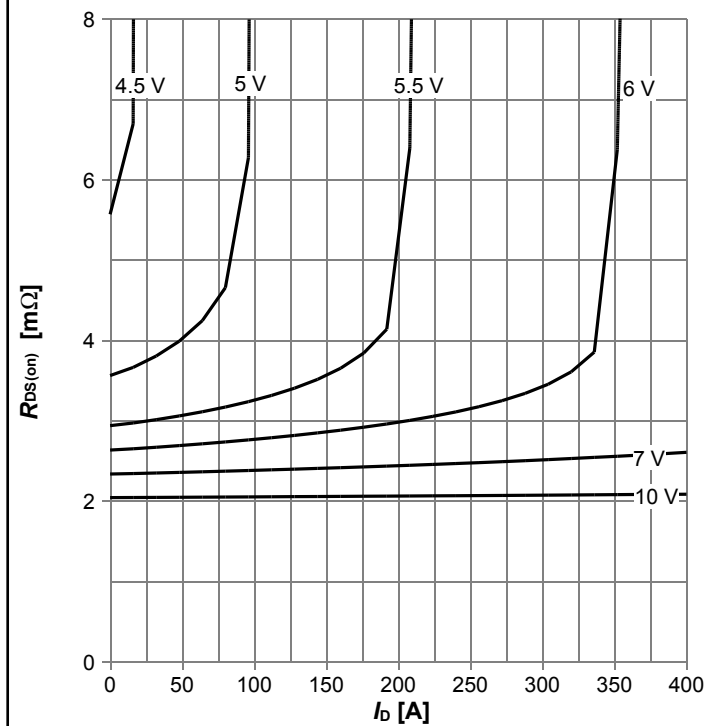


Diagram 5: Typ. output characteristics



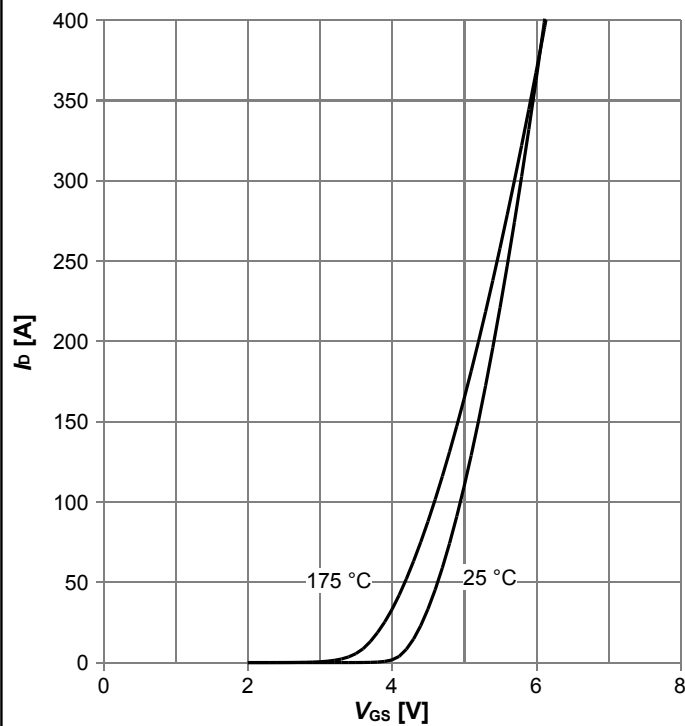
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



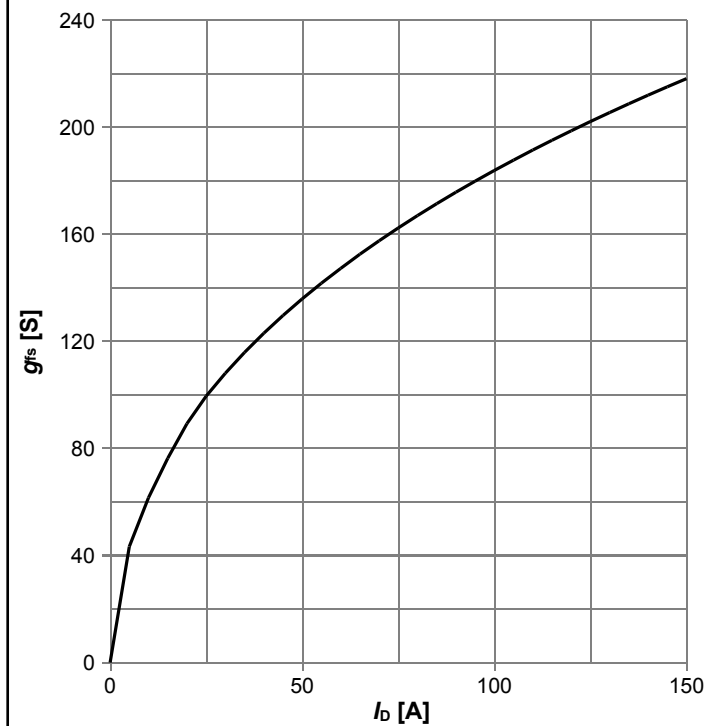
$R_{DS(on)} = f(I_D)$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



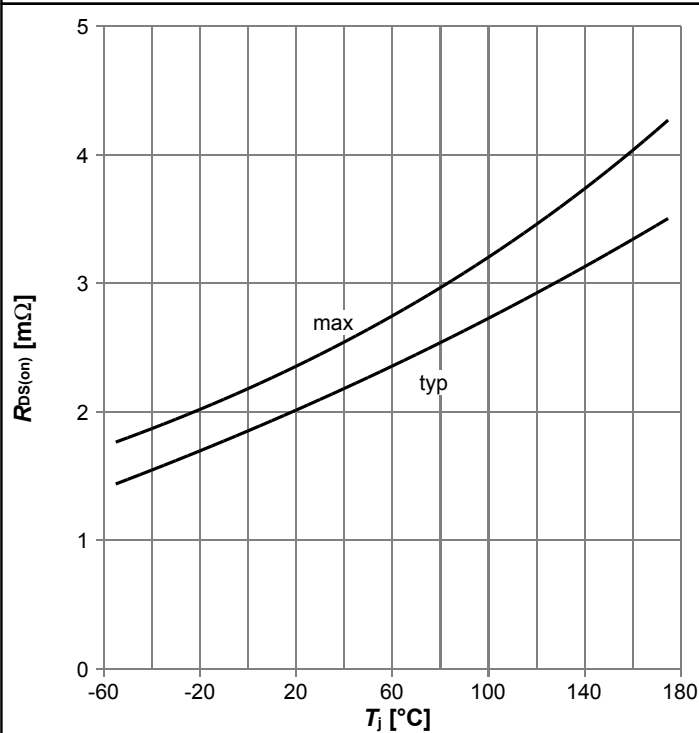
$I_D = f(V_{GS})$ ;  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. forward transconductance



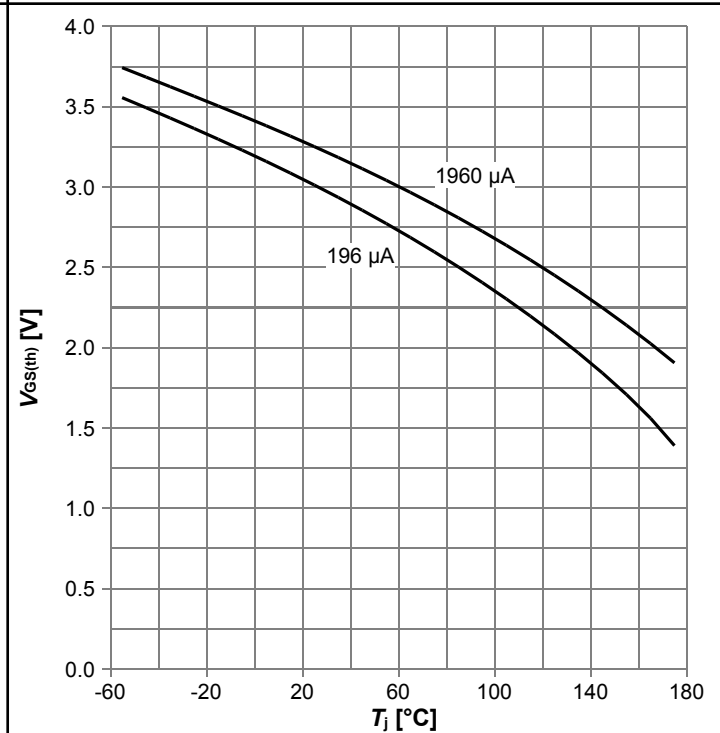
$g_{fs} = f(I_D)$ ;  $T_j = 25^\circ\text{C}$

Diagram 9: Drain-source on-state resistance



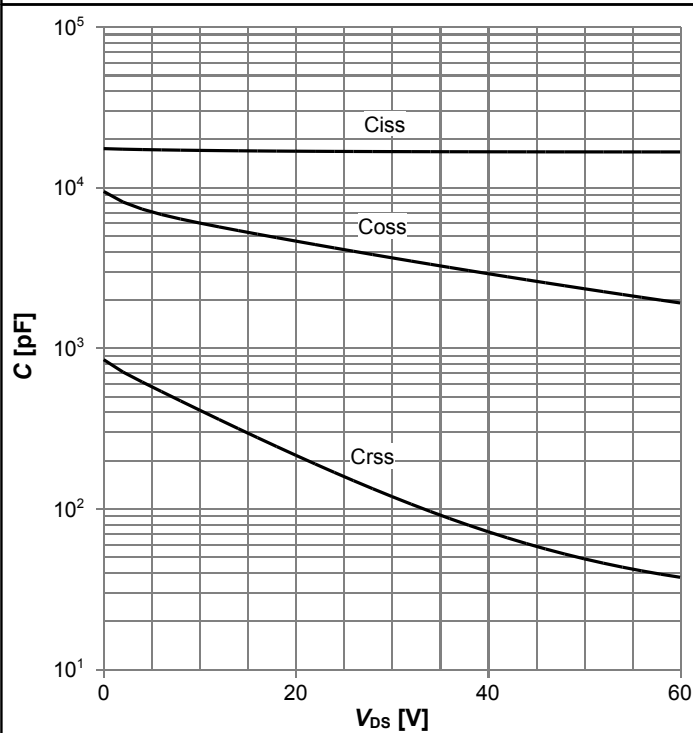
$R_{DS(on)} = f(T_j)$ ;  $I_D = 100 \text{ A}$ ;  $V_{GS} = 10 \text{ V}$

Diagram 10: Typ. gate threshold voltage



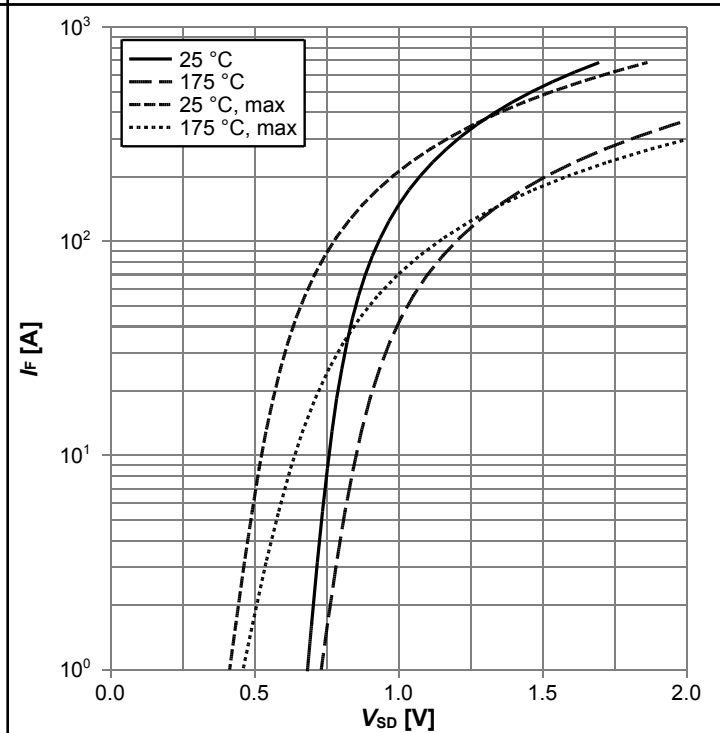
$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



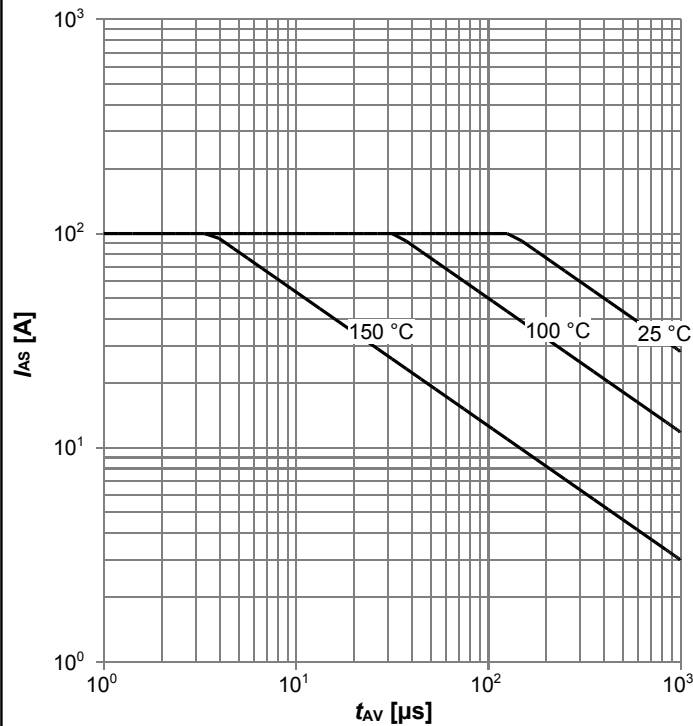
$C = f(V_{DS})$ ;  $V_{GS} = 0 \text{ V}$ ;  $f = 1 \text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



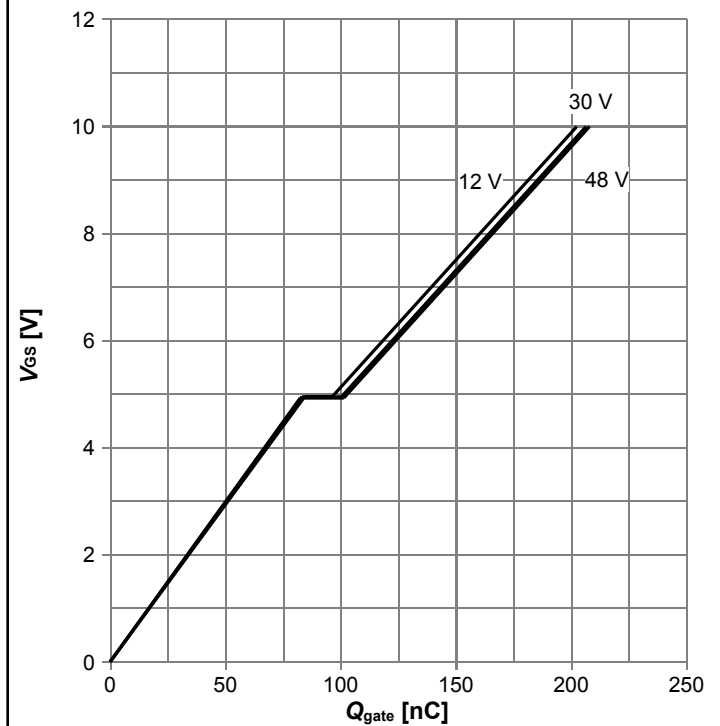
$I_F = f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



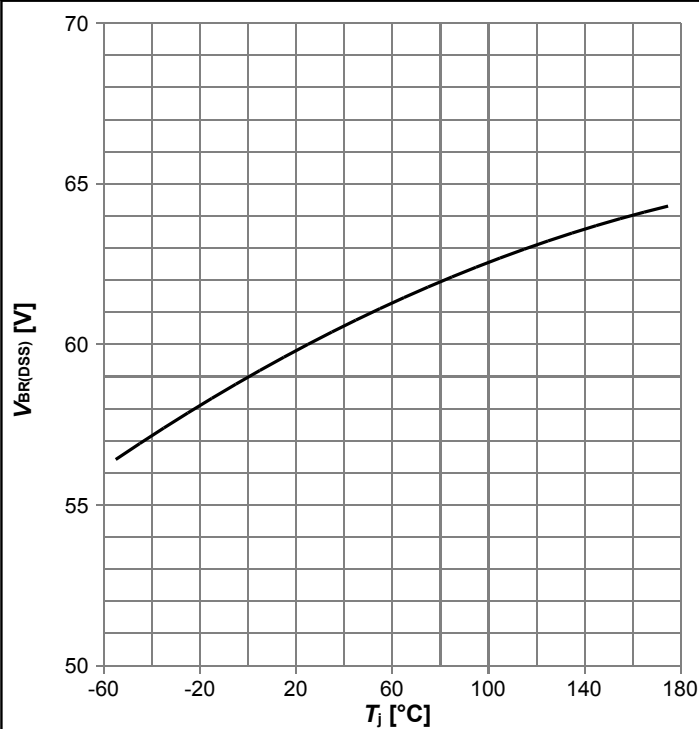
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



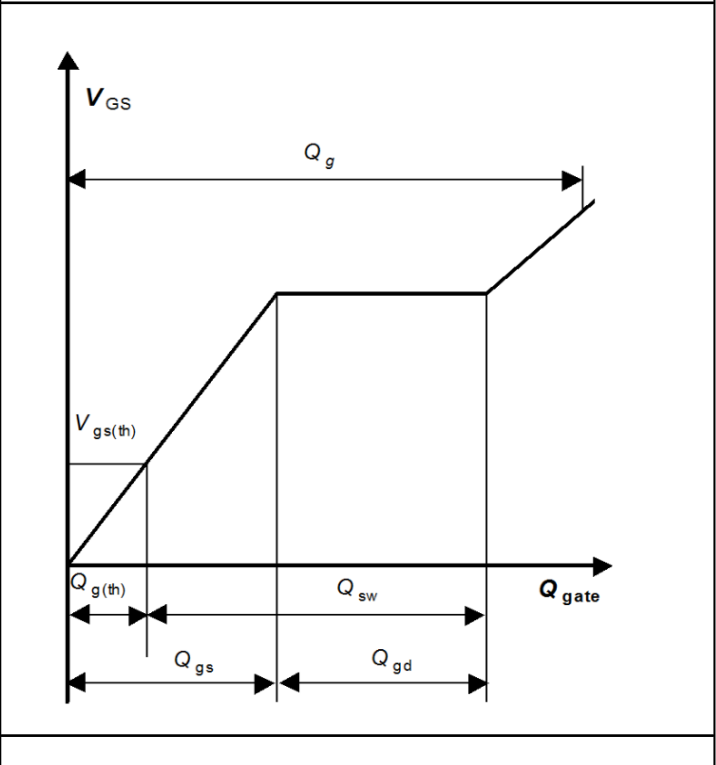
$V_{GS}=f(Q_{gate})$ ;  $I_D=100\text{ A}$  pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



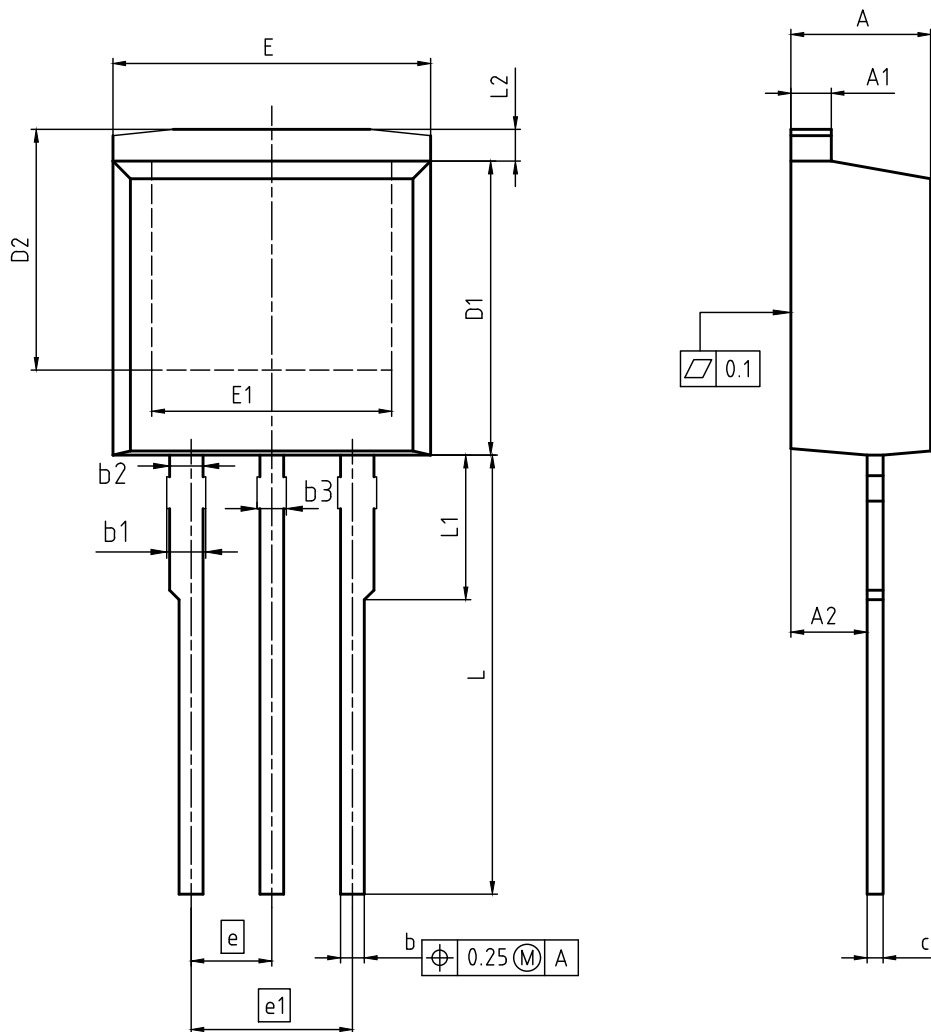
$V_{BR(DSS)}=f(T_j)$ ;  $I_D=1\text{ mA}$

Diagram Gate charge waveforms





## 5 Package Outlines



DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.57
A1	1.17	1.40
A2	2.15	2.72
b	0.65	0.86
b1	0.95	1.40
b2	0.95	1.15
b3	0.65	1.15
c	0.33	0.60
D1	8.51	9.45
D2	6.90	-
E	9.70	10.36
E1	6.50	8.60
e	2.54	
e1	5.08	
N	3	
L	13.00	14.00
L1	-	4.80
L2	-	1.73

<b>DOCUMENT NO.</b> Z8B00003325
<b>REVISION</b> 05
<b>SCALE</b> 5:1 0 1 2 3 4 5mm
<b>EUROPEAN PROJECTION</b> 
<b>ISSUE DATE</b> 29.11.2018

Figure 1 Outline PG-TO 262-3, dimensions in mm

## Revision History

IPI024N06N3 G

**Revision: 2019-02-07, Rev. 2.4**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.3	2017-08-01	Update product current
2.4	2019-02-07	Update package outline

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