

MOSFET

StrongIRFET™2 Power-Transistor

Features

- Optimized for wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

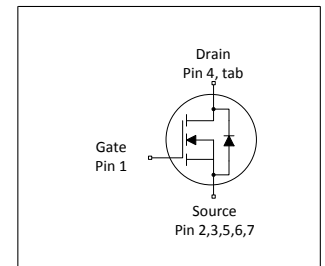
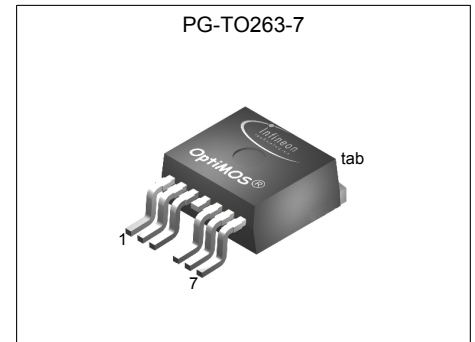


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.2	m Ω
I_D	282	A
Q_{oss}	153	nC
$Q_G (0V..10V)$	155	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPF012N06NF2S	PG-TO263-7	012N06NS	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	282 216 41	A	$V_{GS}=10V, T_C=25\text{ °C}$ $V_{GS}=10V, T_C=100\text{ °C}$ $V_{GS}=10V, T_A=25\text{ °C}, R_{THJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1128	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	727	mJ	$I_D=100A, R_{GS}=25\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	250 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}, R_{THJA}=40\text{ °C/W}^2)$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.6	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics
 at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$, $I_D=186\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.5 10	1 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.1 1.4	1.2 1.9	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	2.7	-	Ω	-
Transconductance ¹⁾	g_{fs}	130	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	10500	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	2190	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	75	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	27	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	34	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	65	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	27	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	46	-	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	29	-	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	28	-	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	45	-	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	155	233	nC	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=30\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	144	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	153	-	nC	$V_{DS}=30\text{ V}$, $V_{GS}=0\text{ V}$

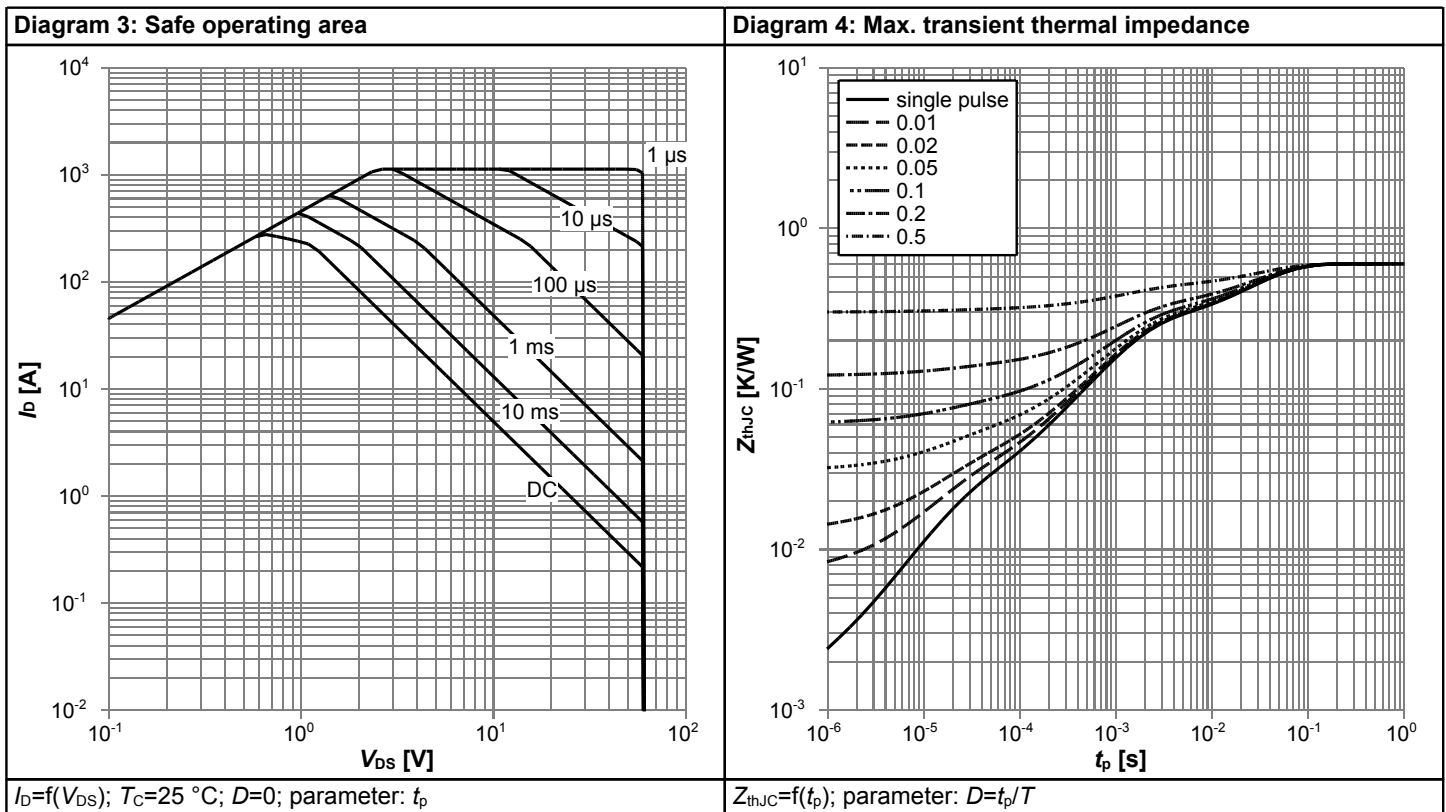
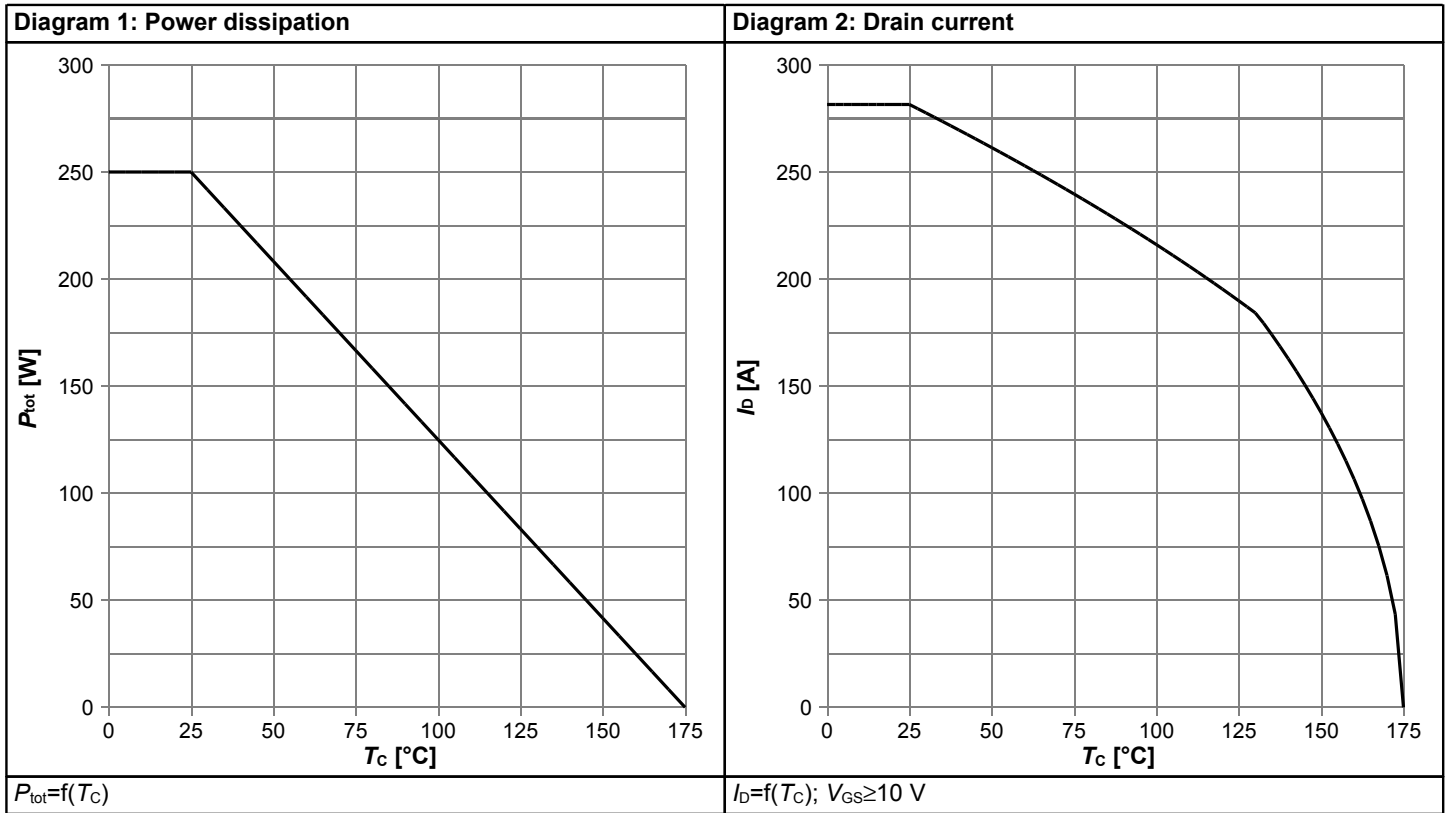
¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	204	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1128	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.86	1	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	38	-	ns	$V_R=30\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	201	-	nC	$V_R=30\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$

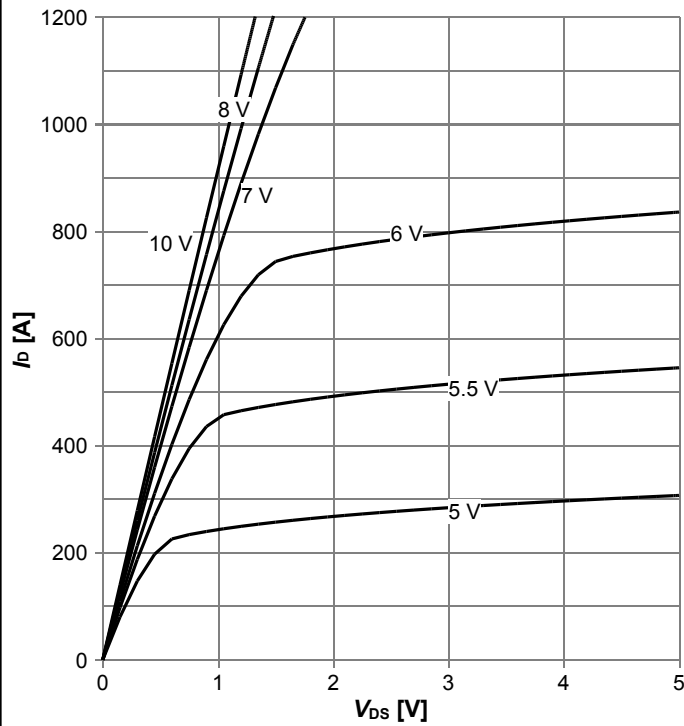
4 Electrical characteristics diagrams



StrongIRFET™2 Power-Transistor

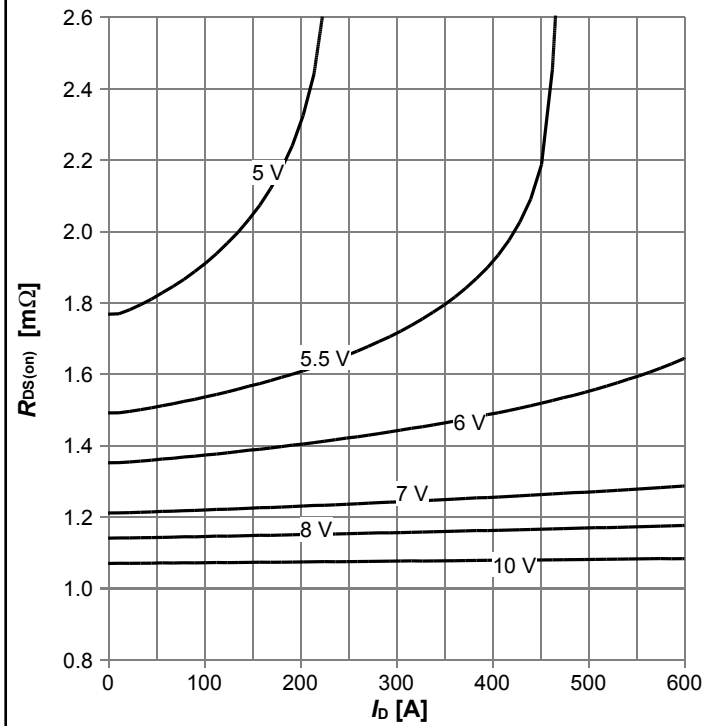
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Diagram 5: Typ. output characteristics



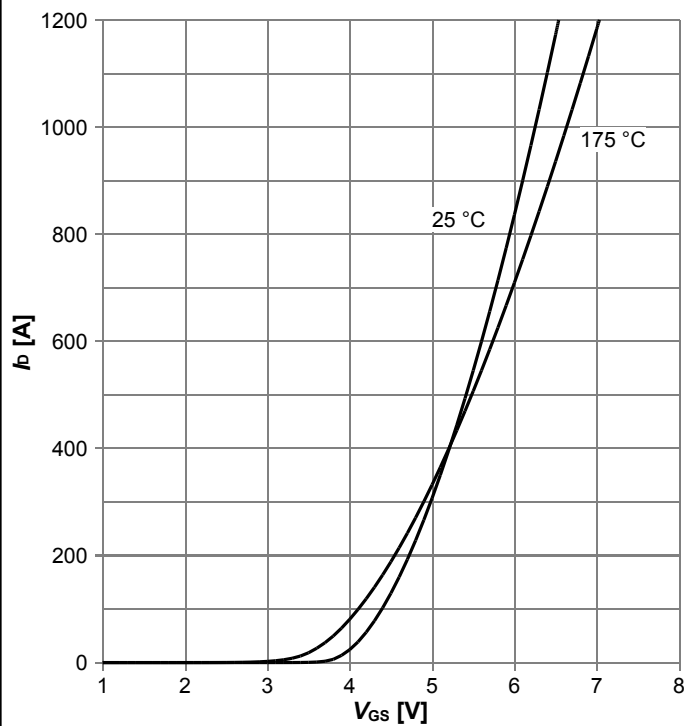
$I_D=f(V_{DS})$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



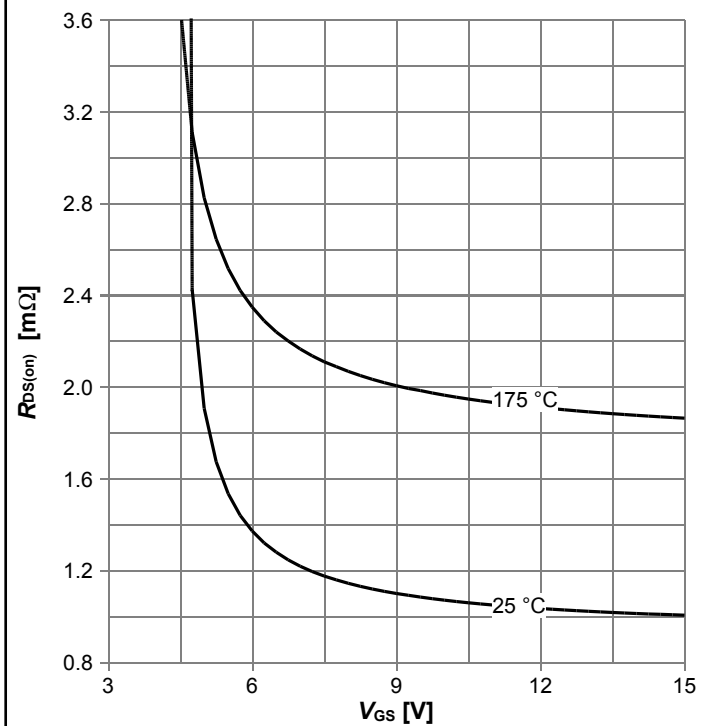
$R_{DS(on)}=f(I_D)$, $T_j=25\text{ }^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



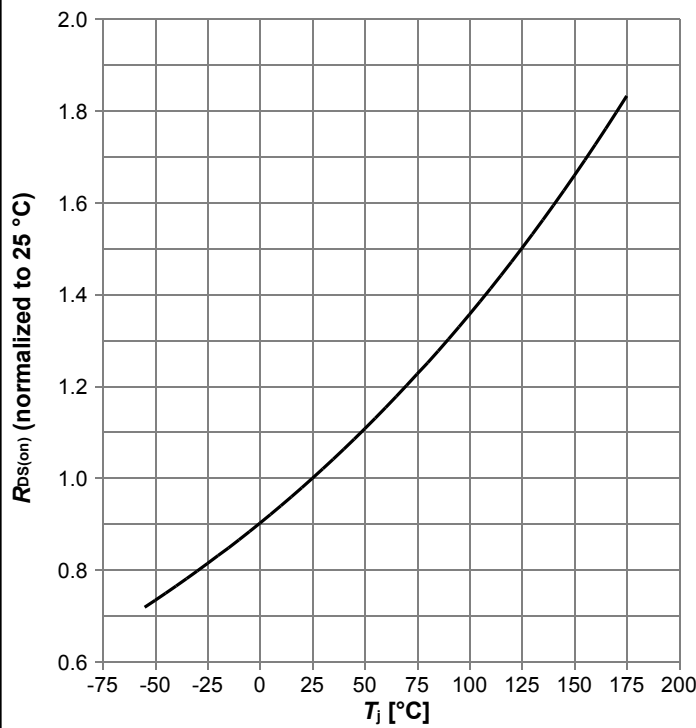
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



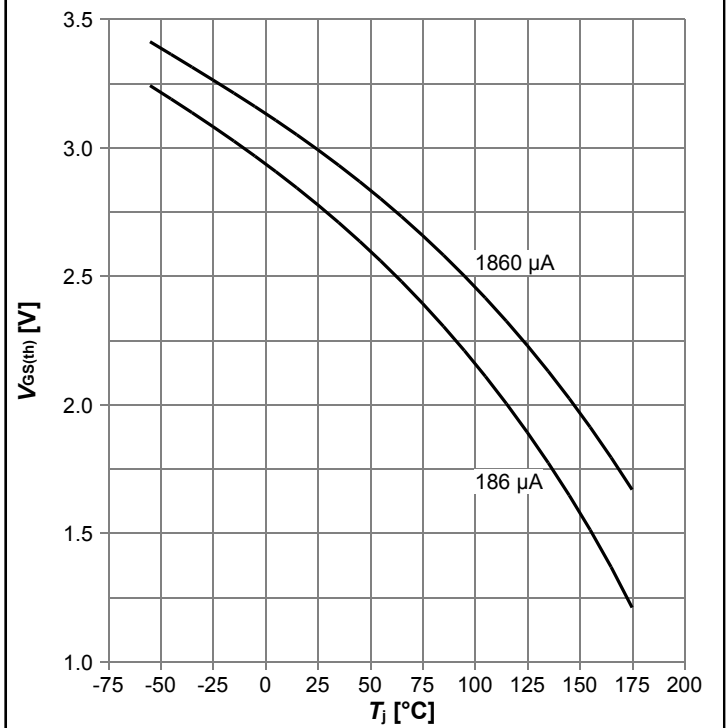
$R_{DS(on)}=f(V_{GS})$, $I_D=100\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



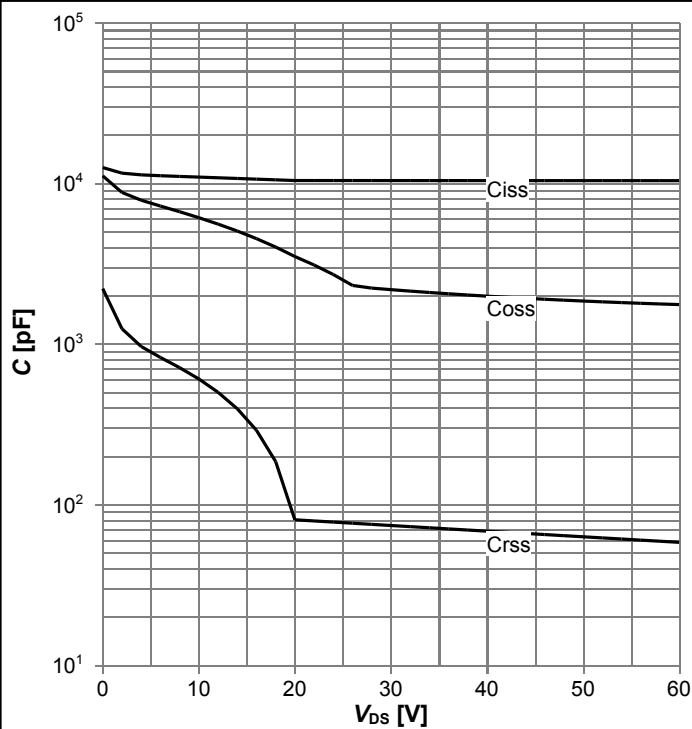
$R_{DS(on)}=f(T_j)$, $I_D=100$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



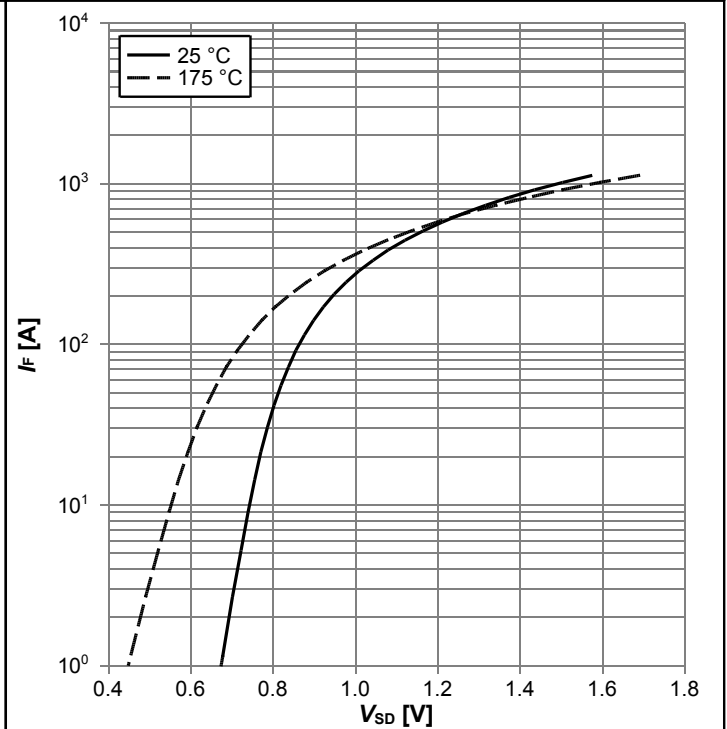
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



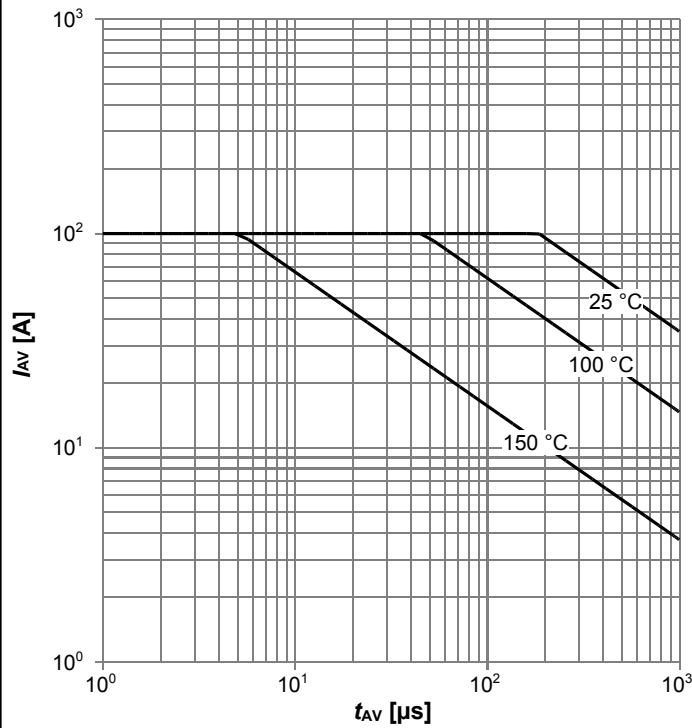
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode



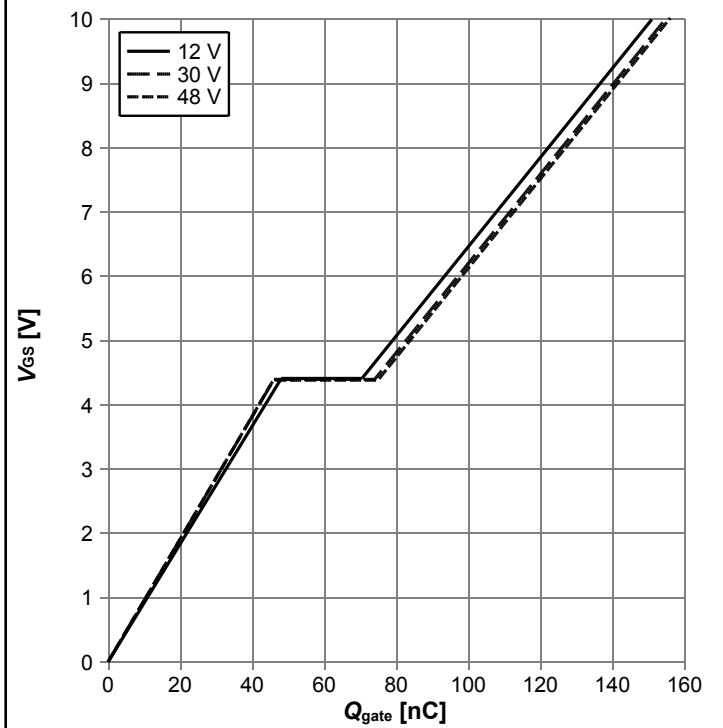
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



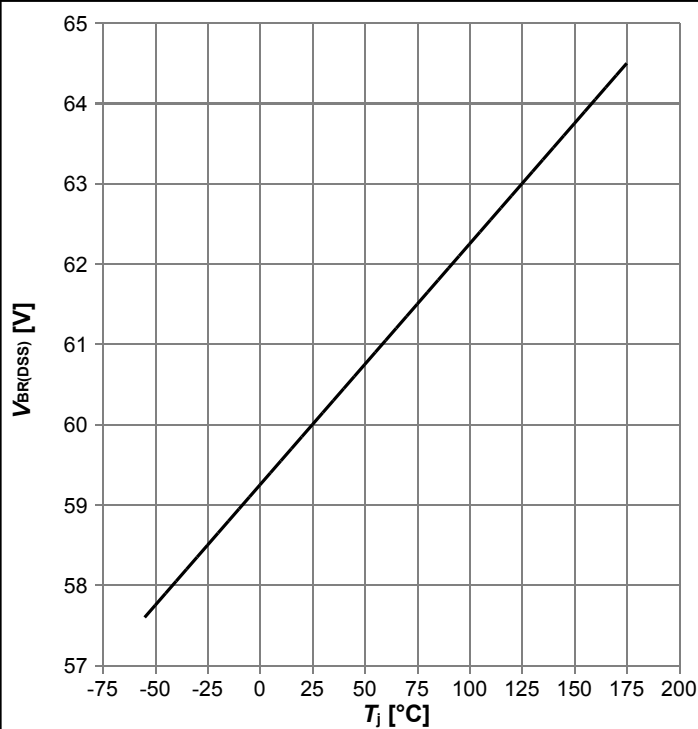
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}), I_D=100 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

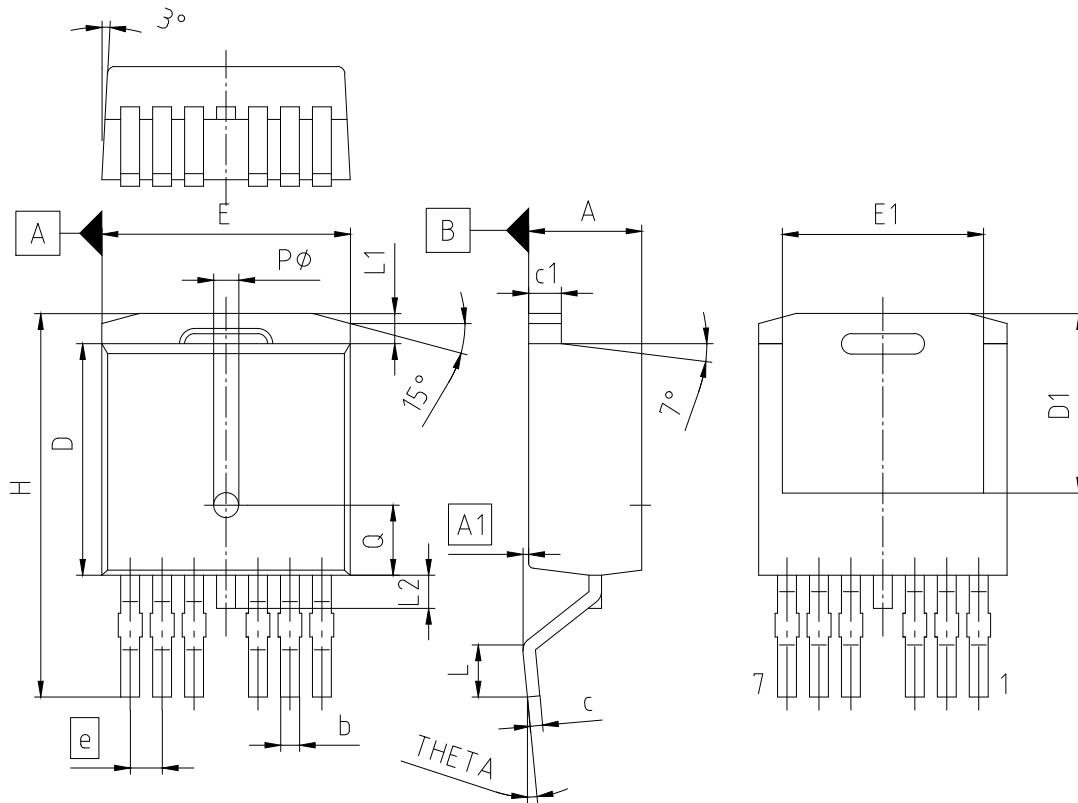


$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER:		PG-TO263-7-U02	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	4.30	4.70	
A1	0.00	0.25	
b	0.65	0.85	
c	0.45	0.60	
c1	1.25	1.40	
D	9.00	9.40	
D1	6.86	7.42	
E	9.68	10.08	
E1	7.70	8.30	
e	1.27		
N	7		
H	14.61	15.88	
L	1.78	2.79	
L1	0.00	1.60	
L2	0.00	1.78	
THETA	0° - 8°		
PØ	0.90	1.10	
Q	2.78		

Figure 1 Outline PG-TO263-7, dimensions in mm

Revision History

IPF012N06NF2S

Revision: 2022-10-17, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-10-17	Release of final version

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Published by

Infineon Technologies AG

81726 München, Germany

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