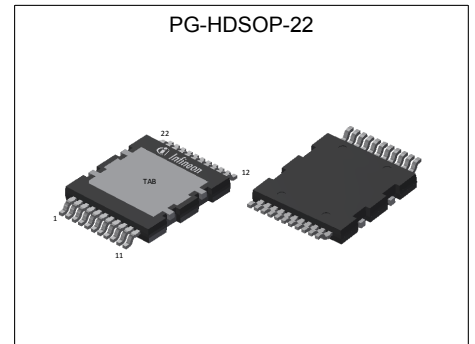


# MOSFET

## 650V CoolMOS™ CFD7 SJ Power Device

The latest 650 V CoolMOS™ CFD7 extends the voltage class offering of the CFD7 family and is a successor to the 650 V CoolMOS™ CFD2. Resulting from improved switching performance and excellent thermal behavior, 650 V CoolMOS™ CFD7 offers highest efficiency in resonant switching topologies, such as LLC and phase-shift-full-bridge (ZVS). As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions.



### Features

- Ultra-fast body diode
- 650V break down voltage
- Best-in-class  $R_{DS(on)}$
- Reduced switching losses
- Low  $R_{DS(on)}$  dependency over temperature

### Benefits

- Excellent hard commutation ruggedness
- Extra safety margin for designs with increased bus voltage
- Enabling increased power density solutions
- Outstanding light load efficiency in industrial SMPS applications
- Improved full load efficiency in industrial SMPS applications

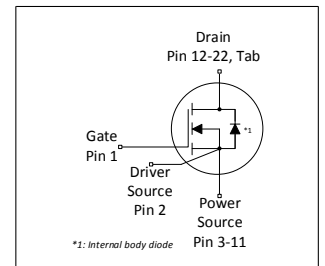
### Potential applications

Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging, Solar

### Product validation

Fully qualified according to JEDEC for Industrial Applications

*Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.*



RoHS

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	29	mΩ
$Q_{g,typ}$	139	nC
$I_{D,pulse}$	304	A
$E_{oss} @ 400V$	20.9	μJ
Body diode $di_F/dt$	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPDQ65R029CFD7	PG-HDSOP-22	65R029F7	see Appendix A

## Table of Contents

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	85 54	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	304	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	358	mJ	$I_D=7.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche energy, repetitive	$E_{AR}$	-	-	1.79	mJ	$I_D=7.3\text{A}$ ; $V_{DD}=50\text{V}$ ; see table 10
Avalanche current, single pulse	$I_{AS}$	-	-	7.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	463	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current <sup>1)</sup>	$I_S$	-	-	85	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	304	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 35.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di <sub>F</sub> /dt	-	-	1300	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}$ , $I_{SD}\leq 35.8\text{A}$ , $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}$ , $T_C=25^\circ\text{C}$ , $t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_\theta$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.27	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	45	55	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area. Tap exposed to air. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	$T_{sold}$	-	-	260	°C	reflow MSL1

### 3 Electrical characteristics

at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}, I_D=1.79mA$
Zero gate voltage drain current <sup>1)</sup>	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS}=650V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=650V, V_{GS}=0V, T_j=125^\circ C$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.024	0.029	$\Omega$	$V_{GS}=10V, I_D=35.8A, T_j=25^\circ C$ $V_{GS}=10V, I_D=35.8A, T_j=150^\circ C$
Gate resistance	$R_G$	-	3.8	-	$\Omega$	$f=1MHz, \text{open drain}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	7149	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Output capacitance	$C_{oss}$	-	106	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250kHz$
Effective output capacitance, energy related <sup>2)</sup>	$C_{o(er)}$	-	261	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>3)</sup>	$C_{o(tr)}$	-	2774	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	54	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega; \text{see table 9}$
Rise time	$t_r$	-	13	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega; \text{see table 9}$
Turn-off delay time	$t_{d(off)}$	-	159	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega; \text{see table 9}$
Fall time	$t_f$	-	3	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=35.8A,$ $R_G=1.8\Omega; \text{see table 9}$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	41	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate to drain charge	$Q_{gd}$	-	41	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate charge total	$Q_g$	-	139	-	nC	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V, I_D=35.8A, V_{GS}=0 \text{ to } 10V$

<sup>1)</sup> Maximum specification is defined by calculated six sigma upper confidence bound

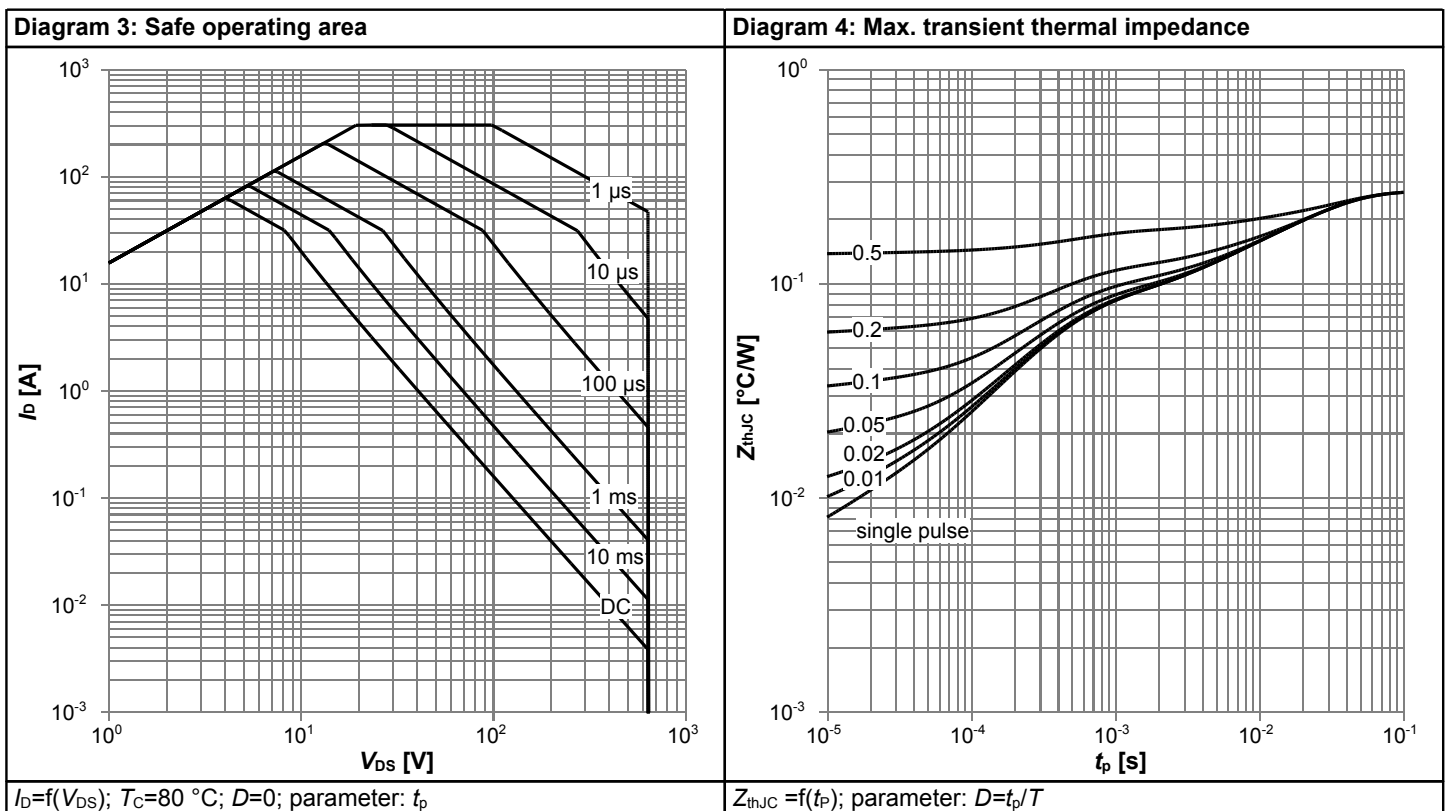
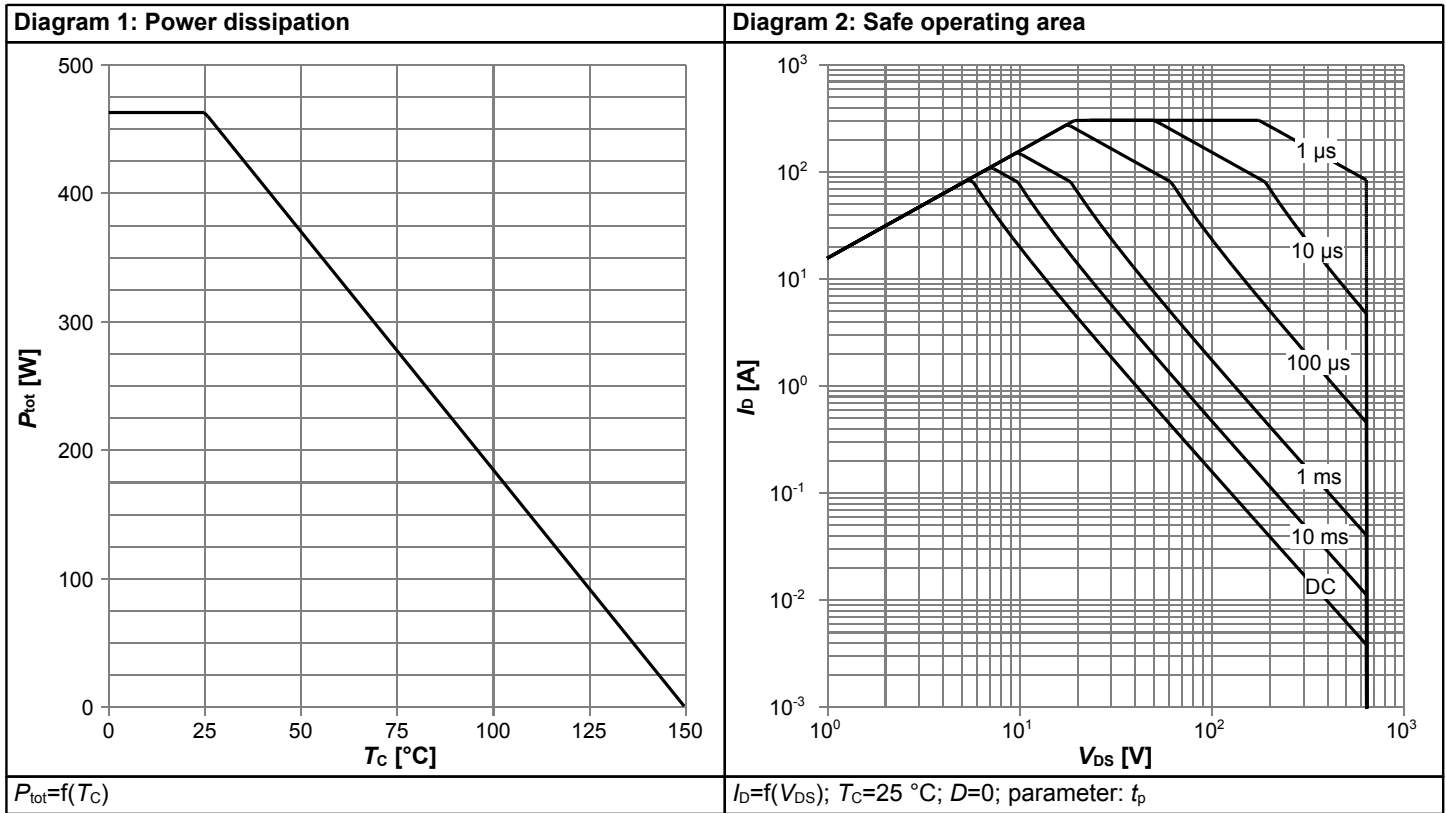
<sup>2)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>3)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

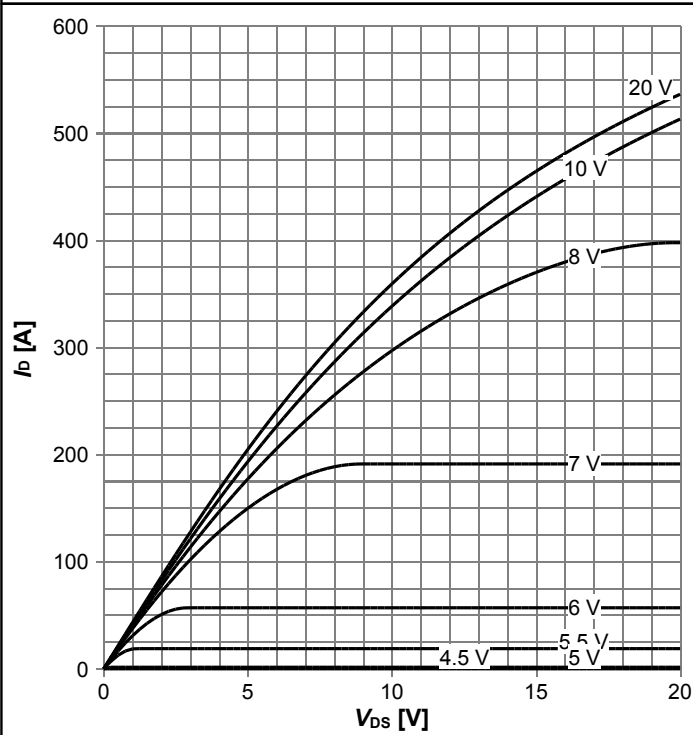
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	1.0	-	V	$V_{GS}=0V, I_F=35.8A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	208	312	ns	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8
Reverse recovery charge	$Q_{rr}$	-	1.6	3.2	$\mu C$	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8
Peak reverse recovery current	$I_{rrm}$	-	13.1	-	A	$V_R=400V, I_F=35.8A, di_F/dt=100A/\mu s$ ; see table 8

## 4 Electrical characteristics diagrams

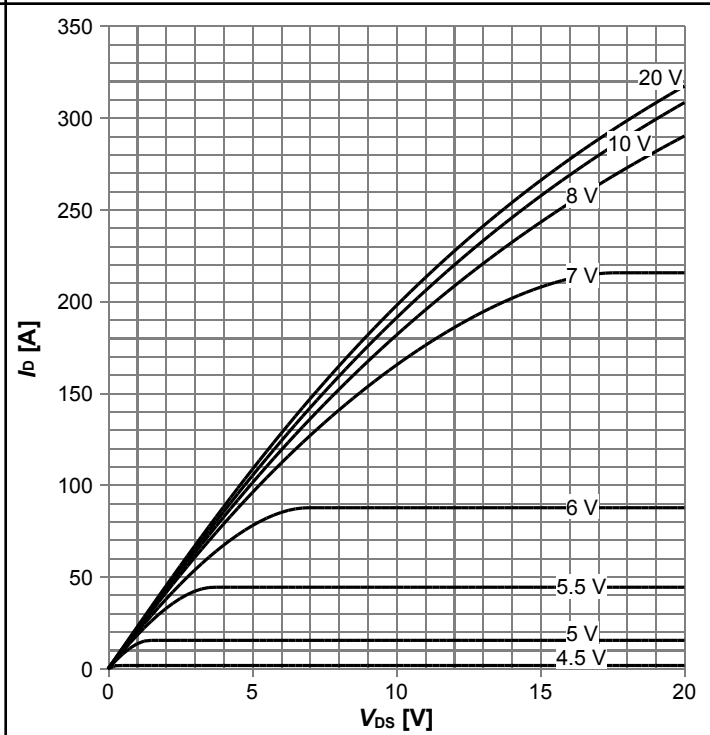


**Diagram 5: Typ. output characteristics**



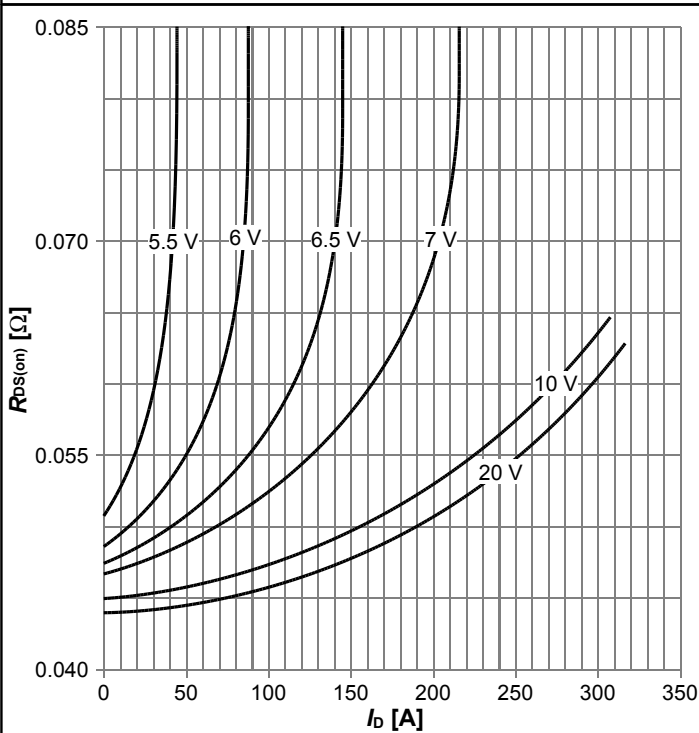
$I_D = f(V_{DS})$ ;  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



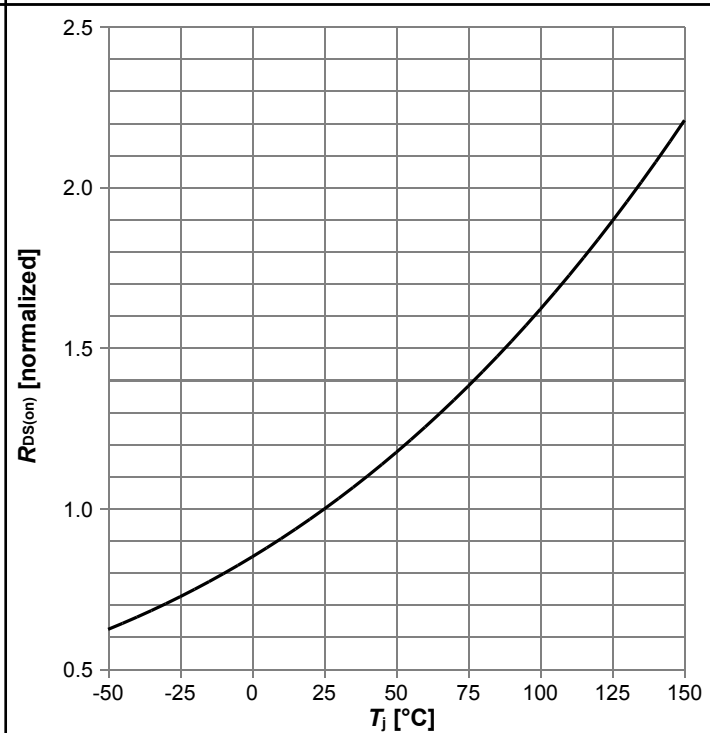
$I_D = f(V_{DS})$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)} = f(I_D)$ ;  $T_j = 125^\circ\text{C}$ ; parameter:  $V_{GS}$

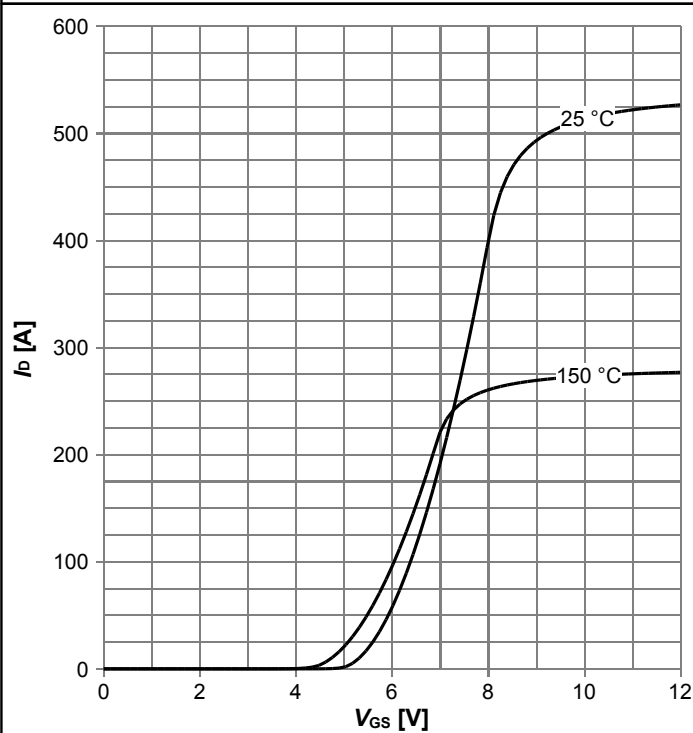
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)} = f(T_j)$ ;  $I_D = 35.8\text{ A}$ ;  $V_{GS} = 10\text{ V}$

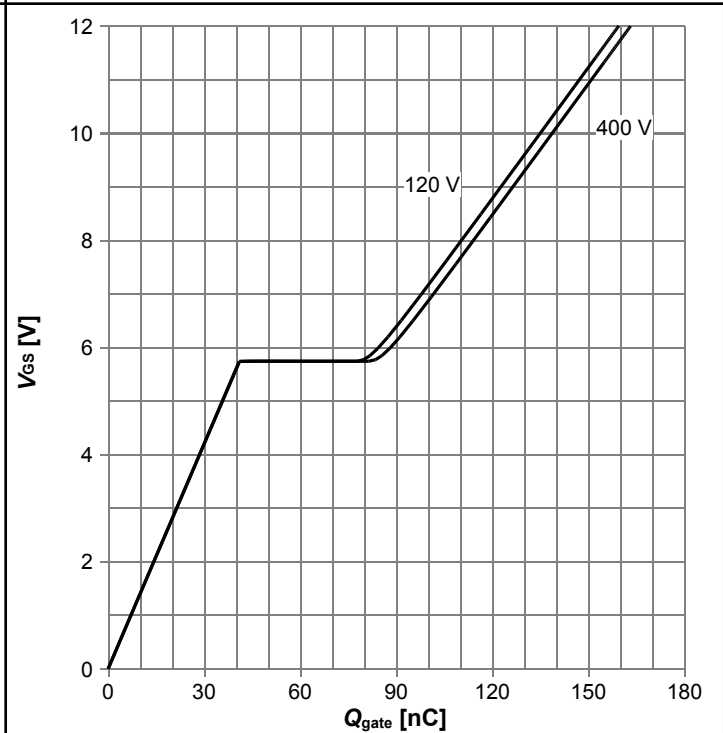


**Diagram 9: Typ. transfer characteristics**



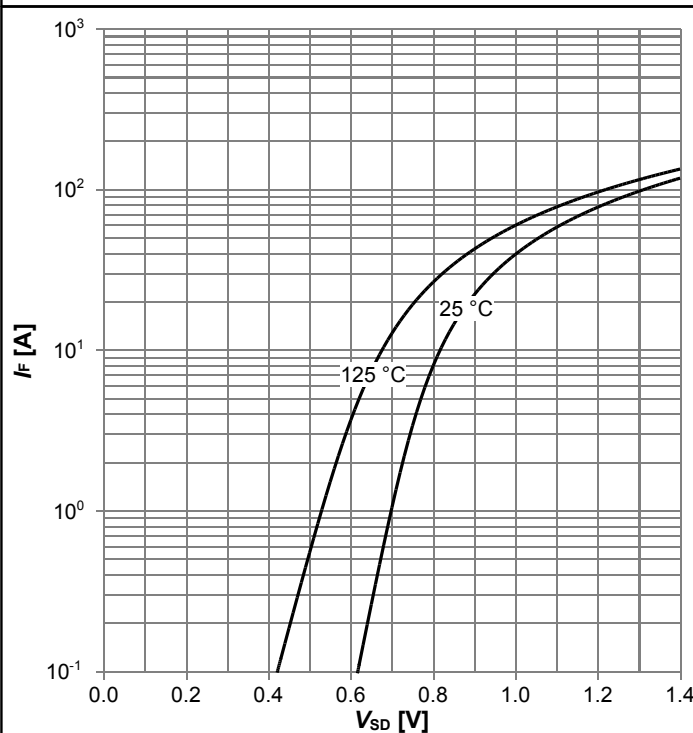
$I_D = f(V_{GS})$ ;  $V_{DS} = 20V$ ; parameter:  $T_j$

**Diagram 10: Typ. gate charge**



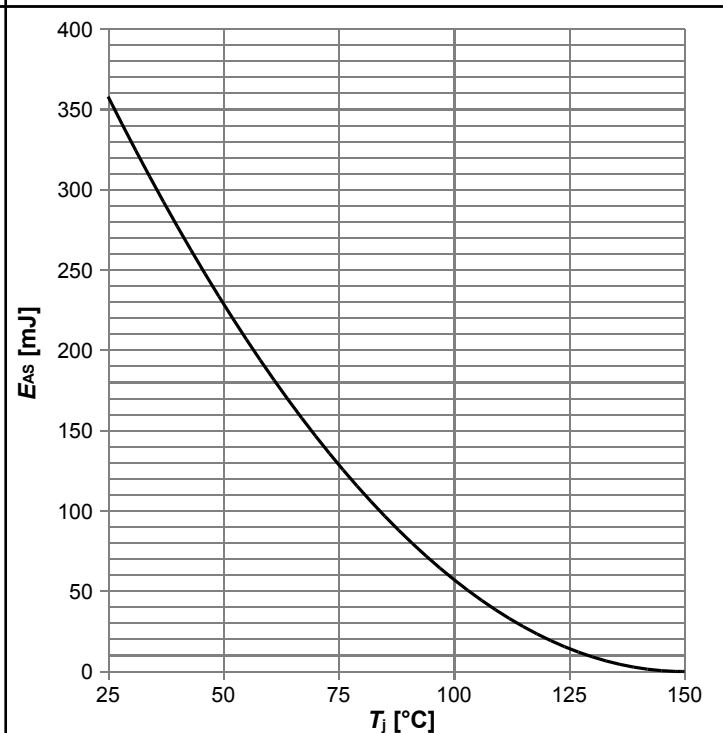
$V_{GS} = f(Q_{gate})$ ;  $I_D = 35.8$  A pulsed; parameter:  $V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



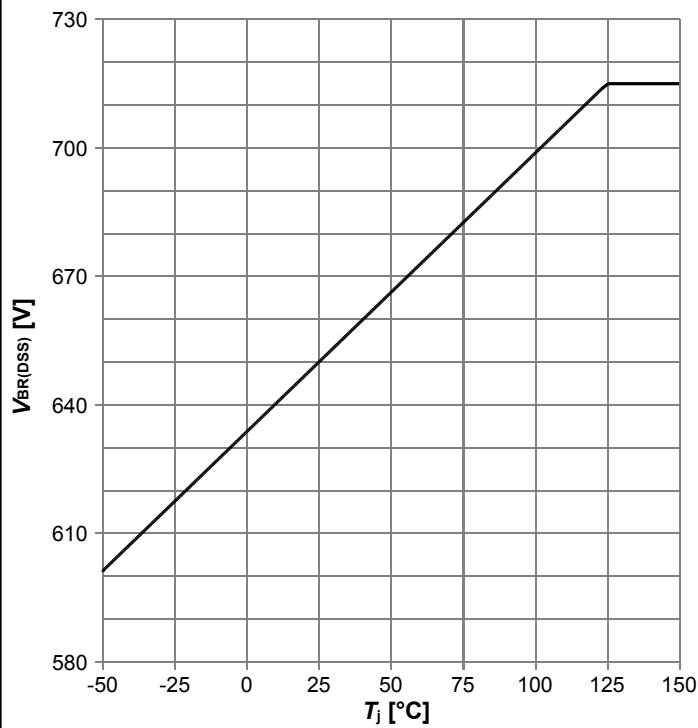
$I_F = f(V_{SD})$ ; parameter:  $T_j$

**Diagram 12: Avalanche energy**



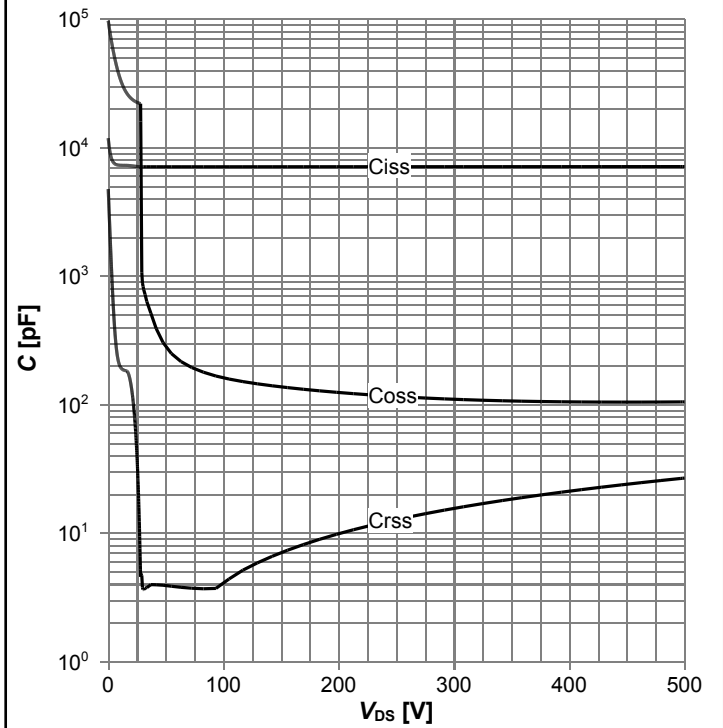
$E_{AS} = f(T_j)$ ;  $I_D = 7.3$  A;  $V_{DD} = 50$  V

**Diagram 13: Drain-source breakdown voltage**



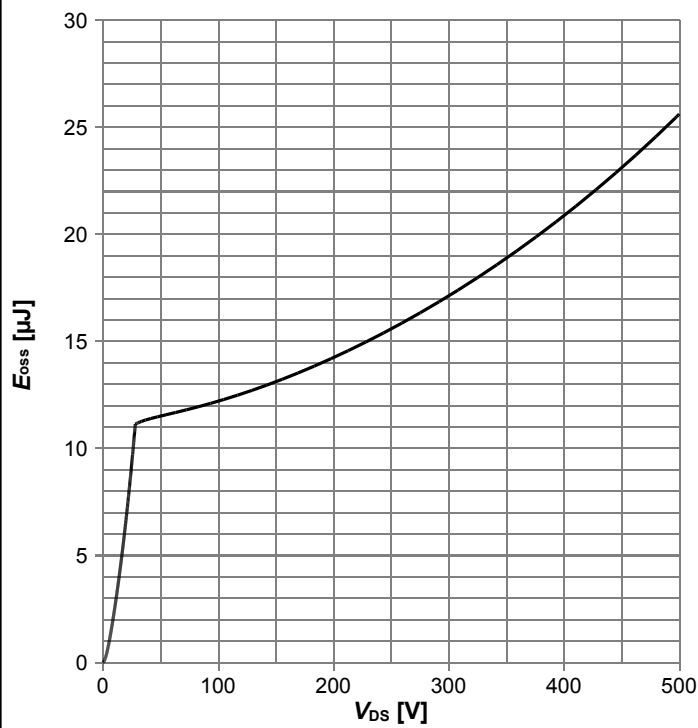
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



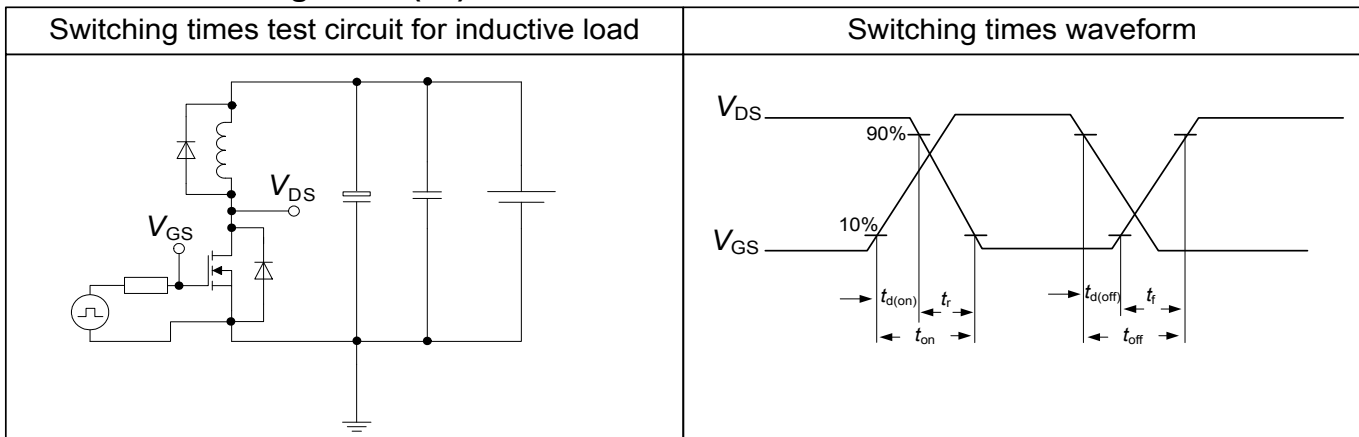
$E_{oss}=f(V_{DS})$

## 5 Test Circuits

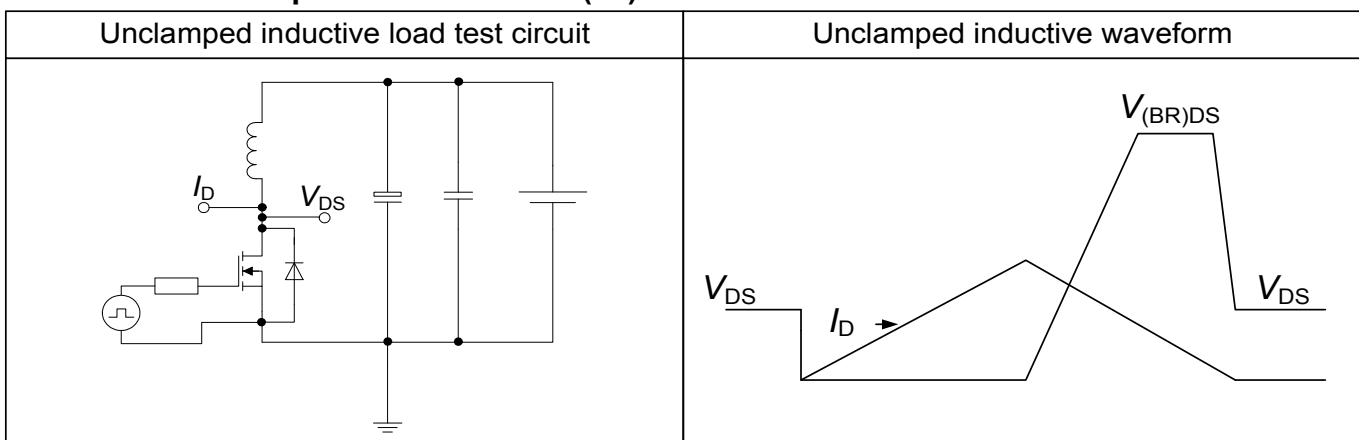
**Table 8 Diode characteristics**



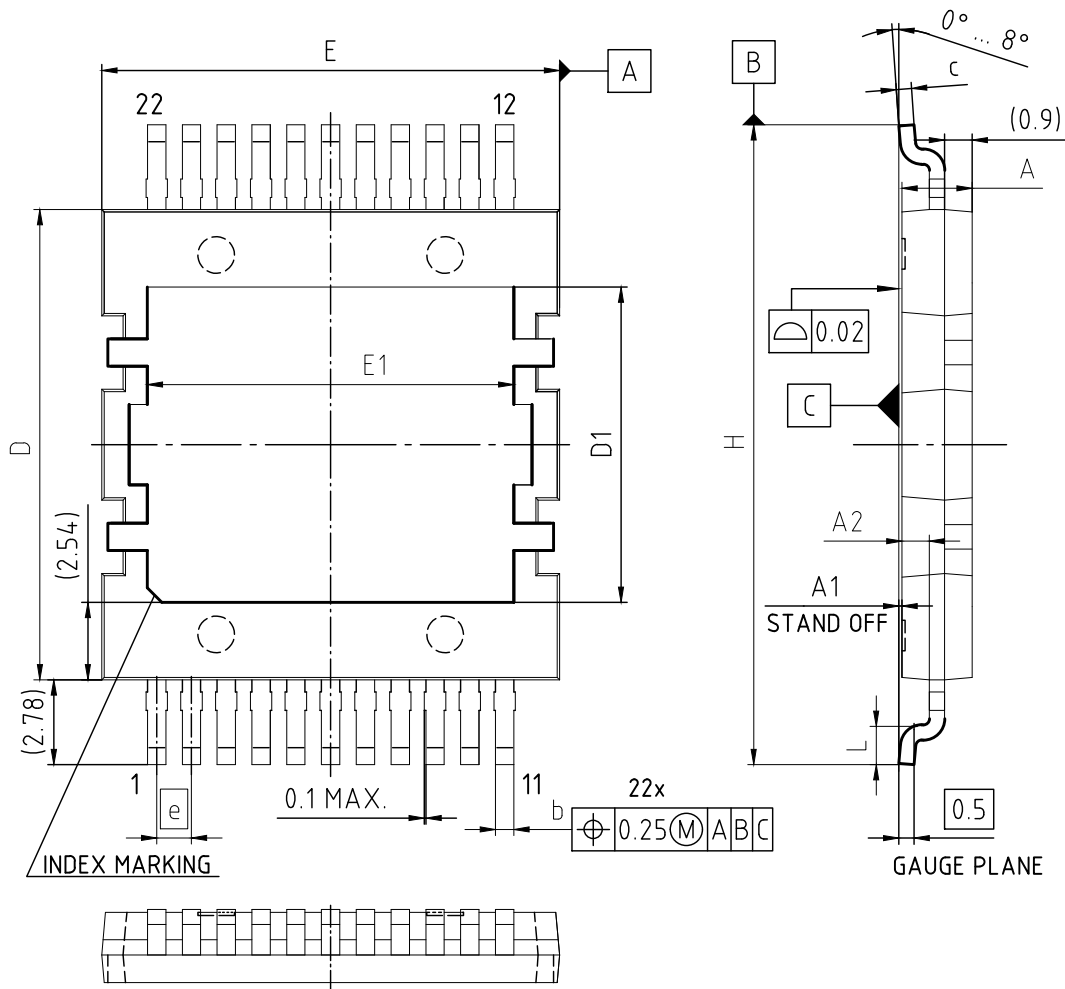
**Table 9 Switching times (ss)**



**Table 10 Unclamped inductive load (ss)**



## 6 Package Outlines



**NOTES:**

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. ALL METAL SURFACES ARE TIN PLATED, EXCEPT AREA OF CUT.

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.89	1.10
b	0.50	0.70
c	0.46	0.58
D	15.30	15.50
D1	10.23	10.43
E	14.90	15.10
E1	11.91	12.11
e	1.14	
N	22	
H	20.86	21.06
L	1.20	1.40

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**Figure 1 Outline PG-HDSOP-22, dimensions in mm**

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS CFD7 650V Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7 650V application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS CFD7 650V simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

## Revision History

IPDQ65R029CFD7

**Revision: 2022-08-26, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-08-26	Release of final version

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