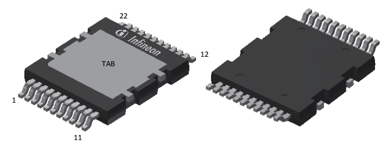
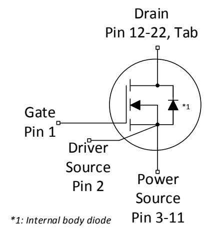
MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process.

PG-HDSOP-22-1





Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)}$*Q_g and $R_{DS(on)}$*E_{oss}
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction. For paralleling 4pin MOSFET devices the placement of the gate resistor is generally recommended to be on the Driver Source instead of the Gate.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	35	mΩ
$Q_{g,typ}$	108	nC
$I_{D,pulse}$	212	A
E_{oss} @ 400V	12.5	µJ
Body diode di_F/dt	1300	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPDQ60R035CFD7	PG-HDSOP-22	60R035F7	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	68 43	A	T_C=25°C T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	212	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	249	mJ	I_D=7.3A; V_{DD}=50V; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	1.25	mJ	I_D=7.3A; V_{DD}=50V; see table 10
Avalanche current, single pulse	I_{AS}	-	-	7.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	V_{DS}=0...400V
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC (f>1 Hz)
Power dissipation	P_{tot}	-	-	367	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	150	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current[1]	I_S	-	-	68	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	212	A	T_C=25°C
Reverse diode dv/dt[3]	dv/dt	-	-	70	V/ns	V_{DS}=0...400V, I_{SD}<=50A, T_j=25°C see table 8
Maximum diode commutation speed	di_F/dt	-	-	1300	A/µs	V_{DS}=0...400V, I_{SD}<=50A, T_j=25°C see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_C=25°C, t=1min

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.34	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	45	55	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area. Tap exposed to air. PCB is vertical without air stream cooling.
Soldering temperature, reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	V_{DS}=V_{GS}, I_D=1.25mA
Zero gate voltage drain current[1]	I_{DSS}	- -	- 26	1 103	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=125°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.028 0.063	0.035 -	Ω	V_{GS}=10V, I_D=24.9A, T_j=25°C V_{GS}=10V, I_D=24.9A, T_j=150°C
Gate resistance	R_G	-	3.8	-	Ω	f=1MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4346	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Output capacitance	C_{oss}	-	85	-	pF	V_{GS}=0V, V_{DS}=400V, f=250kHz
Effective output capacitance, energy related[2]	$C_{o(er)}$	-	156	-	pF	V_{GS}=0V, V_{DS}=0...400V
Effective output capacitance, time related[3]	$C_{o(tr)}$	-	1604	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...400V
Turn-on delay time	$t_{d(on)}$	-	36	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=15.6A, R_G=3.0Ω; see table 9
Rise time	t_r	-	7	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=15.6A, R_G=3.0Ω; see table 9
Turn-off delay time	$t_{d(off)}$	-	108	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=15.6A, R_G=3.0Ω; see table 9
Fall time	t_f	-	4	-	ns	V_{DD}=400V, V_{GS}=10V, I_D=15.6A, R_G=3.0Ω; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24	-	nC	V_{DD}=400V, I_D=15.6A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	40	-	nC	V_{DD}=400V, I_D=15.6A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	108	-	nC	V_{DD}=400V, I_D=15.6A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	V_{DD}=400V, I_D=15.6A, V_{GS}=0 to 10V

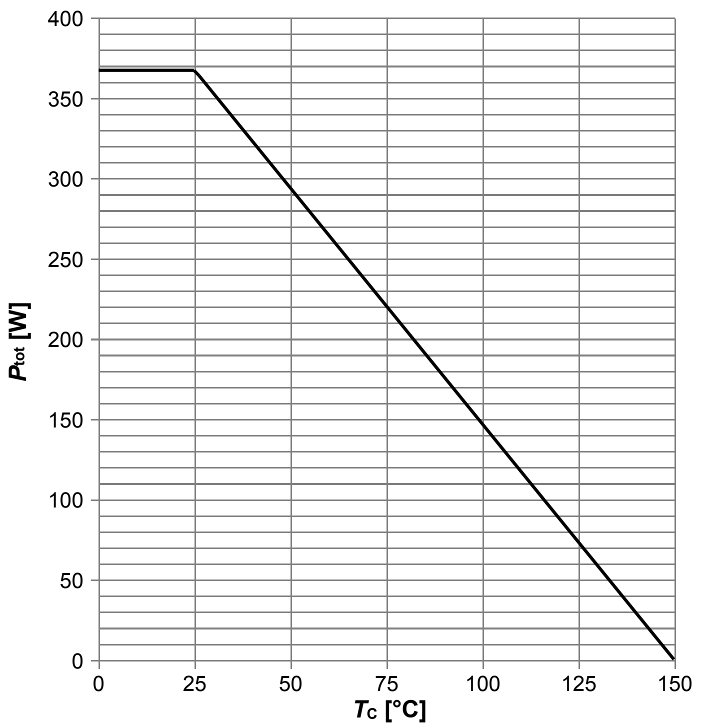
[1] Maximum specification is defined by calculated six sigma upper confidence bound
[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=24.9A, T_j=25°C
Reverse recovery time	t_{rr}	-	155	232	ns	V_R=400V, I_F=15.6A, di_F/dt=100A/µs; see table 8
Reverse recovery charge	Q_{rr}	-	0.87	1.74	µC	V_R=400V, I_F=15.6A, di_F/dt=100A/µs; see table 8
Peak reverse recovery current	I_{rrm}	-	9.9	-	A	V_R=400V, I_F=15.6A, di_F/dt=100A/µs; see table 8

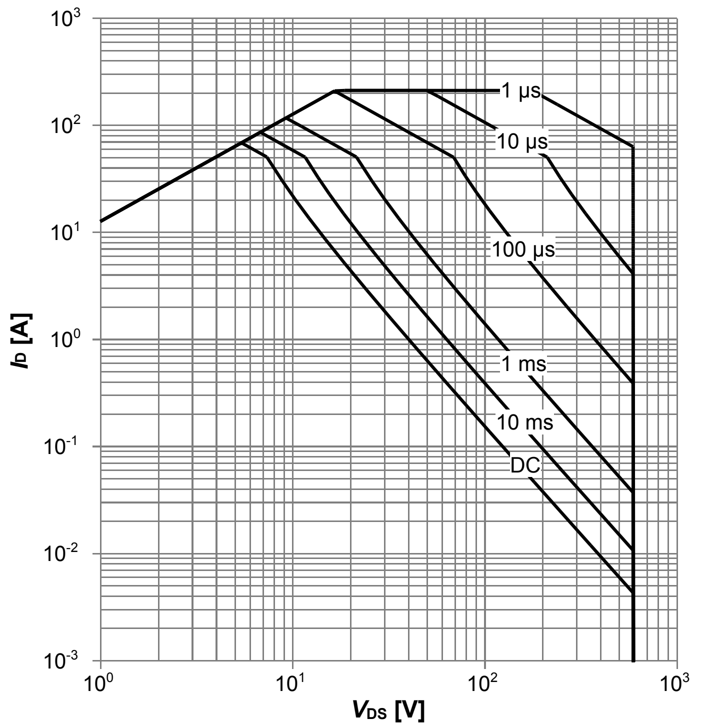
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



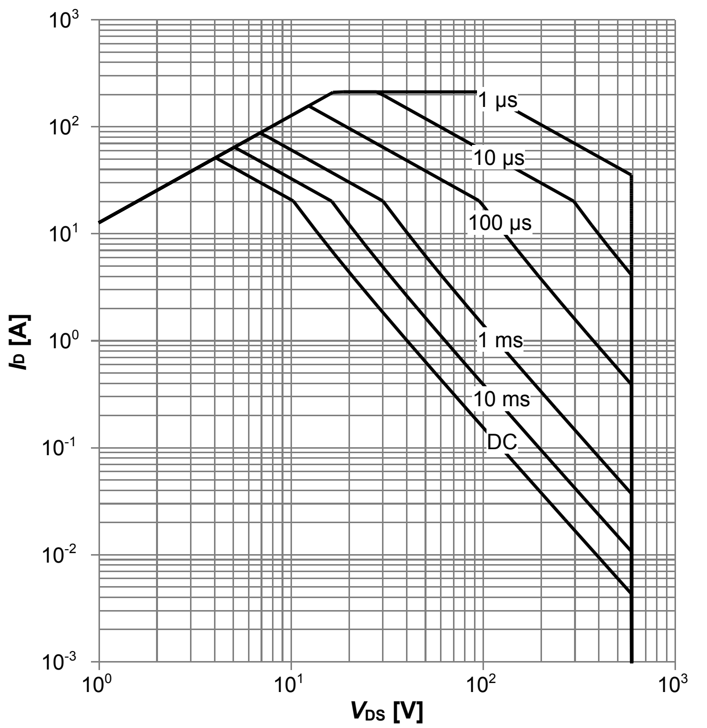
P_{tot}=f(T_C)

Diagram 2: Safe operating area



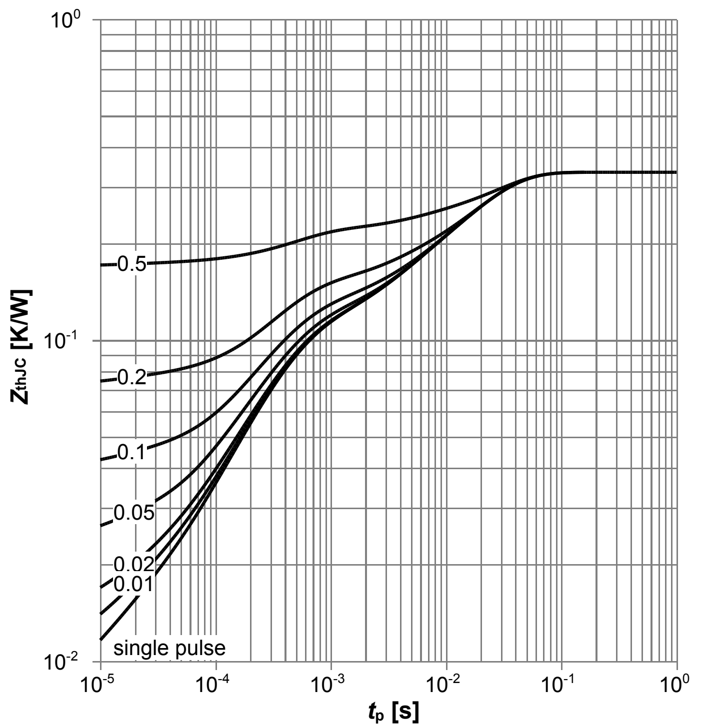
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJC} =f(t_P); parameter: D=t_p/T

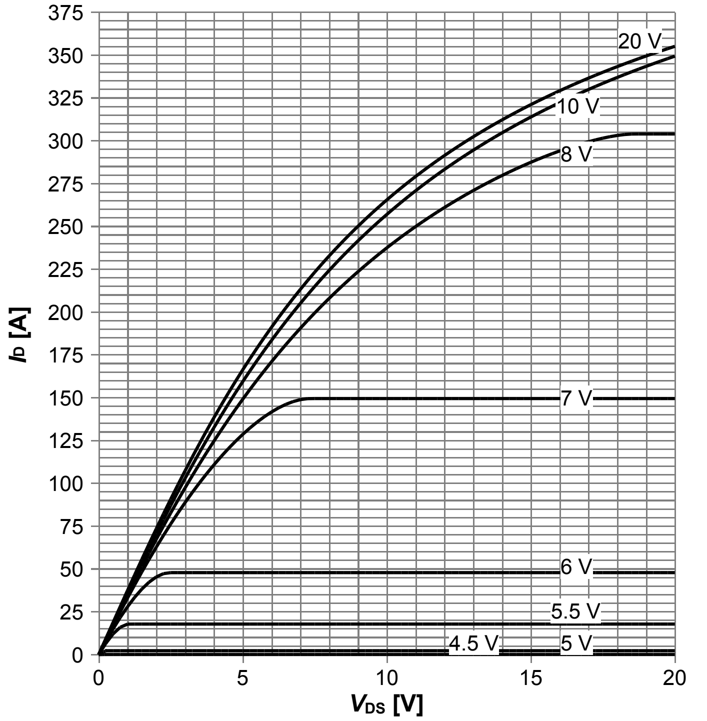
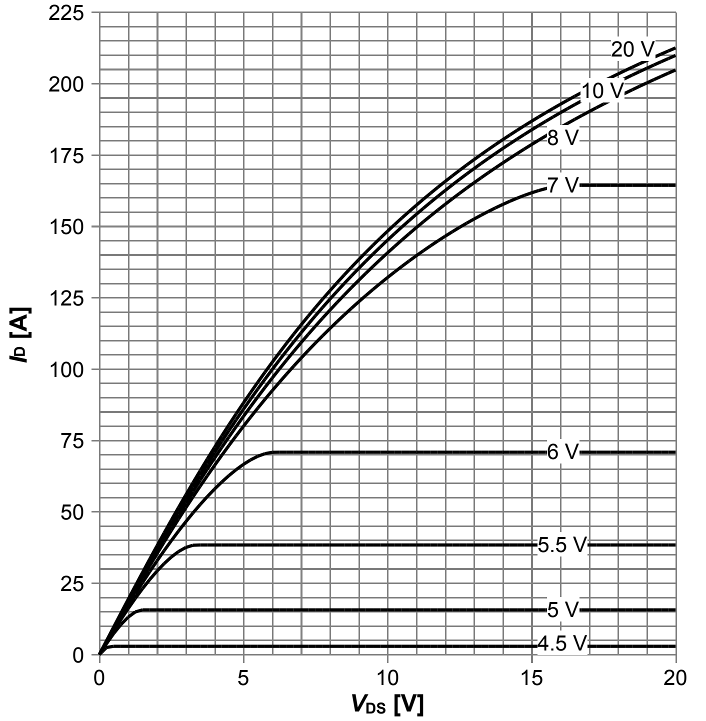
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

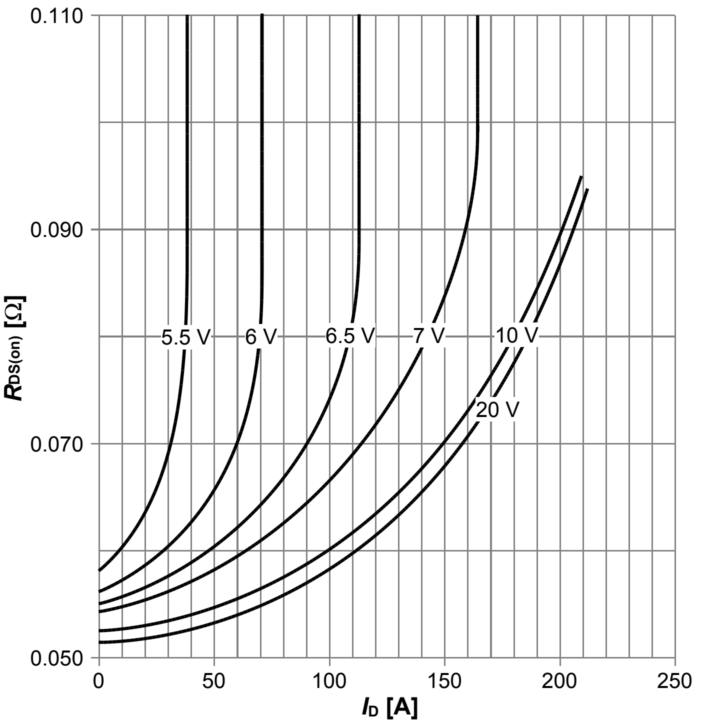
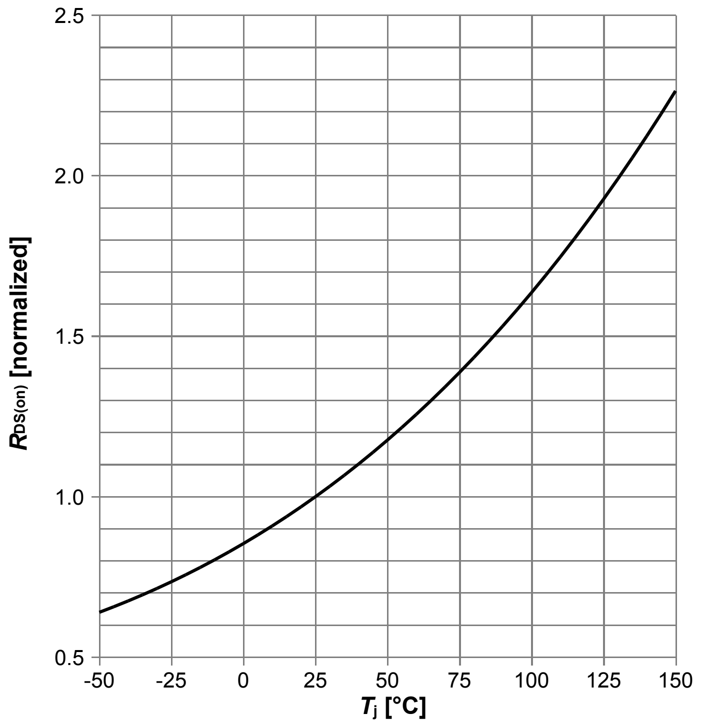
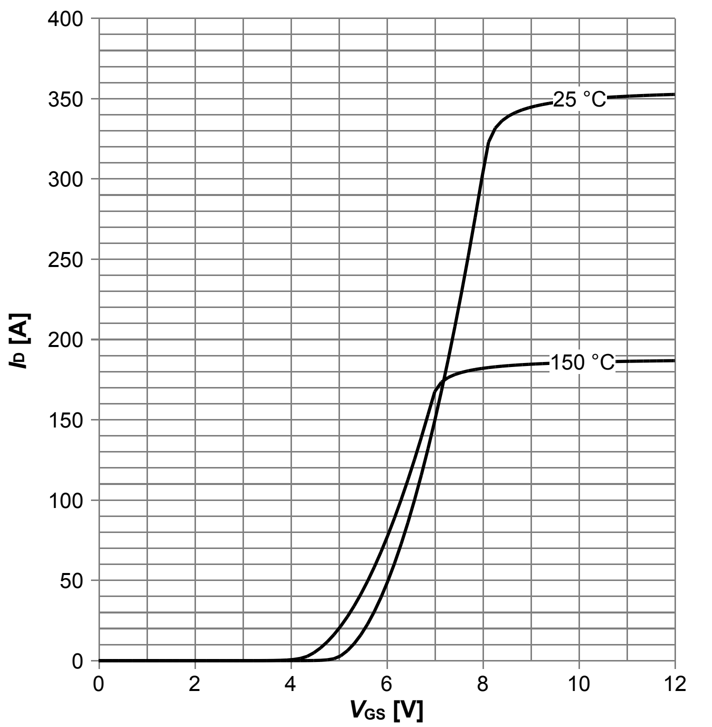
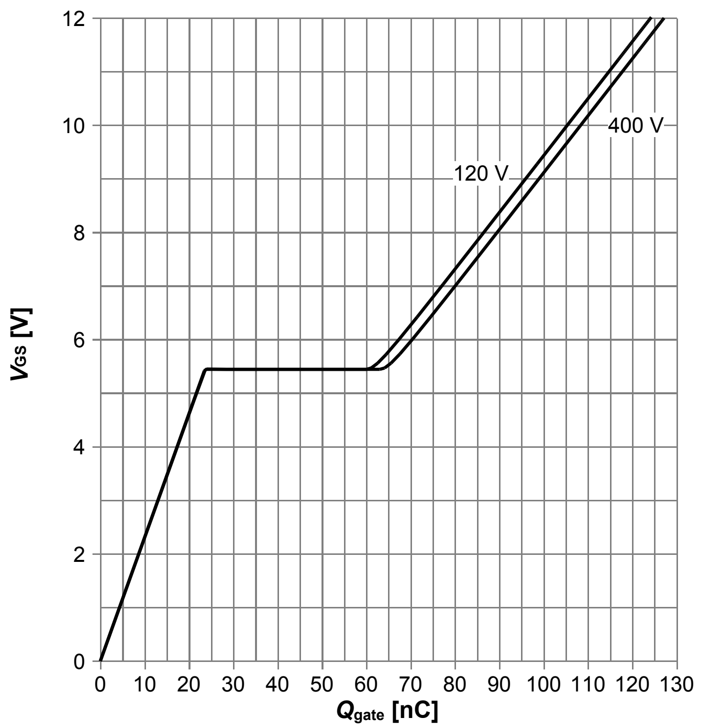
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=24.9 A; V_{GS}=10 V

Diagram 9: Typ. transfer characteristics



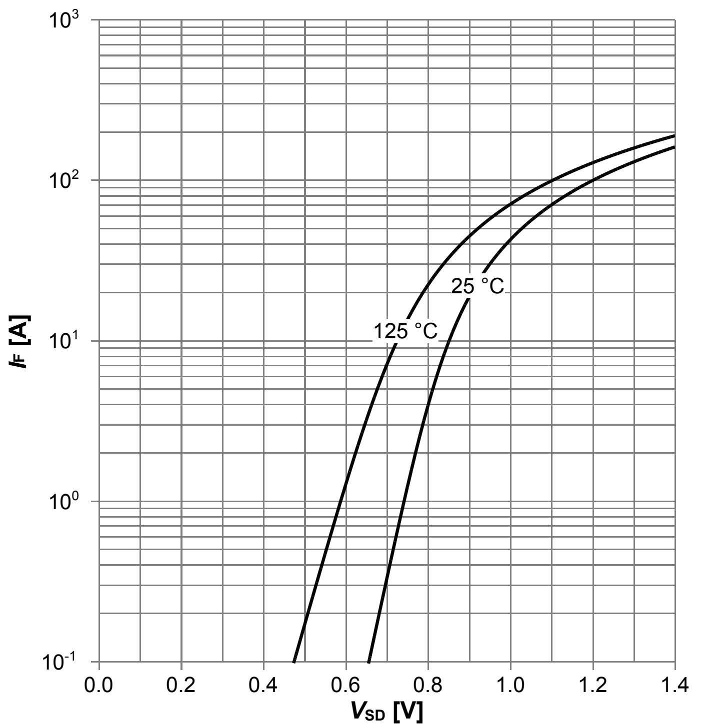
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j

Diagram 10: Typ. gate charge



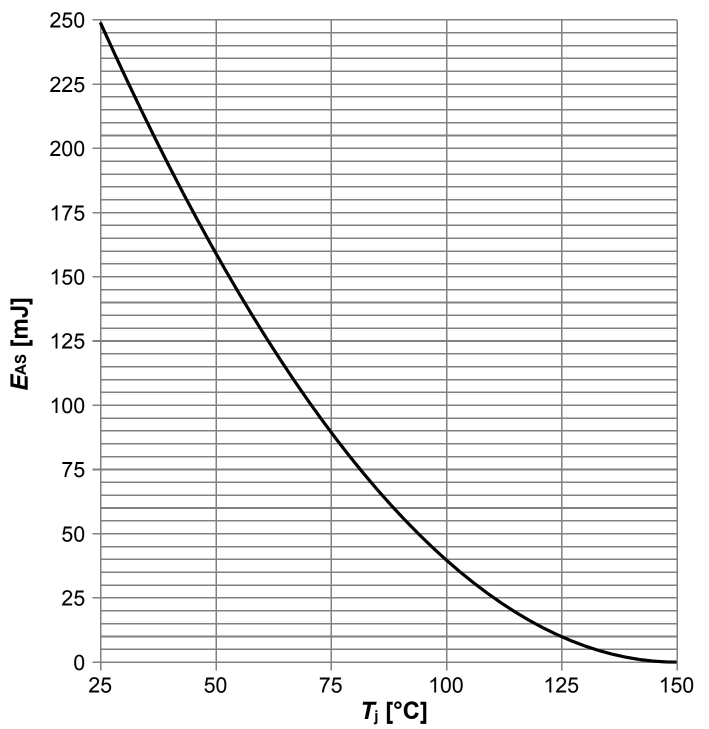
V_{GS}=f(Q_{gate}); I_D=15.6 A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



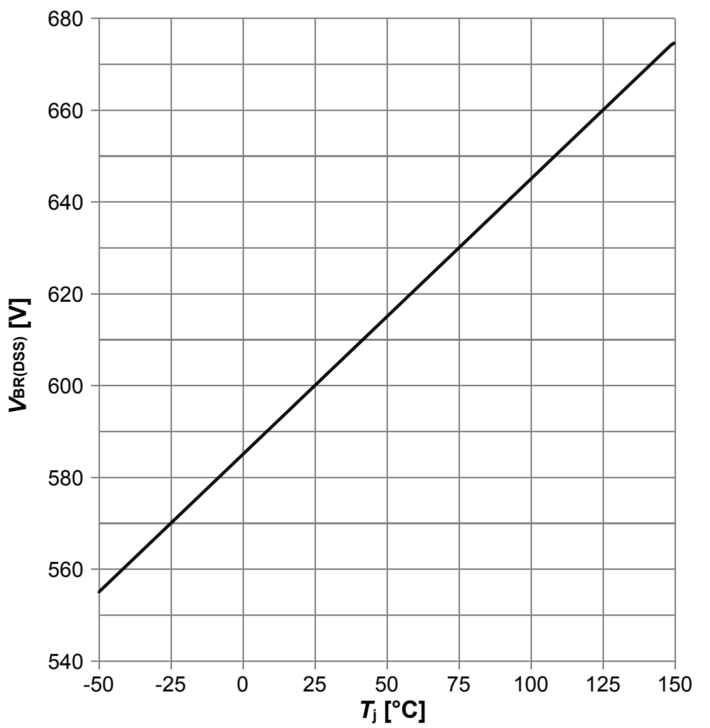
I_F=f(V_{SD}); parameter: T_j

Diagram 12: Avalanche energy



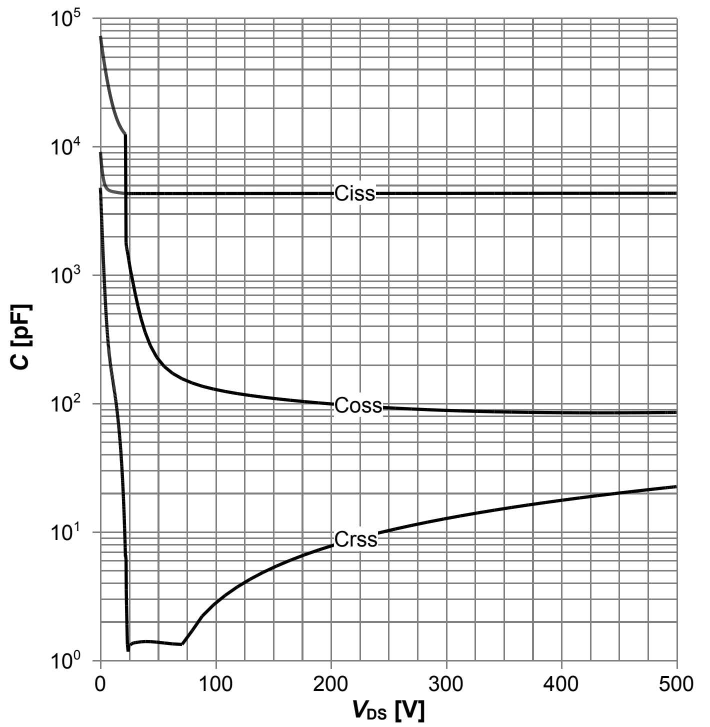
E_{AS}=f(T_j); I_D=7.3 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



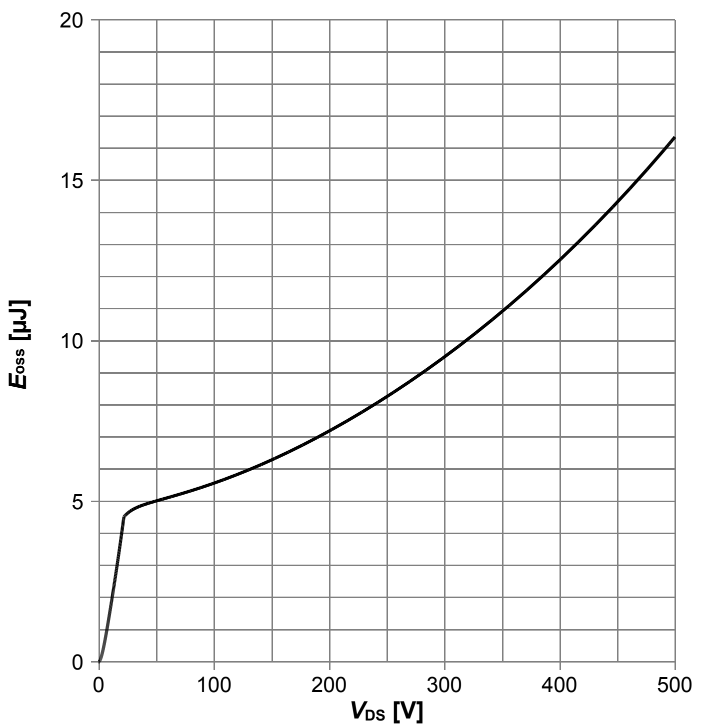
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=250 kHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

5 Test Circuits

Table 8 Diode characteristics

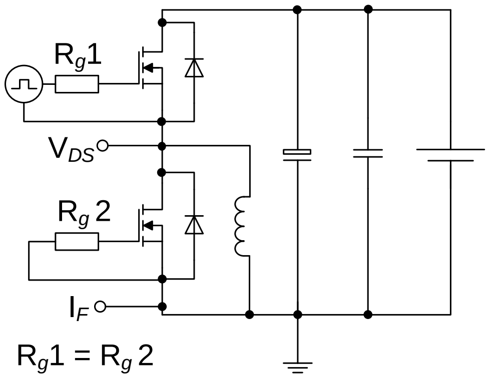
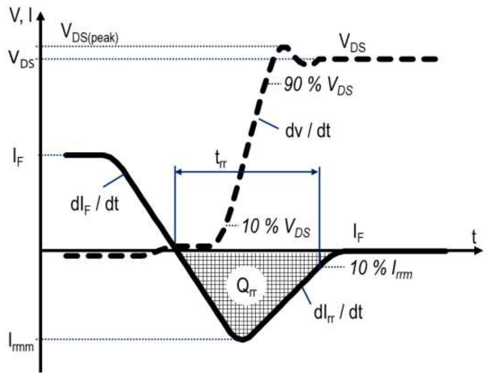
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times (ss)

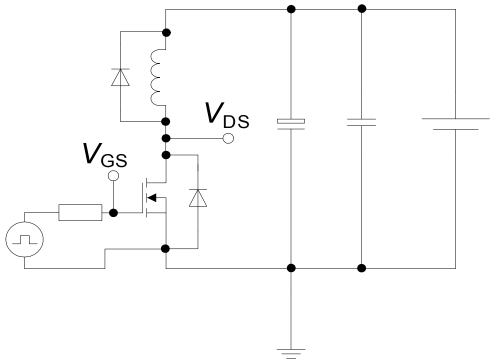
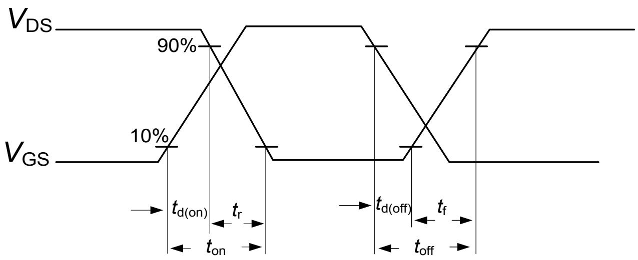
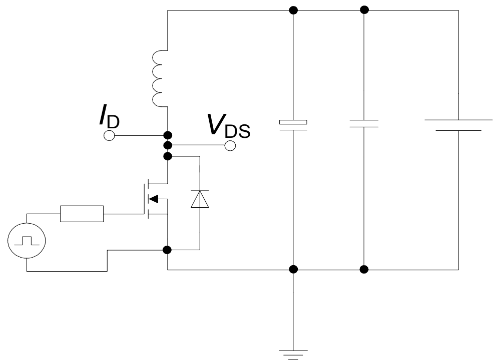
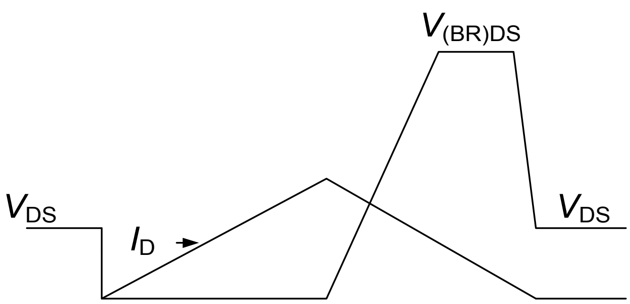
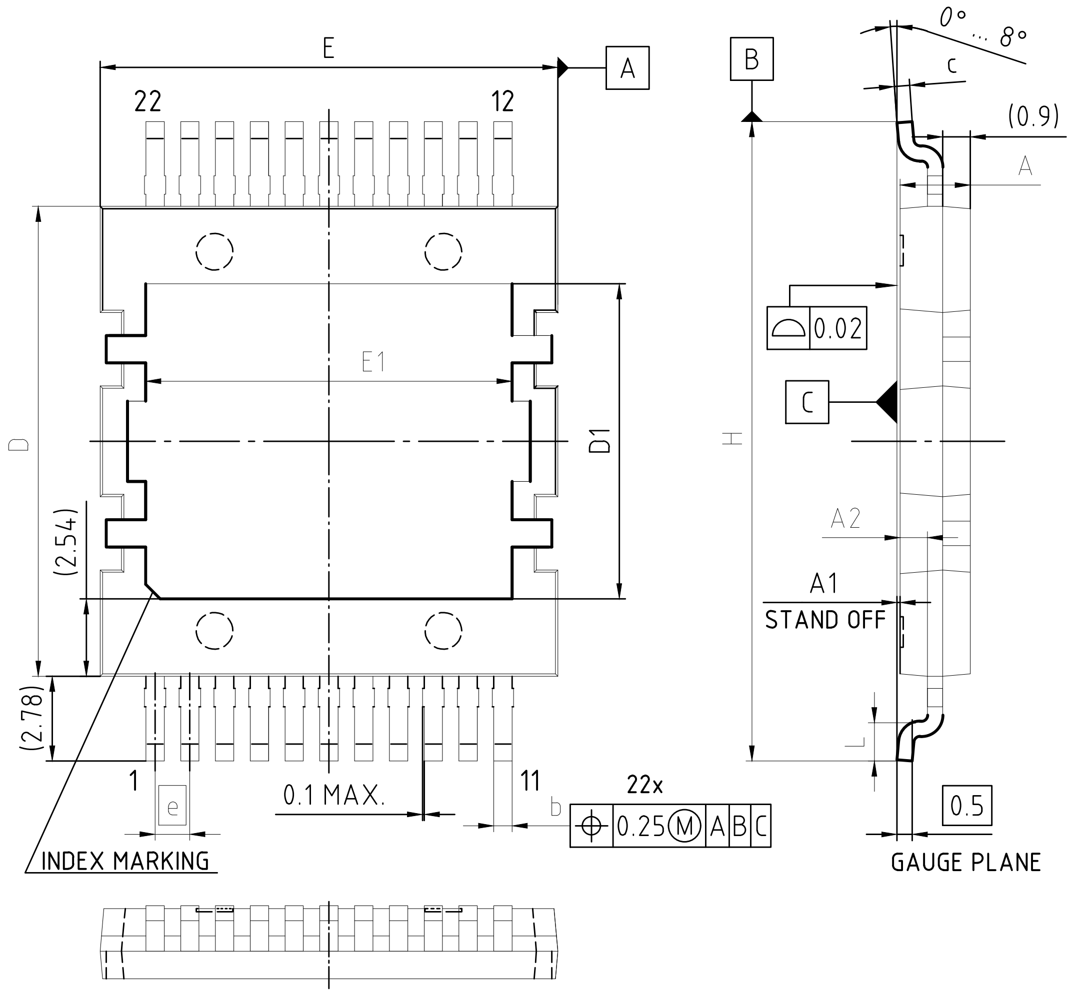
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:

1. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. ALL METAL SUFACES ARE TIN PLATED, EXCEPT AREA OF CUT.

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.35
A1	0.00	0.15
A2	0.89	1.10
b	0.50	0.70
c	0.46	0.58
D	15.30	15.50
D1	10.23	10.43
E	14.90	15.10
E1	11.91	12.11
e	1.14	
N	22	
H	20.86	21.06
L	1.20	1.40

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REVISION 02
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION
ISSUE DATE 16.01.2018

Figure 1 Outline PG-HDSOP-22, dimensions in mm

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPDQ60R035CFD7

Revision: 2021-09-22, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-09-22	Release of final version

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