

# MOSFET

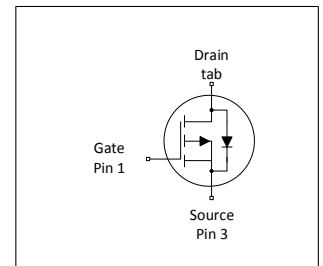
## OptiMOS™ Power Transistor, -60 V

### Features

- P-Channel
- Very low on-resistance  $R_{DS(on)}$
- 100% avalanche tested
- Normal Level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

#### Product Validation:

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	-60	V
$R_{DS(on),max}$	400	mΩ
$I_D$	-4.3	A

Type / Ordering Code	Package	Marking	Related Links
IPD06P007N	PG-TO 252-3	06P007N	-

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## 1 Maximum ratings

at  $T_C=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	-4.3 -3.3	A	$V_{GS}=-10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$ , $T_C=100\text{ °C}$
Pulsed drain current <sup>1)</sup>	$I_{D,pulse}$	-	-	-17.2	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	-	-	43	mJ	$I_D=-4.3\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	19	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	-	7.9	°C/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>3)</sup>	$R_{thJA}$	-	-	75	°C/W	-

## 3 Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=-250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	-2.1	-3	-4	V	$V_{DS}=V_{GS}$ , $I_D=-166\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	-0.1 -10	1 -100	$\mu\text{A}$	$V_{DS}=-60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$ $V_{DS}=-60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	-10	-100	nA	$V_{GS}=-20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	328	400	m $\Omega$	$V_{GS}=-10\text{ V}$ , $I_D=-4.3\text{ A}$
Gate resistance	$R_G$	-	4	-	$\Omega$	-
Transconductance	$g_{fs}$	-	3.8	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$ , $I_D=-4.3\text{ A}$

<sup>1)</sup> See Diagram 3 for more detailed information

<sup>2)</sup> See Diagram 13 for more detailed information

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	260	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=-30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	40	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=-30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	12	-	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=-30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	$V_{DD}=-30\text{ V}$ , $V_{GS}=-10\text{ V}$ , $I_D=-2.15\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Rise time	$t_r$	-	6	-	ns	$V_{DD}=-30\text{ V}$ , $V_{GS}=-10\text{ V}$ , $I_D=-2.15\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Turn-off delay time	$t_{d(off)}$	-	10	-	ns	$V_{DD}=-30\text{ V}$ , $V_{GS}=-10\text{ V}$ , $I_D=-2.15\text{ A}$ , $R_{G,ext}=1.6\ \Omega$
Fall time	$t_f$	-	4	-	ns	$V_{DD}=-30\text{ V}$ , $V_{GS}=-10\text{ V}$ , $I_D=-2.15\text{ A}$ , $R_{G,ext}=1.6\ \Omega$

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	1.5	-	nC	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	0.8	-	nC	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	2.7	-	nC	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Switching charge	$Q_{sw}$	-	3.4	-	nC	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Gate charge total	$Q_g$	-	6.7	-	nC	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=-30\text{ V}$ , $I_D=-4.3\text{ A}$ , $V_{GS}=0\text{ to }-10\text{ V}$
Output charge	$Q_{oss}$	-	-2.9	-	nC	$V_{DD}=-30\text{ V}$ , $V_{GS}=0\text{ V}$

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	-4.3	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-17.2	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	-0.9	-1.2	V	$V_{GS}=0\text{ V}$ , $I_F=-4.3\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery time	$t_{rr}$	-	36	-	ns	$V_R=-30\text{ V}$ , $I_F=-4.3\text{ A}$ , $di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge	$Q_{rr}$	-	-60	-	nC	$V_R=-30\text{ V}$ , $I_F=-4.3\text{ A}$ , $di_F/dt=-100\text{ A}/\mu\text{s}$

<sup>1)</sup> See Diagram "Gate charge waveforms" for gate charge parameter definition

## 4 Electrical characteristics diagrams

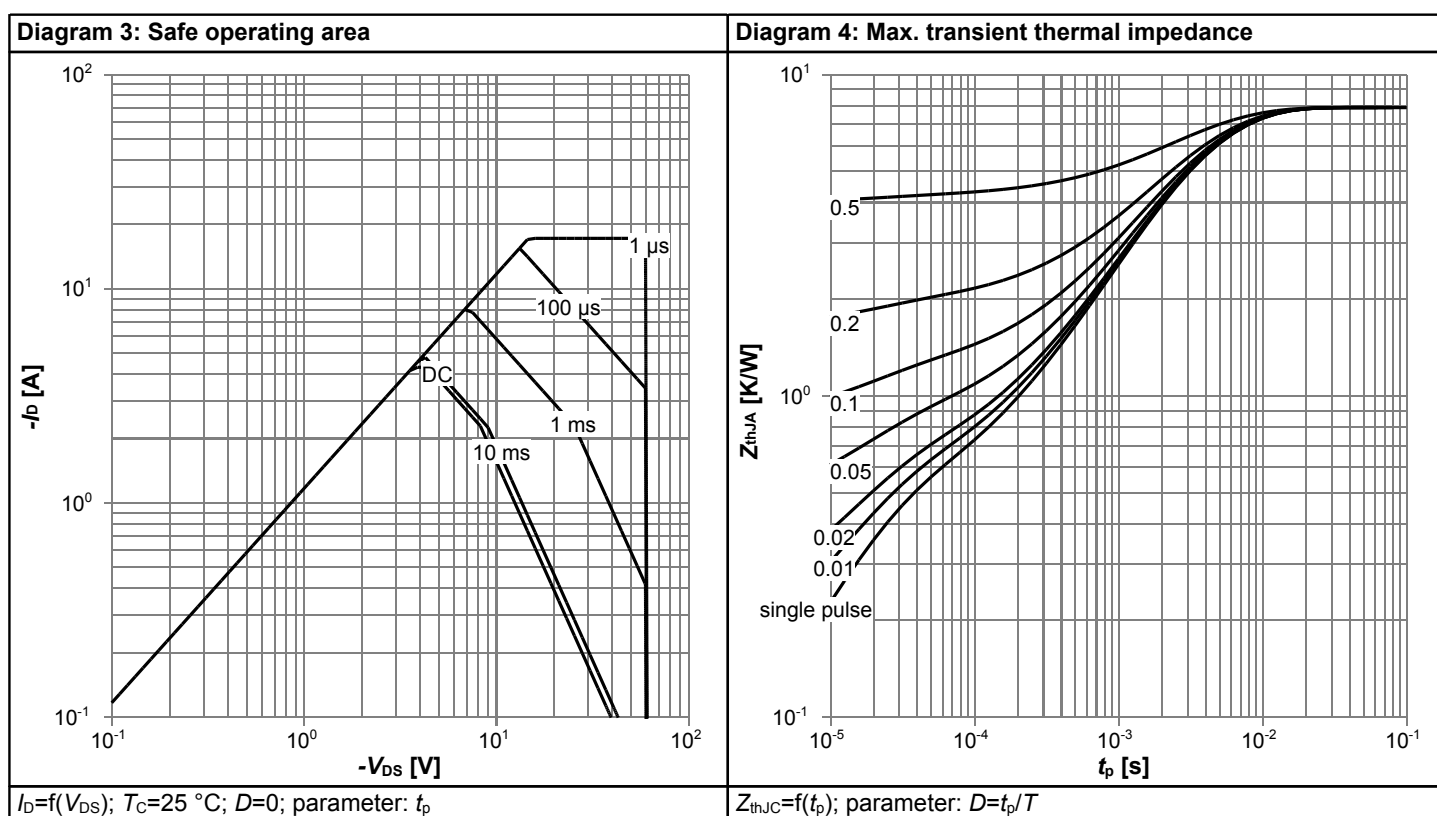
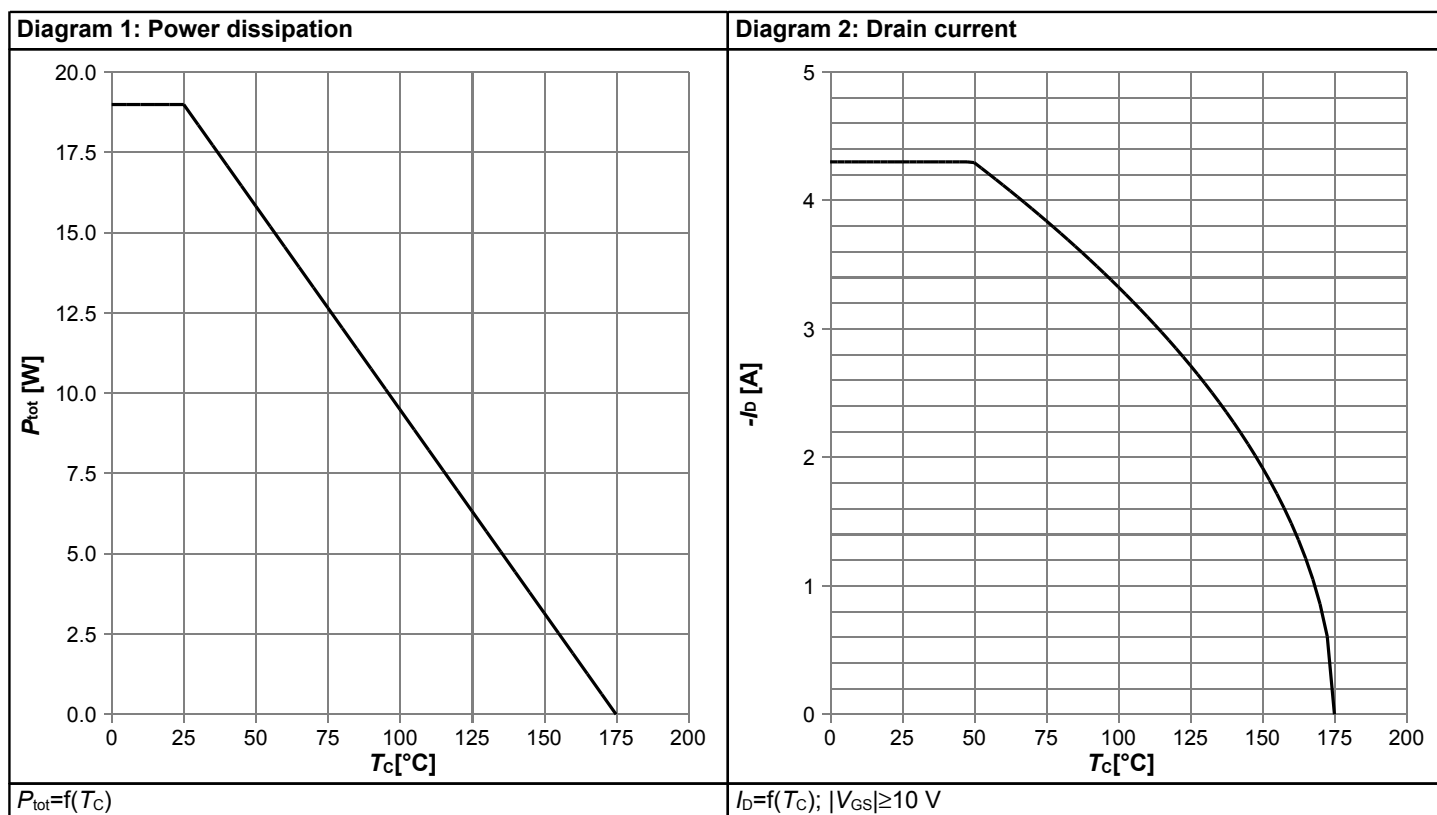
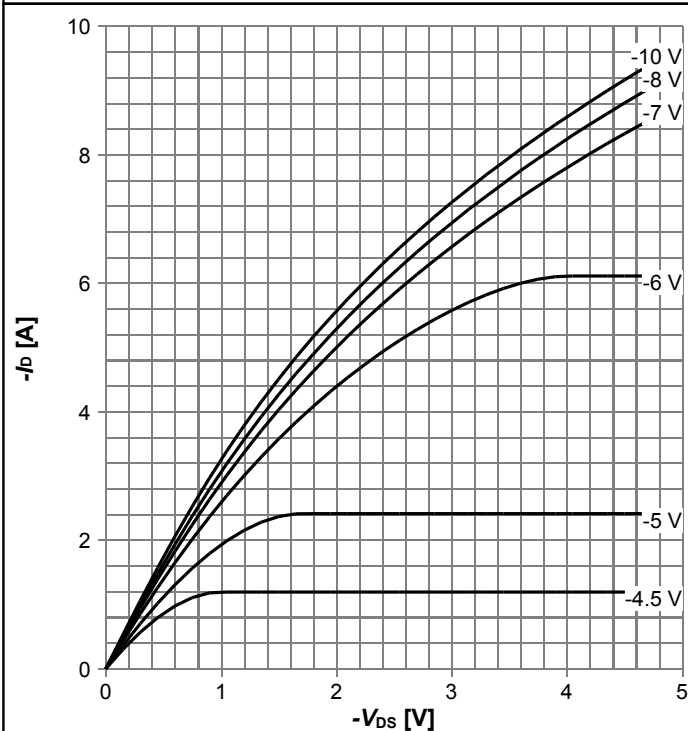
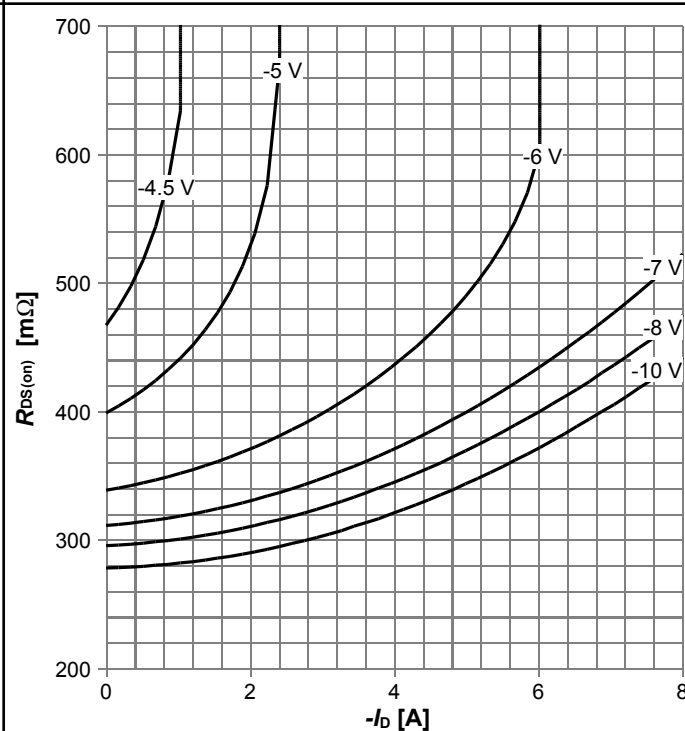


Diagram 5: Typ. output characteristics



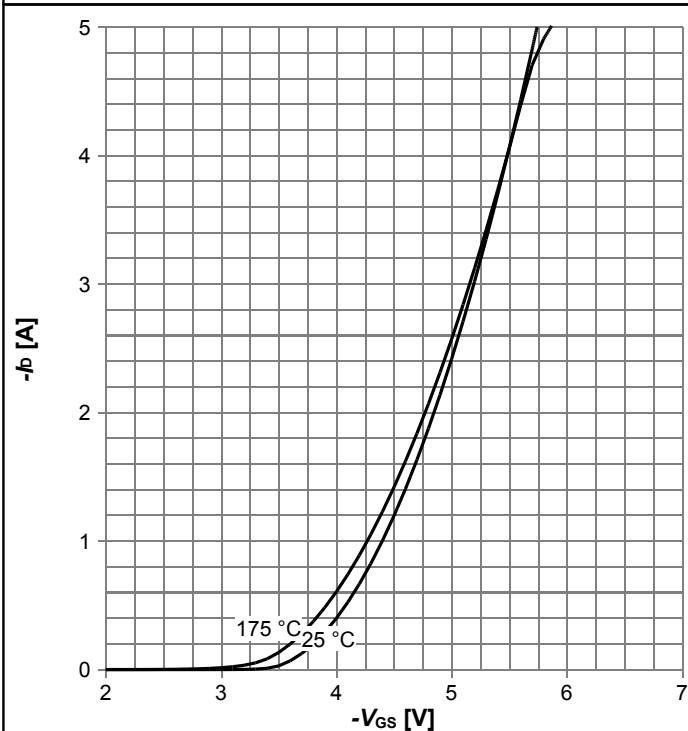
$I_D = f(V_{DS})$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



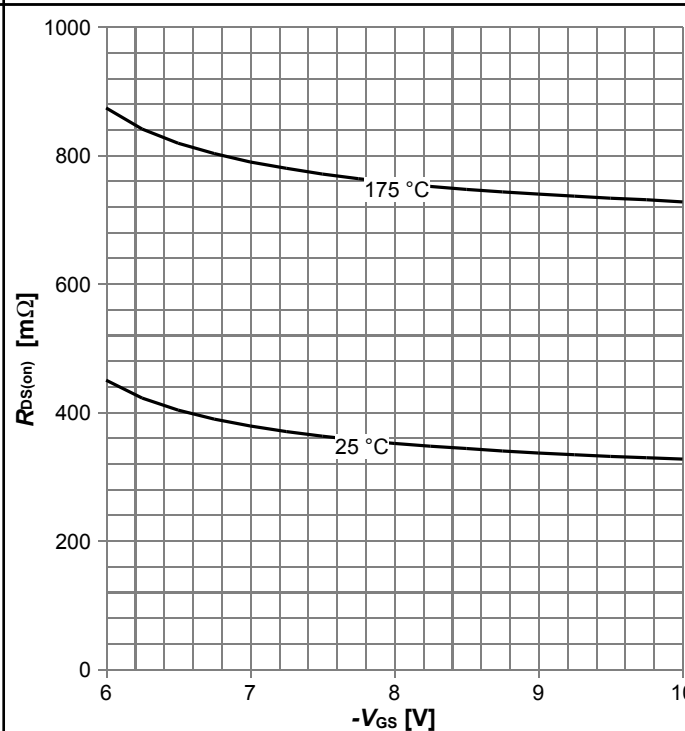
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25^\circ\text{C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



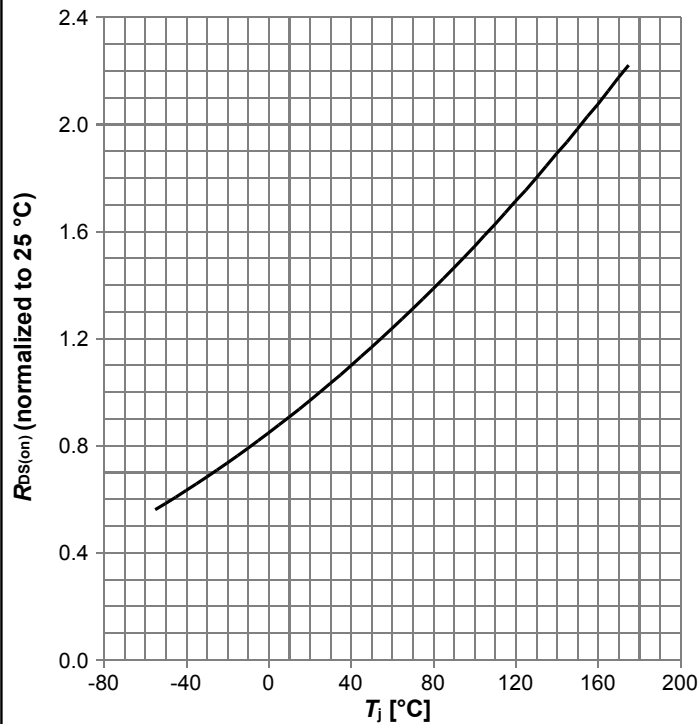
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. drain-source on resistance



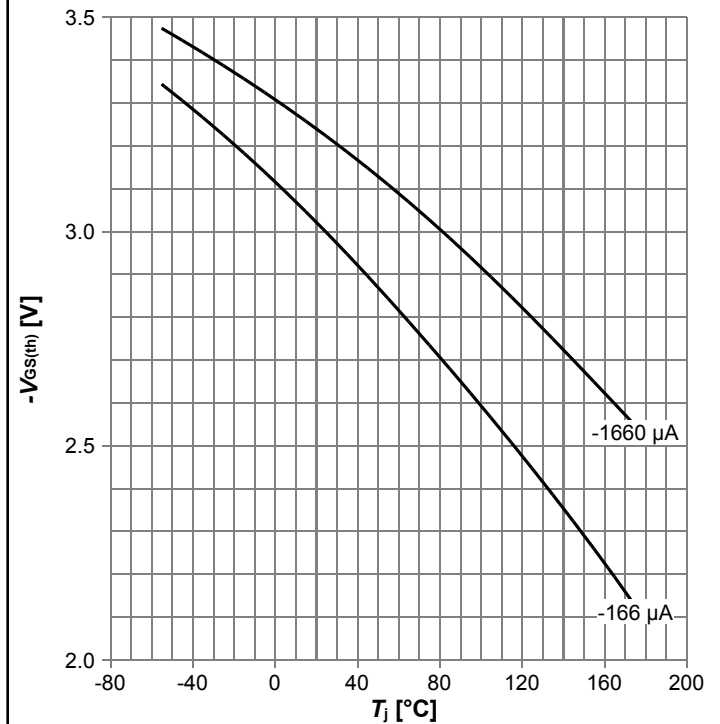
$R_{DS(on)} = f(V_{GS})$ ,  $I_D = -4.3\text{ A}$ ; parameter:  $T_j$

Diagram 9: Normalized drain-source on resistance



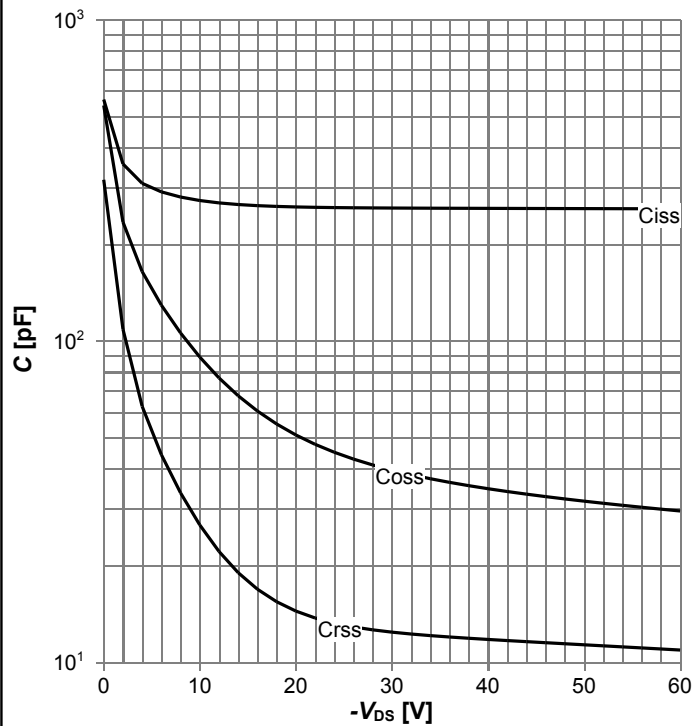
$R_{DS(on)} = f(T_j)$ ,  $I_D = 4.3$  A,  $V_{GS} = -10$  V

Diagram 10: Typ. gate threshold voltage



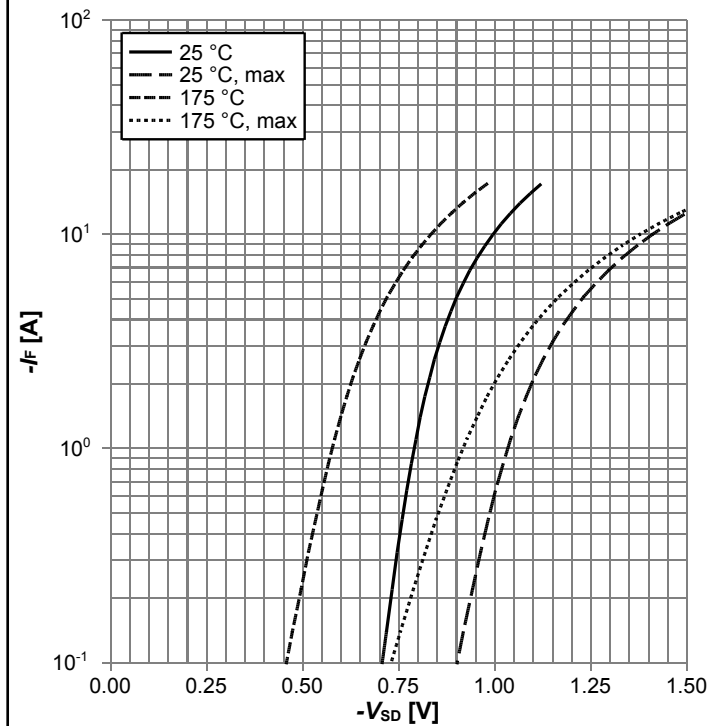
$V_{GS(th)} = f(T_j)$ ,  $V_{GS} = V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



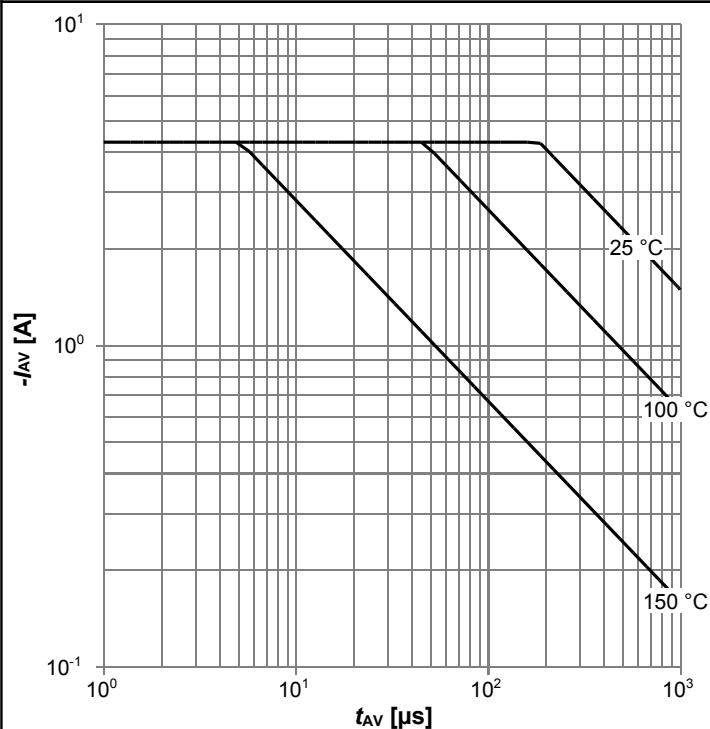
$C = f(V_{DS})$ ;  $V_{GS} = 0$  V;  $f = 1$  MHz

Diagram 12: Forward characteristics of reverse diode



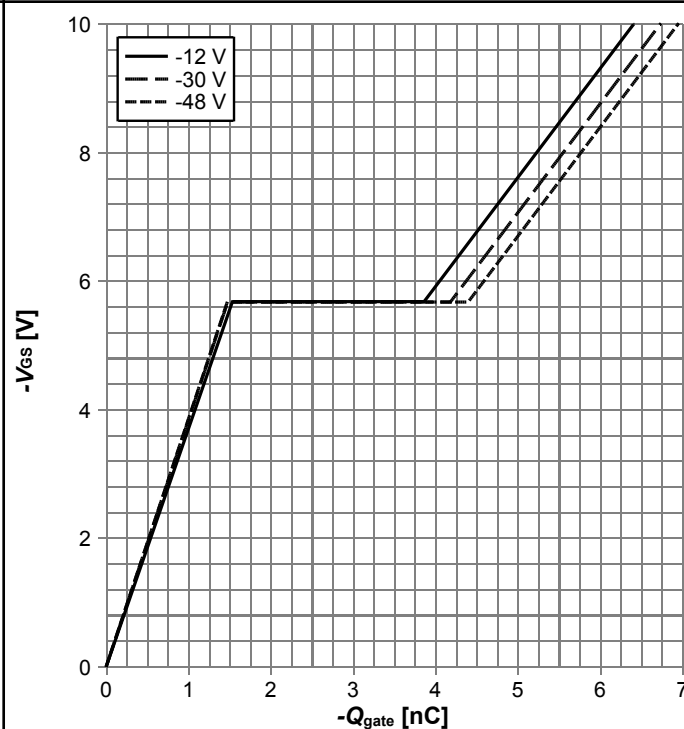
$I_F = f(V_{SD})$ ; parameter:  $T_j$

Diagram 13: Avalanche characteristics



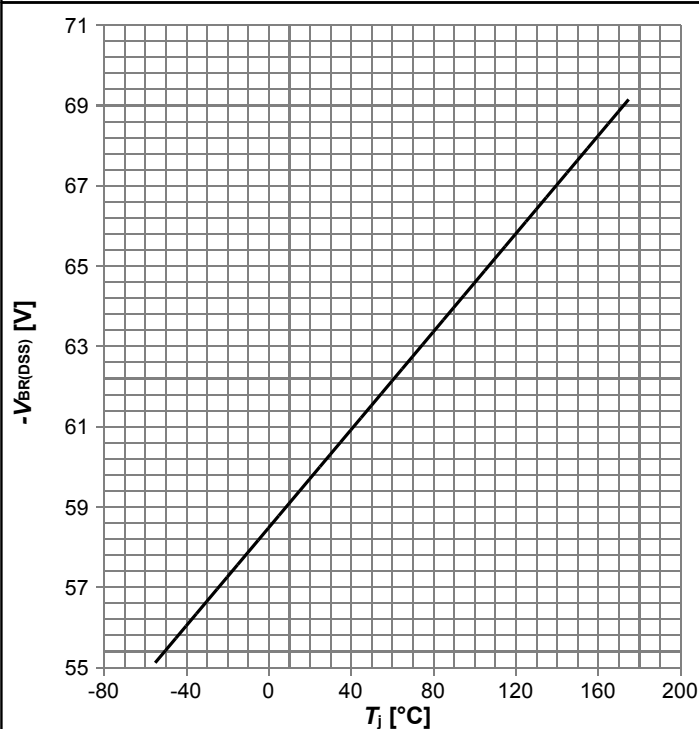
$I_{AS}=f(t_{AV})$ ;  $R_{GS}=25\ \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



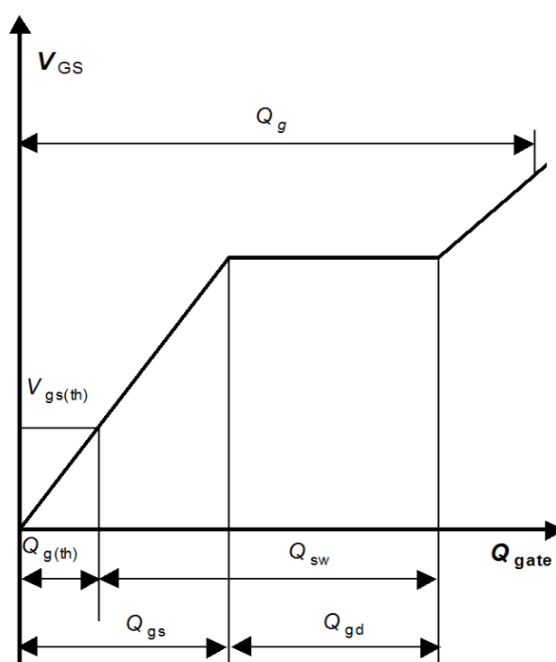
$V_{GS}=f(Q_{gate})$ ,  $I_D=-4.3\text{ A}$  pulsed,  $T_j=25\text{ °C}$ ; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



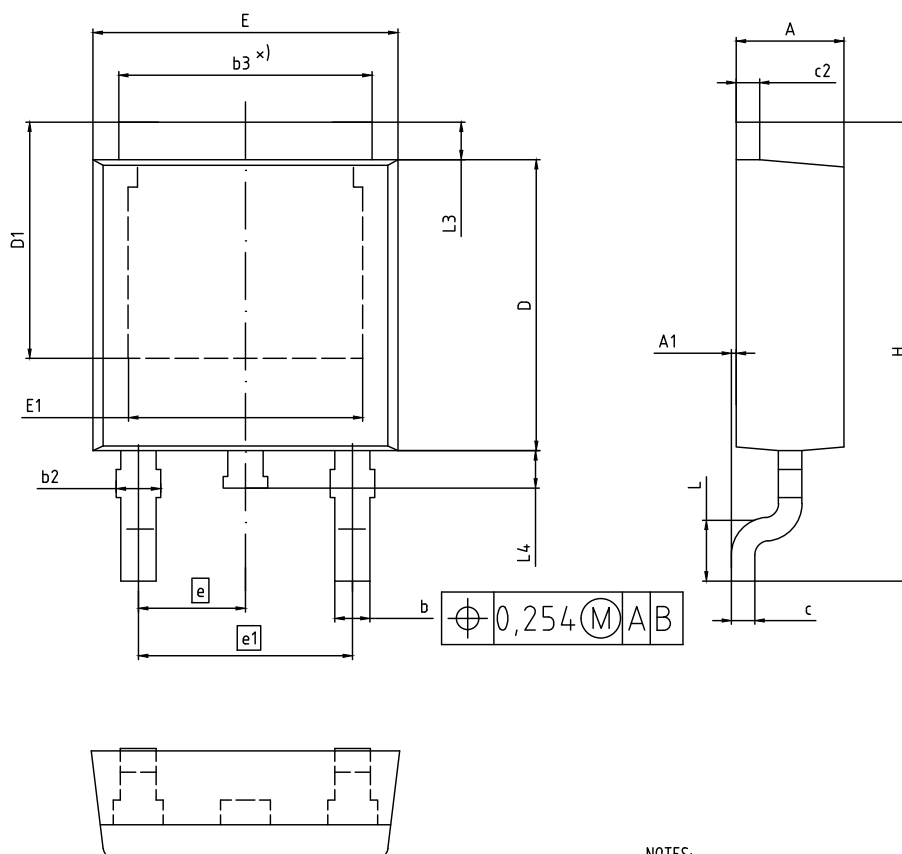
$V_{BR(DSS)}=f(T_j)$ ;  $I_D=-250\ \mu\text{A}$

Diagram Gate charge waveforms





## 5 Package Outlines



### NOTES:

1. INDUSTRIAL QUALITY GRADE
2. ALL DIMENSIONS REFER TO JEDEC STANDARD TO-252 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

<b>DOCUMENT NO.</b> Z8B00003328
<b>SCALE</b> 0 2.5 5mm
<b>EUROPEAN PROJECTION</b> 
<b>ISSUE DATE</b> 05-02-2016
<b>REVISION</b> 06

Figure 1 Outline PG-TO 252-3, dimensions in mm/inches

## Revision History

IPD06P007N

**Revision: 2018-05-09, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-05-09	Release of final version

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