# OptiMOS™-T2 Power-Transistor

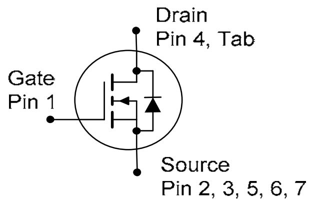
### Product Summary

| | | |
|---|---|---|
| $V_{DS}$ | 30 | V |
| $R_{DS(on)}$ | 0.95 | mΩ |
| $I_D$ | 180 | A |

PG-TO263-7-3

### Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested




| **Type** | **Package** | **Marking** |
|---|---|---|
| IPB180N03S4L-H0 | PG-TO263-7-3 | 4N03LH0 |

**Maximum ratings,** at $T_j$=25 °C, unless otherwise specified

| **Parameter** | **Symbol** | **Conditions** | **Value** | **Unit** |
|---|---|---|---|---|
| Continuous drain current | $I_D$ | $T_C$=25°C, $V_{GS}$=10V[1)] | 180 | A |
| | | $T_C$=100 °C, $V_{GS}$=10 V[2)] | 180 | |
| Pulsed drain current[2)] | $I_{D,pulse}$ | $T_C$=25 °C | 720 | |
| Avalanche energy, single pulse[2)] | $E_{AS}$ | $I_D$=90 A | 980 | mJ |
| Avalanche current, single pulse | $I_{AS}$ | - | 180 | A |
| Gate source voltage | $V_{GS}$ | - | ±16 | V |
| Power dissipation | $P_{tot}$ | $T_C$=25 °C | 250 | W |
| Operating and storage temperature | $T_j$, $T_{stg}$ | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Thermal characteristics**[2)] | | | | | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | - | 0.6 | K/W |
| SMD version, device on PCB | $R_{thJA}$ | minimal footprint | - | - | 62 | |
| | | 6 $cm^2$ cooling area[3)] | - | - | 40 | |
| **Electrical characteristics,** at $T_j$=25 °C, unless otherwise specified | | | | | | |
| **Static characteristics** | | | | | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}$=0 V, $I_D$= 1 mA | 30 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=200 µA | 1 | 1.5 | 2.2 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$=30 V, $V_{GS}$=0 V, $T_j$=25 °C | - | 0.01 | 1 | µA |
| | | $V_{DS}$=18 V, $V_{GS}$=0 V, $T_j$=85 °C[2)] | - | 5 | 60 | |
| Gate-source leakage current | $I_{GSS}$ | $V_{GS}$=16 V, $V_{DS}$=0 V | - | 1 | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=4.5 V, $I_D$=90 A | - | 0.95 | 1.30 | mΩ |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$=10 V, $I_D$=100 A | - | 0.73 | 0.95 | mΩ |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | |
| **Dynamic characteristics**[2] | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$=0 V, $V_{DS}$=25 V, $f$=1 MHz | - | 17500 | 23000 | pF |
| Output capacitance | $C_{oss}$ | | - | 3720 | 4800 | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 175 | 350 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$=15 V, $V_{GS}$=10 V, $I_D$=100 A, $R_G$=1.6 Ω | - | 9 | - | ns |
| Rise time | $t_r$ | | - | 7 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 60 | - | |
| Fall time | $t_f$ | | - | 25 | - | |
| **Gate Charge Characteristics**[2] | | | | | | |
| Gate to source charge | $Q_{gs}$ | $V_{DD}$=24 V, $I_D$=180 A, $V_{GS}$=0 to 10 V | - | 55 | 72 | nC |
| Gate to drain charge | $Q_{gd}$ | | - | 28 | 56 | |
| Gate charge total | $Q_g$ | | - | 230 | 300 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.1 | - | V |
| **Reverse Diode** | | | | | | |
| Diode continous forward current[2] | $I_S$ | $T_C$=25 °C | - | - | 180 | A |
| Diode pulse current[2] | $I_{S,pulse}$ | | - | - | 720 | |
| Diode forward voltage | $V_{SD}$ | $V_{GS}$=0 V, $I_F$=100 A, $T_j$=25 °C | - | 0.9 | 1.3 | V |
| Reverse recovery time[2] | $t_{rr}$ | $V_R$=20 V, $I_F$=100A, $di_F/dt$=100 A/µs | - | 250 | - | ns |
| Reverse recovery charge[2] | $Q_{rr}$ | | - | 280 | - | nC |

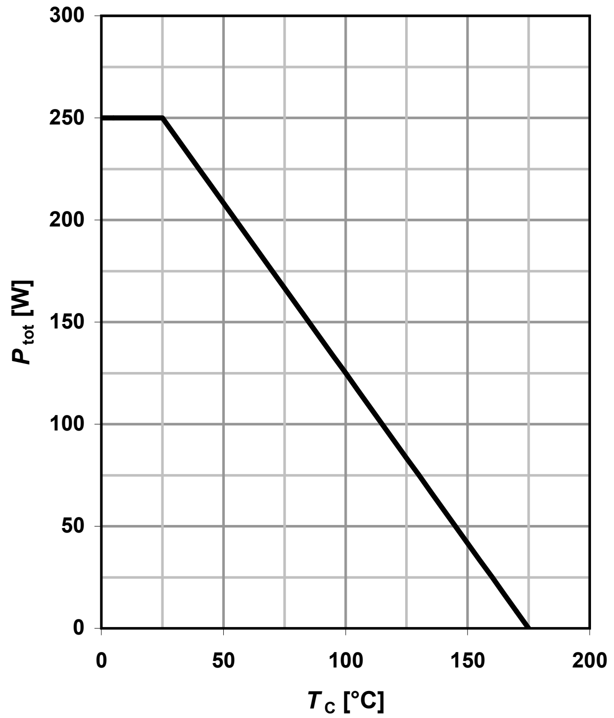
[1] Current is limited by bondwire; with an $R_{thJC}$ = 0.6 K/W the chip is able to carry 400A at 25°C.

[2] Defined by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 $cm^2$ (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

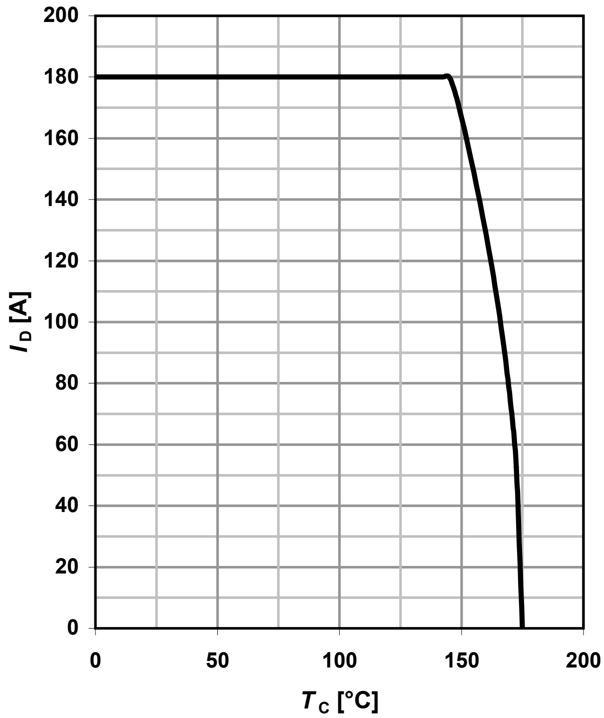
**1 Power dissipation**

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V




**2 Drain current**

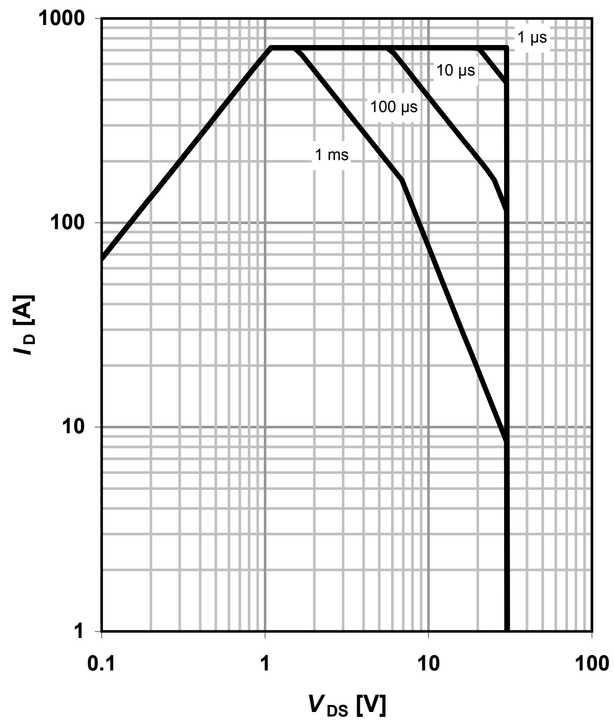
$I_D = f(T_C)$; $V_{GS} \geq 6$ V




**3 Safe operating area**

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

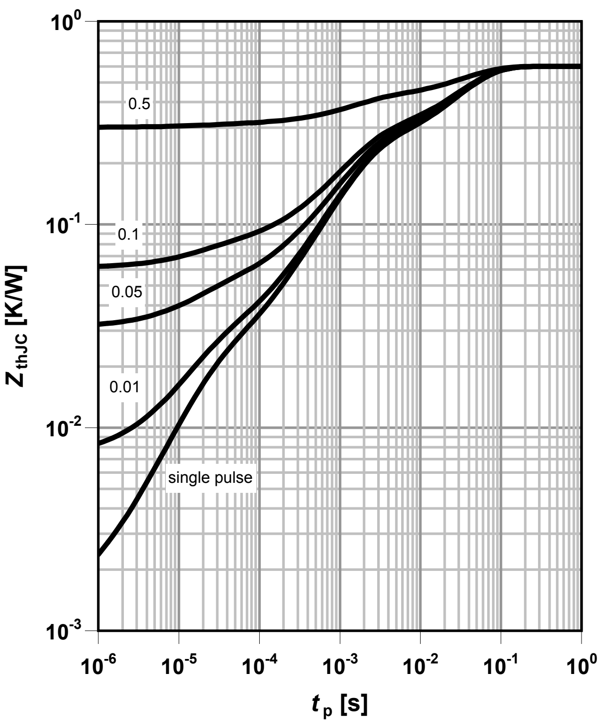
parameter: $t_p$




**4 Max. transient thermal impedance**

$Z_{thJC} = f(t_p)$

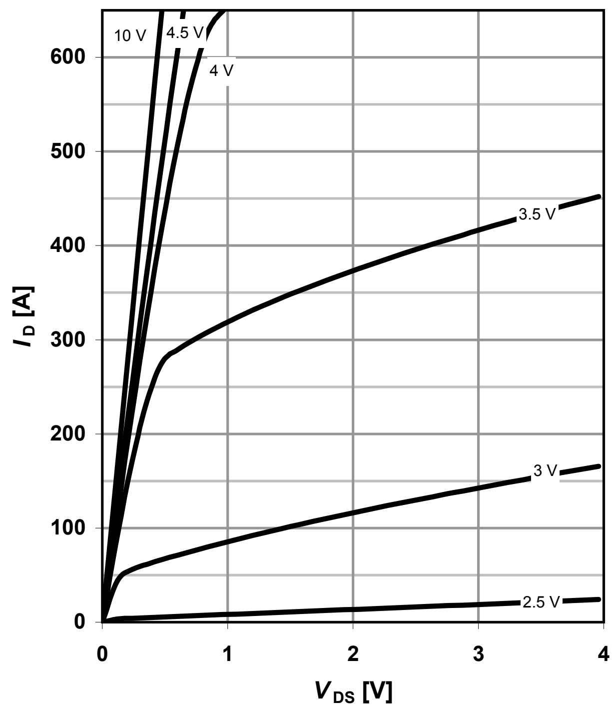
parameter: $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS})$; $T_j = 25\ °C$

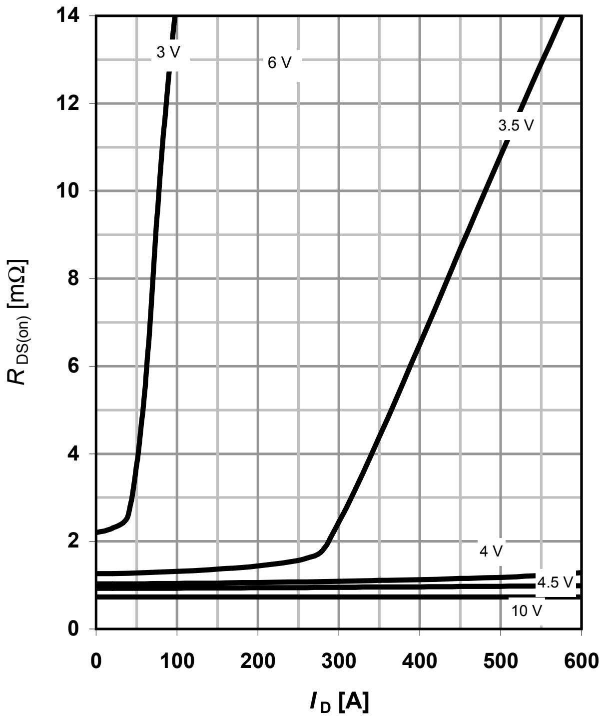
parameter: $V_{GS}$




**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = (I_D)$; $T_j = 25\ °C$

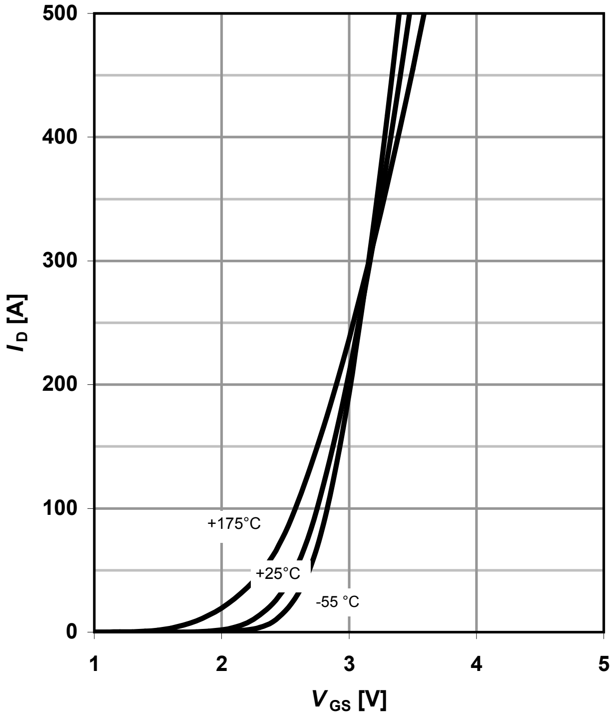
parameter: $V_{GS}$




**7 Typ. transfer characteristics**

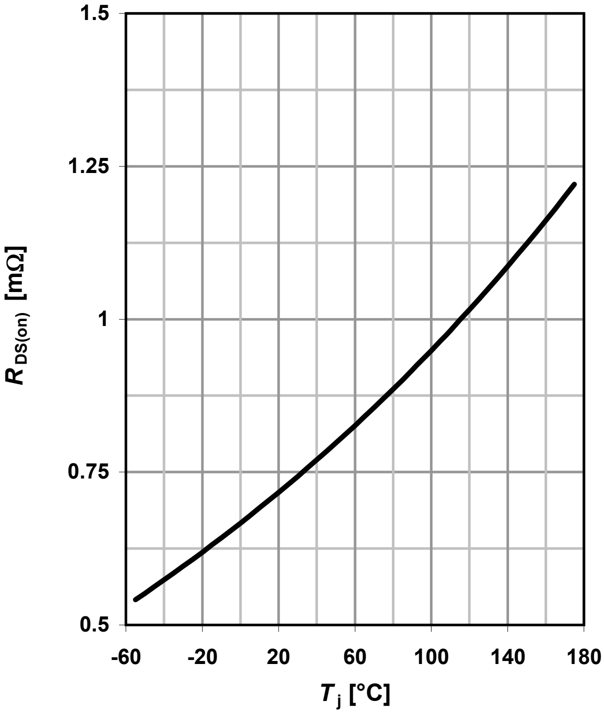
$I_D = f(V_{GS})$; $V_{DS} = 6V$

parameter: $T_j$




**8 Typ. drain-source on-state resistance**

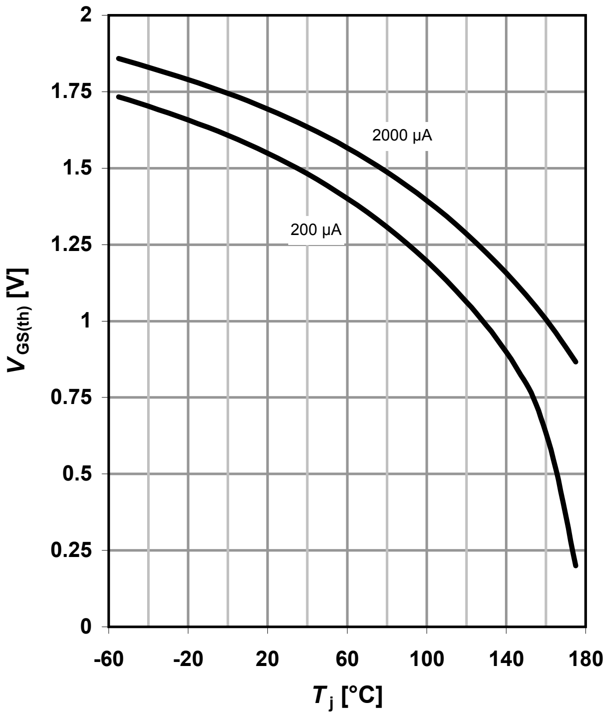
$R_{DS(on)} = f(T_j)$; $I_D = 80\ A$; $V_{GS} = 10\ V$



**9 Typ. gate threshold voltage**

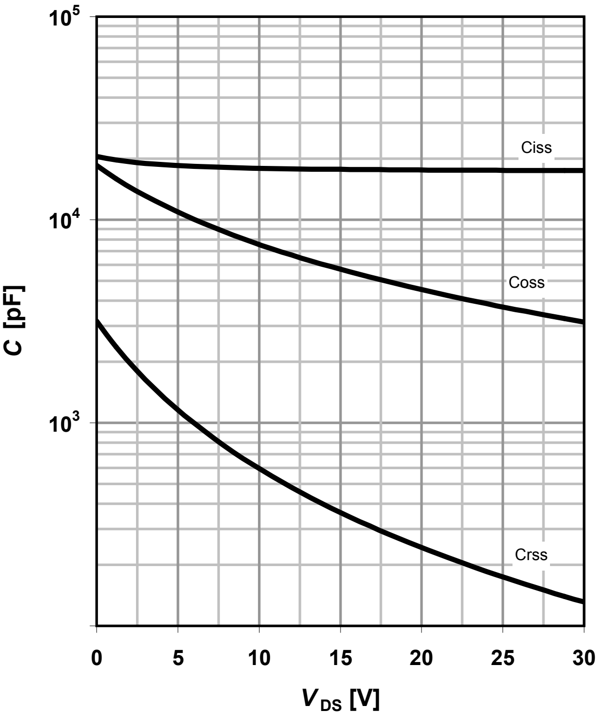
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: $I_D$




**10 Typ. capacitances**

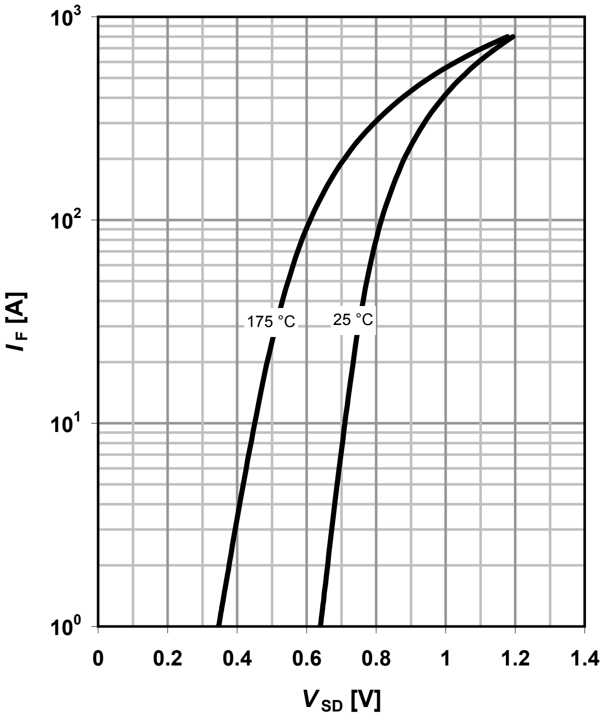
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz




**11 Typical forward diode characteristicis**

IF = f($V_{SD}$)

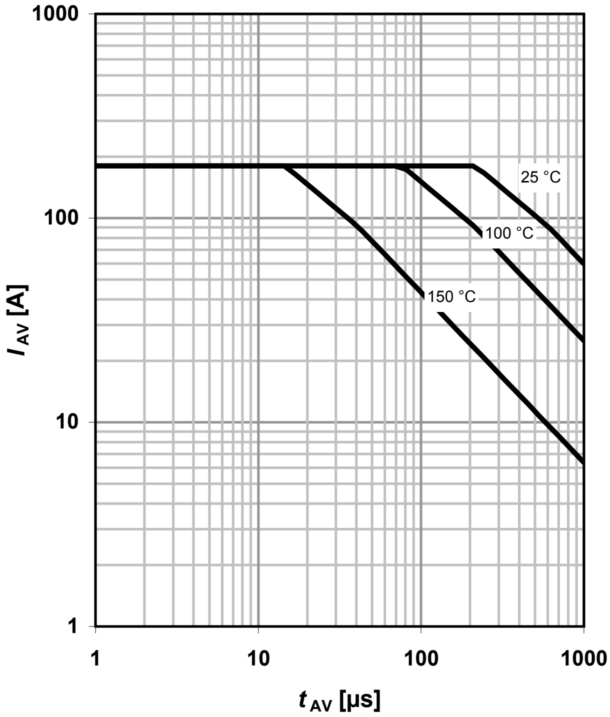
parameter: $T_j$




**12 Typ. avalanche characteristics**

$I_{AS} = f(t_{AV})$

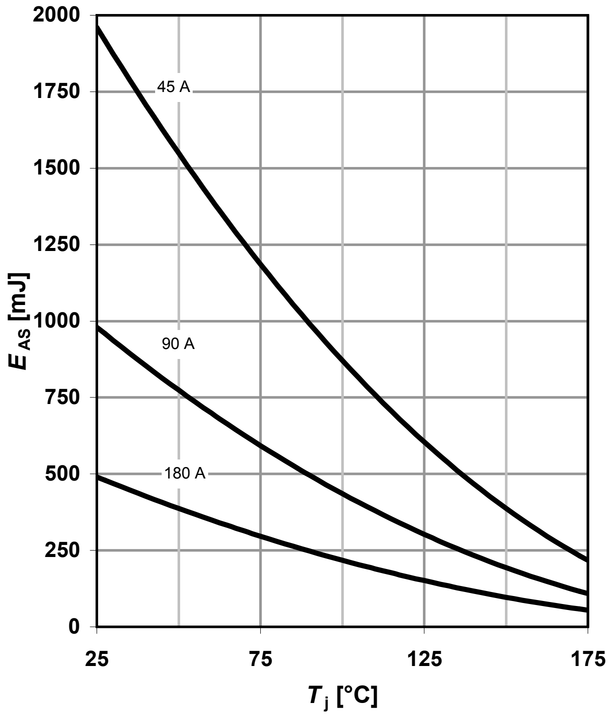
parameter: $T_{j(start)}$



**13 Typical avalanche energy**

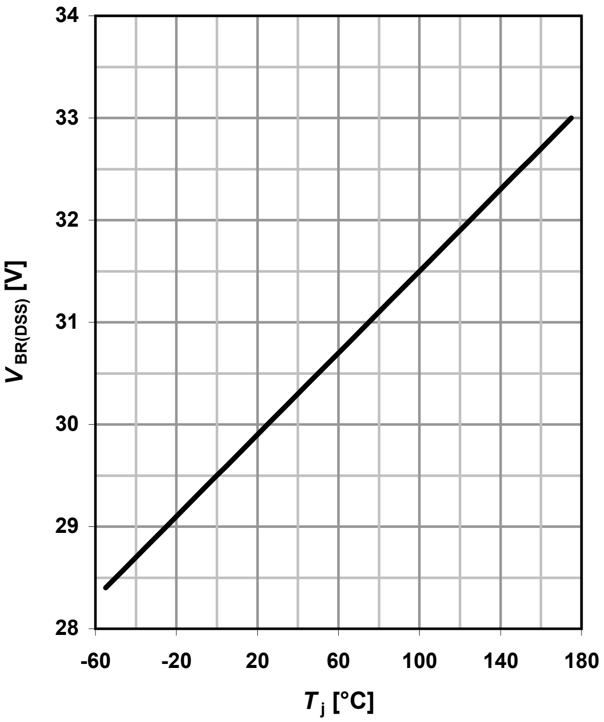
$E_{AS} = f(T_j)$

parameter: $I_D$




**14 Drain-source breakdown voltage**

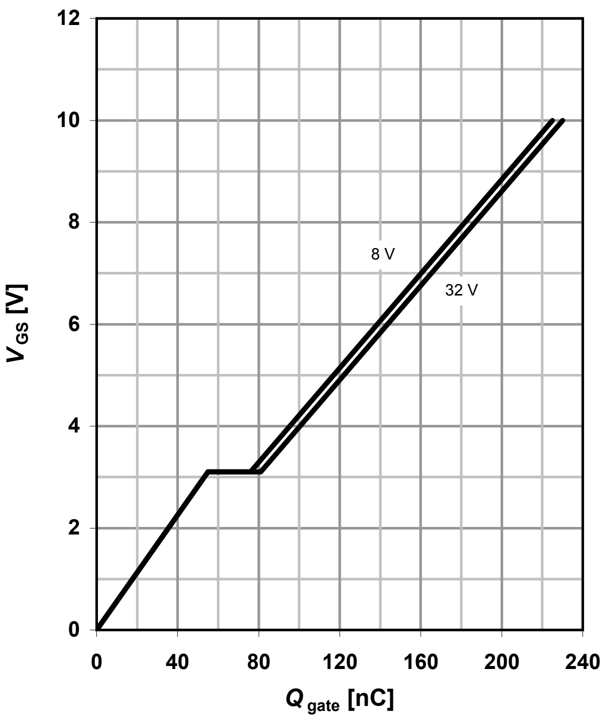
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



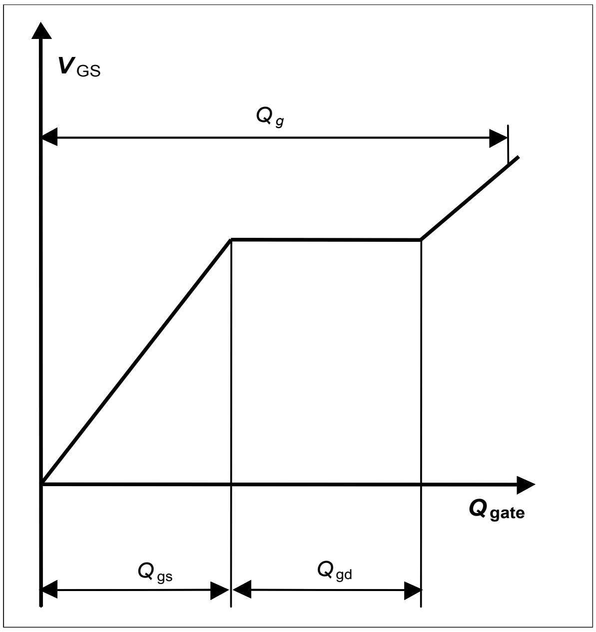

**15 Typ. gate charge**

$V_{GS} = f(Q_{gate})$; $I_D = 180$ A pulsed

parameter: $V_{DD}$




**16 Gate charge waveforms**



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Revision History

| **Version** | Date | Changes |
|---|---|---|
| | | |