

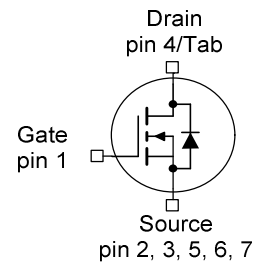
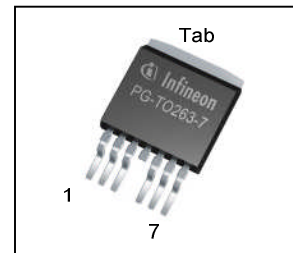
OptiMOS[®]-T2 Power-Transistor

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	1.9	m Ω
I_D	160	A

Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (ELV compliant 100% lead free)
- 100% Avalanche tested
- Ultra low $R_{DS(on)}$
- Ultra high I_D

PG-TO263-7-3


Type	Package	Marking
IPB160N04S4-02D	PG-TO263-7-3	4N0402D

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{V}^{1)}$	160	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}^{2)}$	157	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	640	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=80\text{A}$	220	mJ
Avalanche current, single pulse	I_{AS}	-	160	A
Gate source voltage	V_{GS}	-	± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	231	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	0.65	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=70\mu A$	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40V, V_{GS}=0V, T_j=25\text{ °C}$	-	0.03	1	μA
		$V_{DS}=18V, V_{GS}=0V, T_j=85\text{ °C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=100A$	-	1.4	1.9	m Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	5500	7150	pF
Output capacitance	C_{oss}		-	1310	1700	
Reverse transfer capacitance	C_{rss}		-	45	90	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V,$ $I_D=160A, R_G=3.5\Omega$	-	16	-	ns
Rise time	t_r		-	22	-	
Turn-off delay time	$t_{d(off)}$		-	17	-	
Fall time	t_f		-	25	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32V, I_D=160A,$ $V_{GS}=0 \text{ to } 10V$	-	30	40	nC
Gate to drain charge	Q_{gd}		-	9	21	
Gate charge total	Q_g		-	70	90	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$	-	-	160	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	640	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=100A,$ $T_j=25^\circ C$	-	0.85	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$	-	50	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	50	-	nC

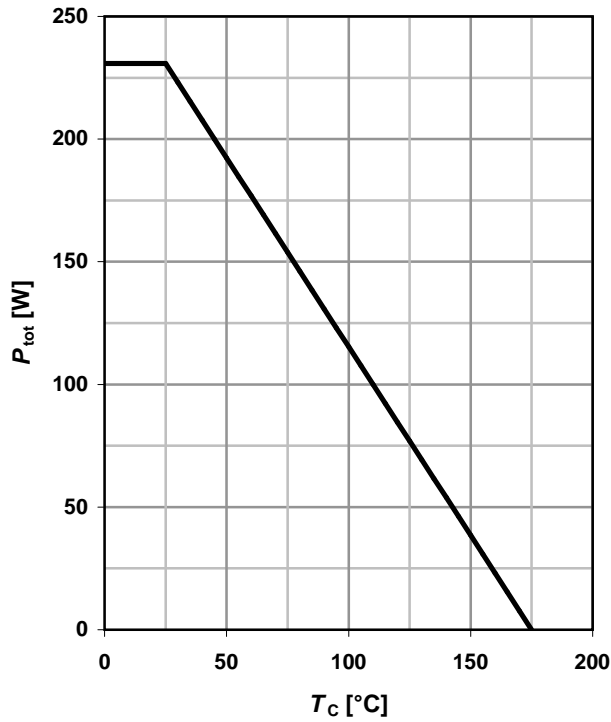
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.65K/W$ the chip is able to carry 269A at 25°C.

²⁾ Specified by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

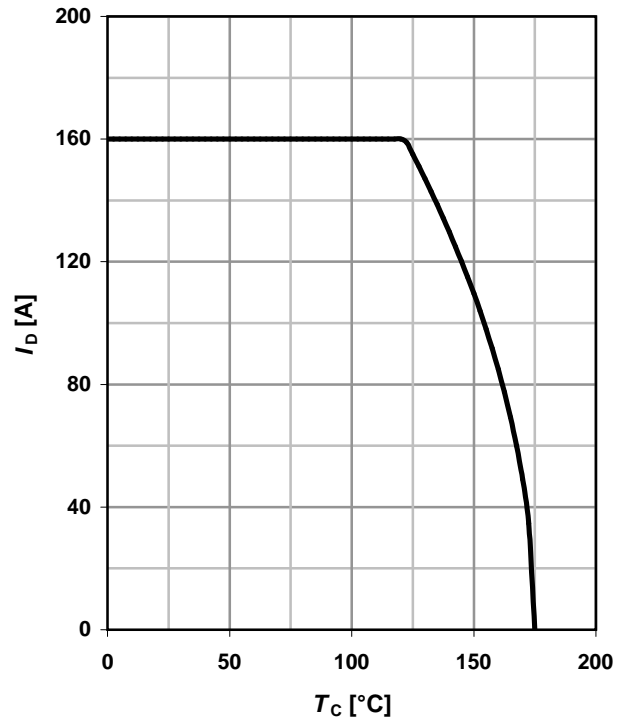
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 V$



2 Drain current

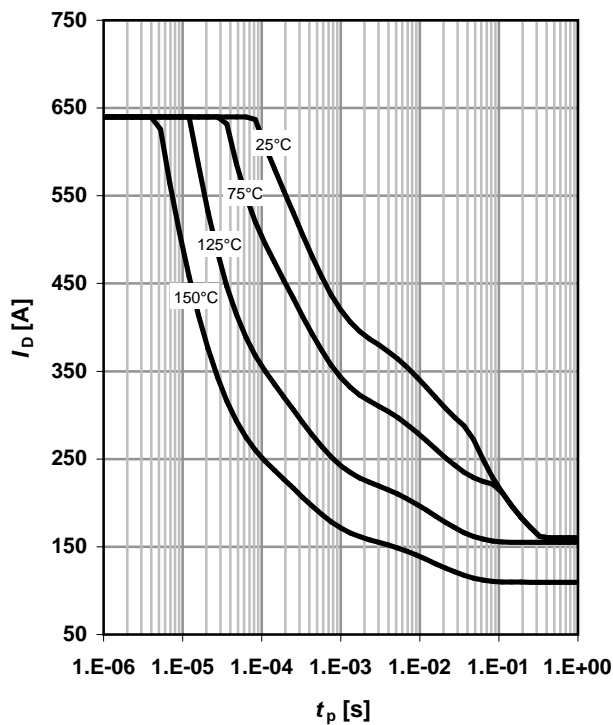
$I_D = f(T_C); V_{GS} \geq 6 V$



3 Safe operating area

$I_D = f(t_p); V_{GS} = 10V; D = 0$

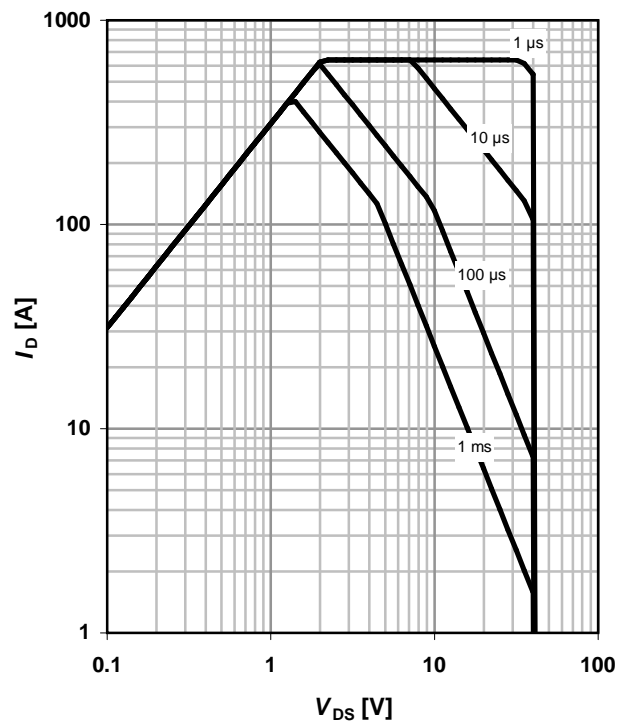
parameter: T_C



4 Safe operating area

$I_D = f(V_{DS}); T_C = 25 °C; D = 0$

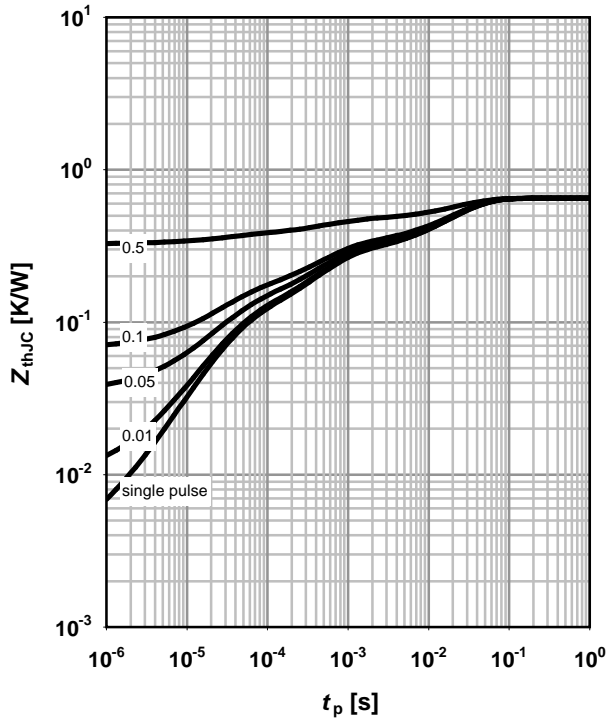
parameter: t_p



5 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

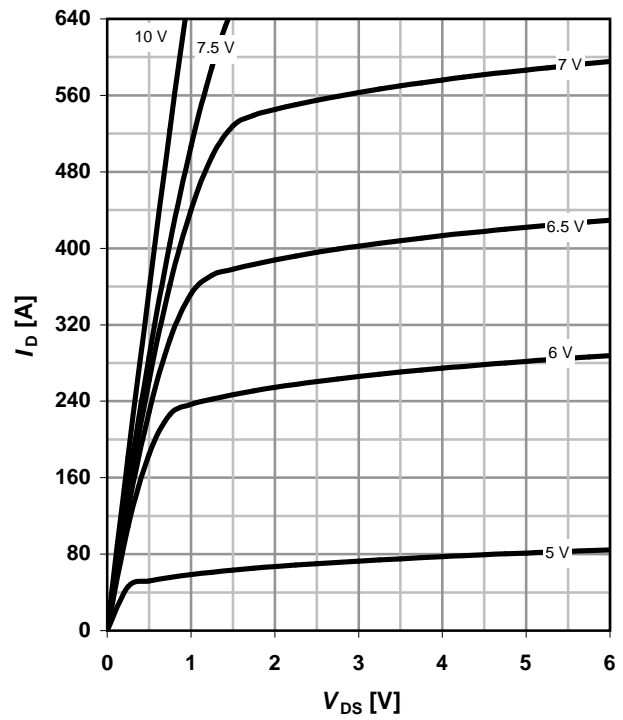
parameter: $D = t_p / T$



6 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

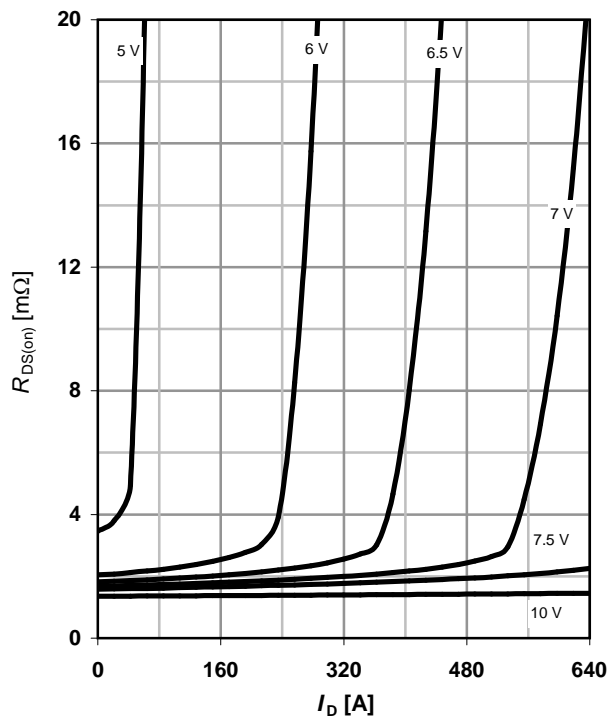
parameter: V_{GS}



7 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

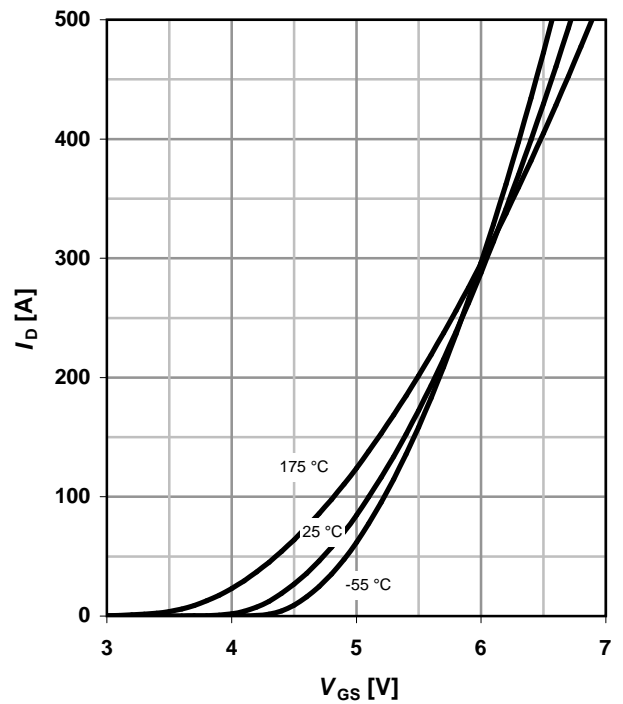
parameter: V_{GS}



8 Typ. transfer characteristics

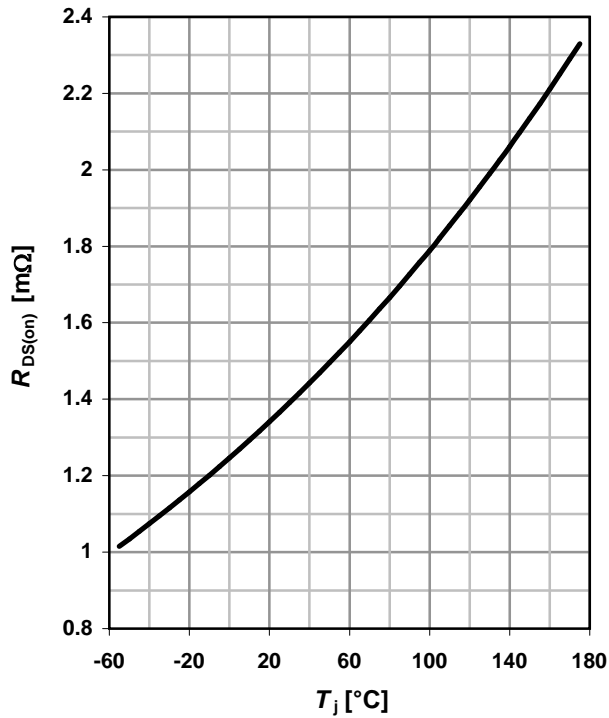
$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

parameter: T_j



9 Typ. drain-source on-state resistance

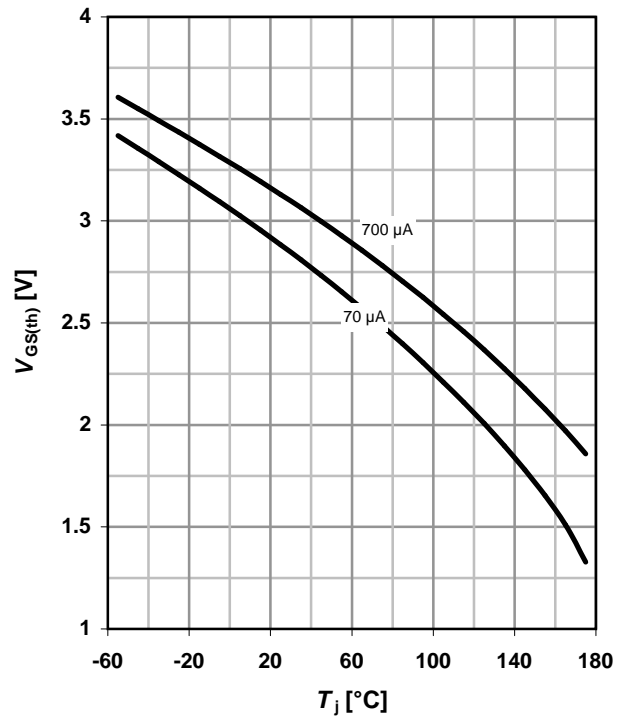
$R_{DS(on)} = f(T_j); I_D = 100 \text{ A}; V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

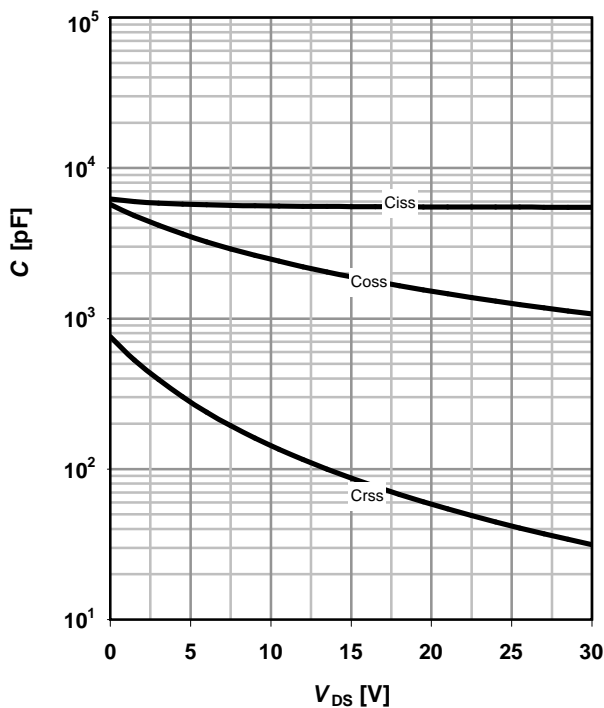
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

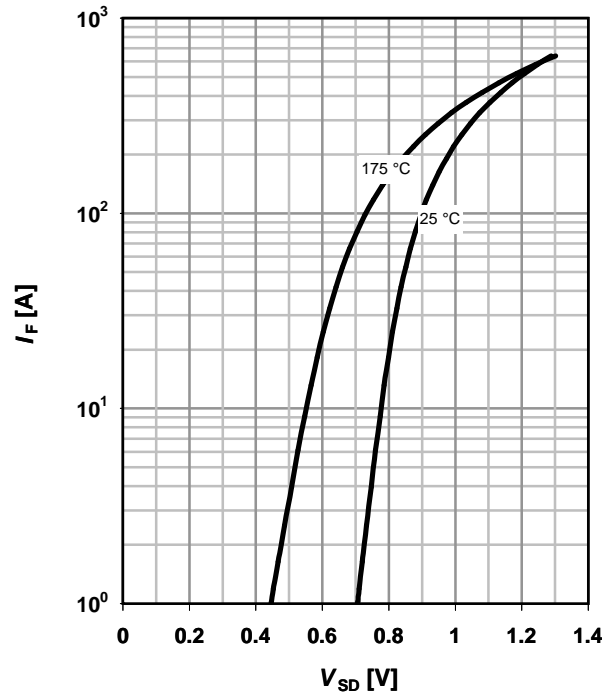
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Typical forward diode characteristics

$I_F = f(V_{SD})$

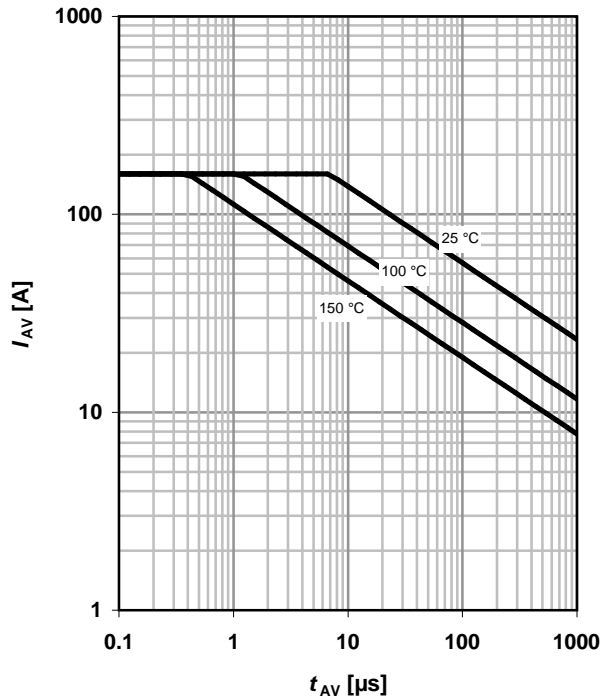
parameter: T_j



13 Avalanche characteristics

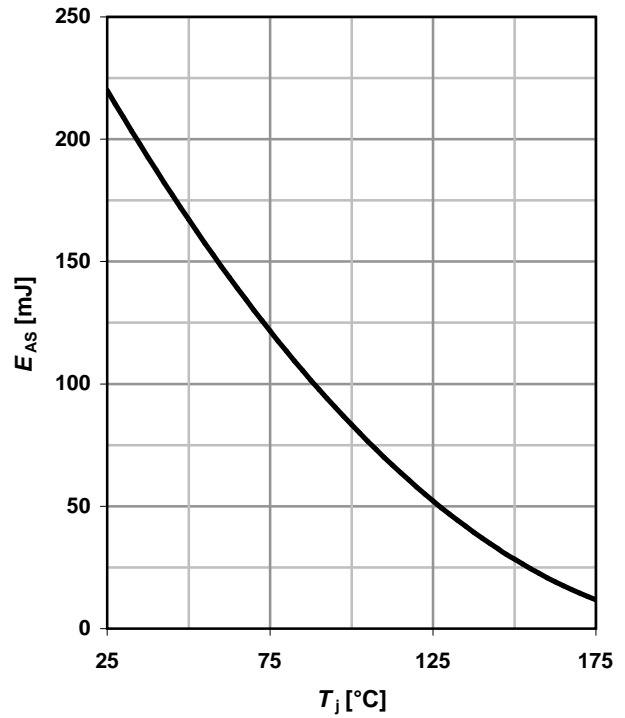
$I_{AS} = f(t_{AV})$

parameter: $T_{j(\text{start})}$



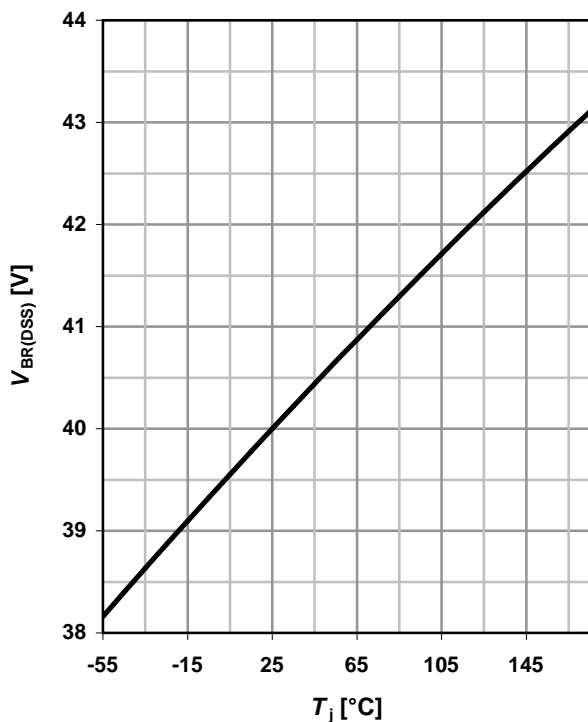
14 Avalanche energy

$E_{AS} = f(T_j); I_D = 80 \text{ A}$



15 Drain-source breakdown voltage

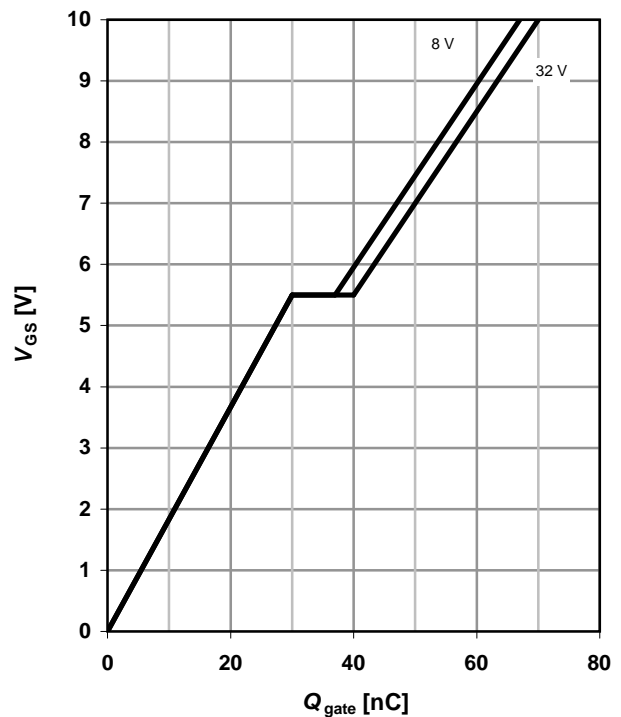
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



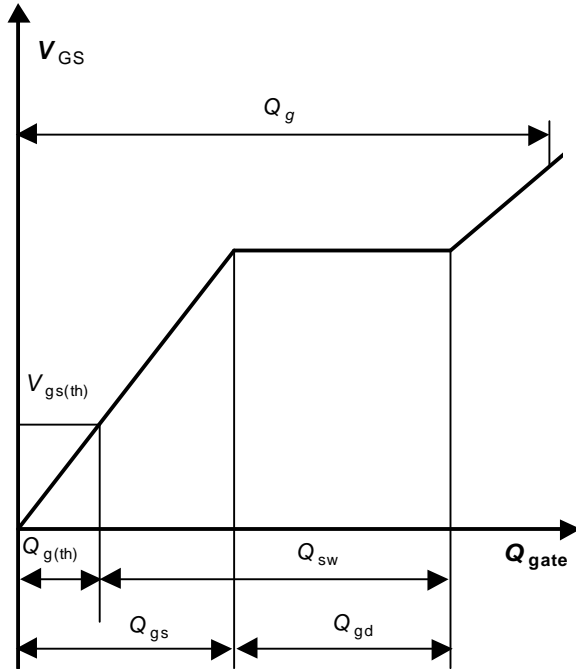
16 Typ. gate charge

$V_{GS} = f(Q_{\text{gate}}); I_D = 160 \text{ A pulsed}$

parameter: V_{DD}



17 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	23.09.2011	Final Data Sheet