

MOSFET

StrongIRFET™2 Power-Transistor, 40 V

Features

- Optimized for wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

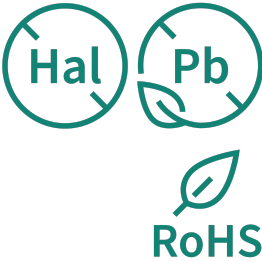
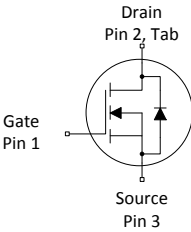
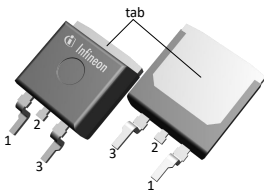
Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	1.15	mΩ
I_D	201	A
Q_{oss}	233	nC
$Q_G(0V..10V)$	210	nC

D²PAK



Type/Ordering Code	Package	Marking	Related Links
IPB011N04NF2S	PG-TO263-3	011N04NS	-



Table of Contents

Description 1

Maximum ratings 3

Thermal characteristics 4

Electrical characteristics 5

Electrical characteristics diagrams 7

Package Outlines 11

Revision History 12

Trademarks 12

Disclaimer 12

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	201 156 43	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	804	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	1112	mJ	$I_D=100\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	375 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.4	V	$V_{DS}=V_{GS}$, $I_D=249\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.74 0.82	1.15 1.21	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$
Gate resistance	R_G	-	2.5	-	Ω	-
Transconductance ⁶⁾	g_{fs}	245	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

⁶⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	14900	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	5460	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	272	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	27	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	51	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	90	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	40	-	ns	$V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	62	-	nC	$V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	42	-	nC	$V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	39	-	nC	$V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	59	-	nC	$V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ⁸⁾	Q_g	-	210	315	nC	$V_{DD}=20\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate plateau voltage	V_{plateau}	-	4.1	-	V	$V_{\text{DD}}=20\text{ V}$, $I_{\text{D}}=100\text{ A}$, $V_{\text{GS}}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{\text{g(sync)}}$	-	187	-	nC	$V_{\text{DS}}=0.1\text{ V}$, $V_{\text{GS}}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	233	-	nC	$V_{\text{DS}}=20\text{ V}$, $V_{\text{GS}}=0\text{ V}$

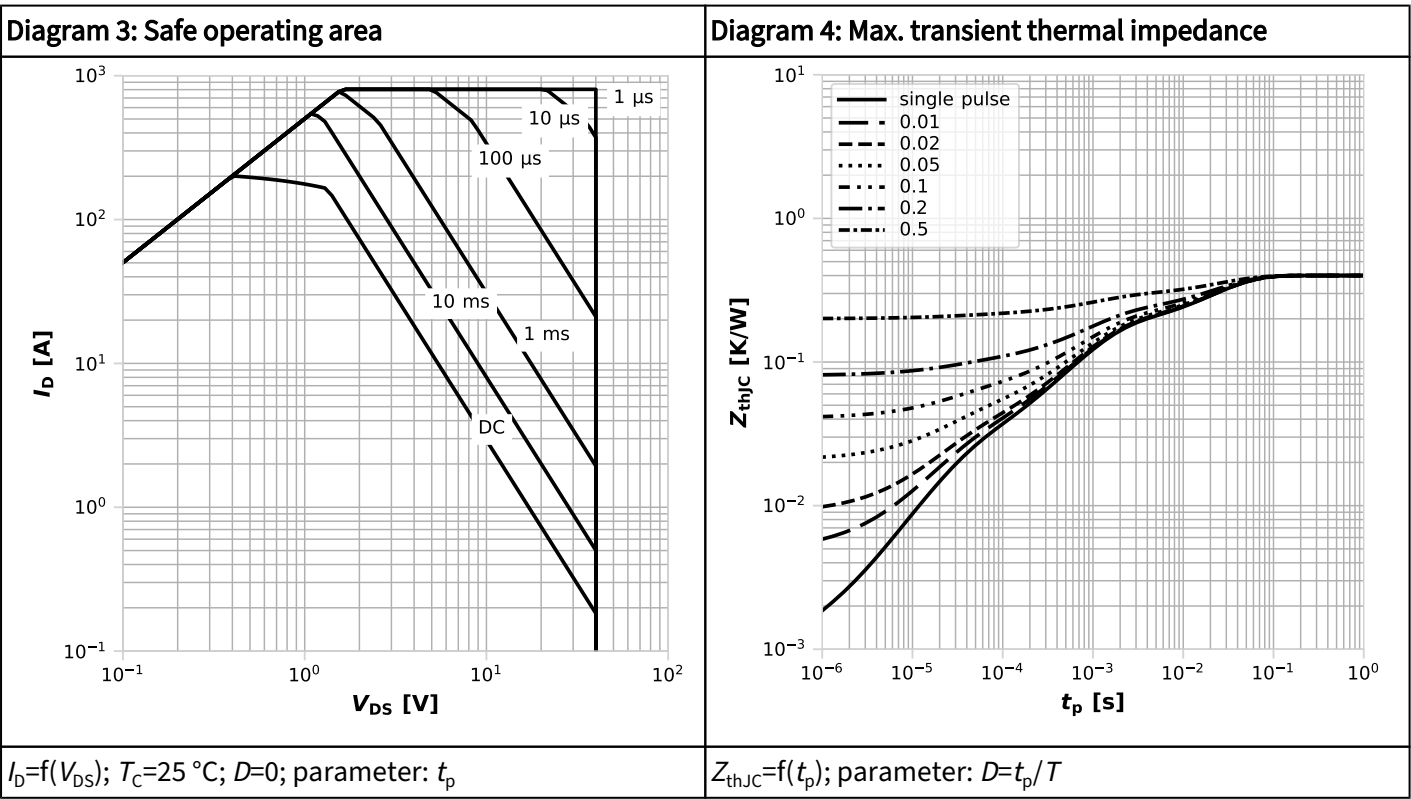
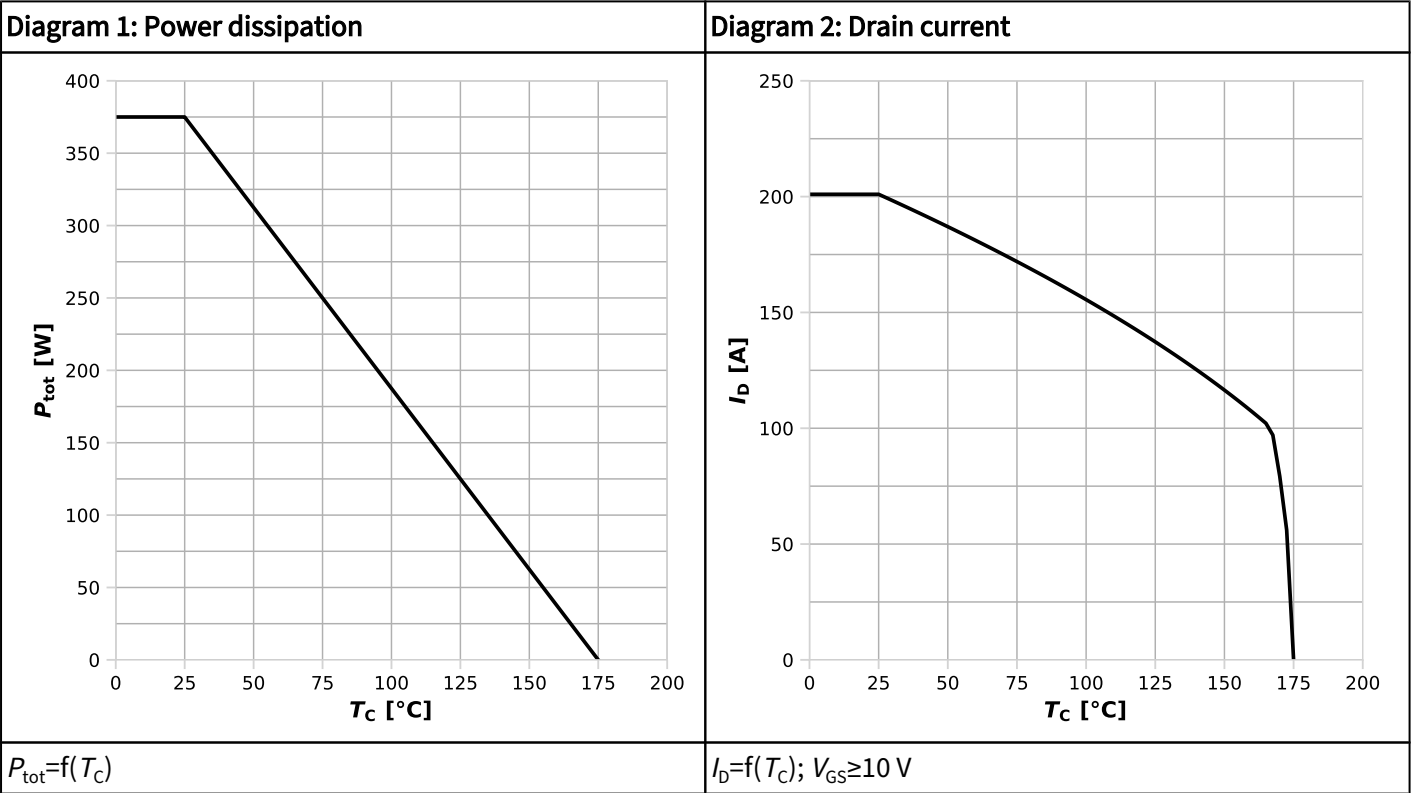
⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_{S}	-	-	169	A	$T_{\text{C}}=25\text{ °C}$
Diode pulse current	$I_{\text{S,pulse}}$	-	-	804	A	$T_{\text{C}}=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.82	1	V	$V_{\text{GS}}=0\text{ V}$, $I_{\text{F}}=100\text{ A}$, $T_{\text{J}}=25\text{ °C}$
Reverse recovery time	t_{rr}	-	61	-	ns	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=100\text{ A}$, $di_{\text{F}}/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	76	-	nC	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=100\text{ A}$, $di_{\text{F}}/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time	t_{rr}	-	51	-	ns	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=100\text{ A}$, $di_{\text{F}}/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	289	-	nC	$V_{\text{R}}=20\text{ V}$, $I_{\text{F}}=100\text{ A}$, $di_{\text{F}}/dt=500\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams



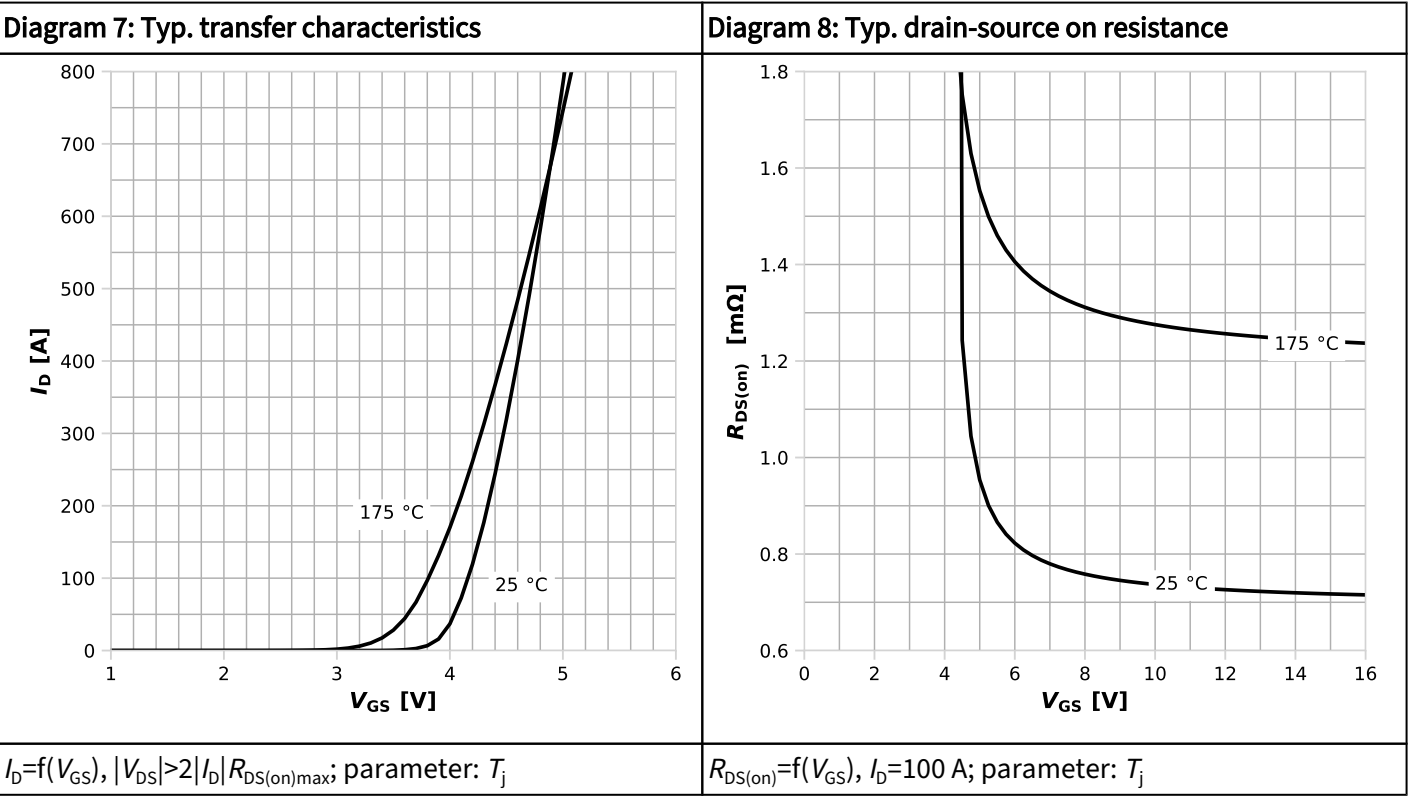
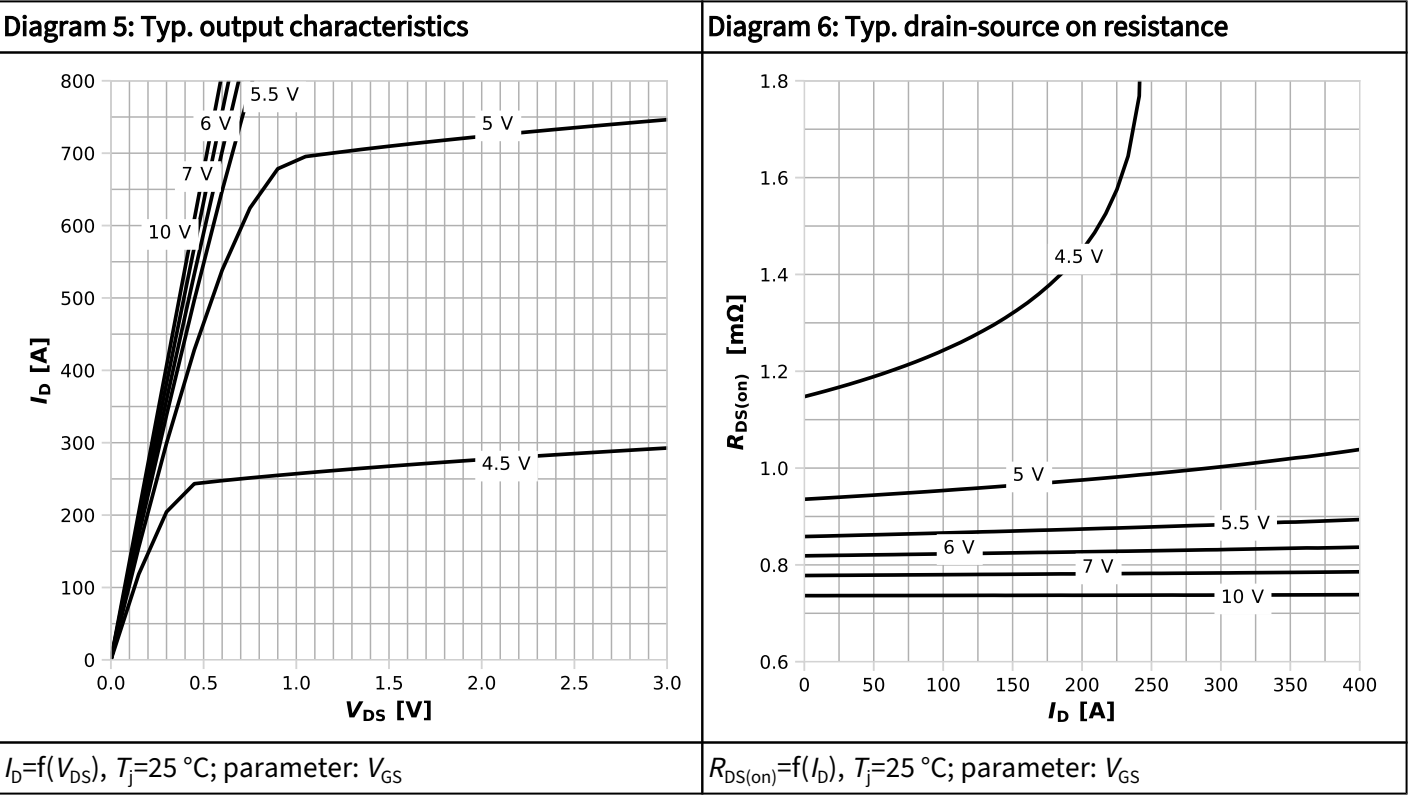
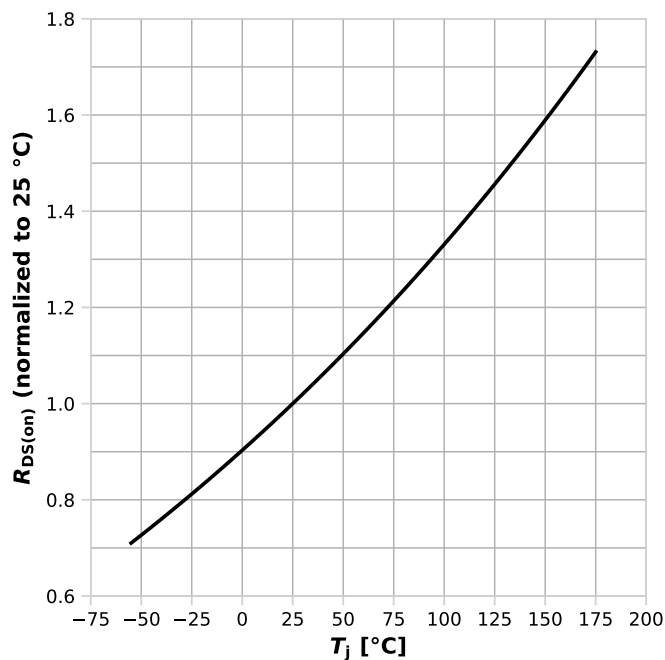
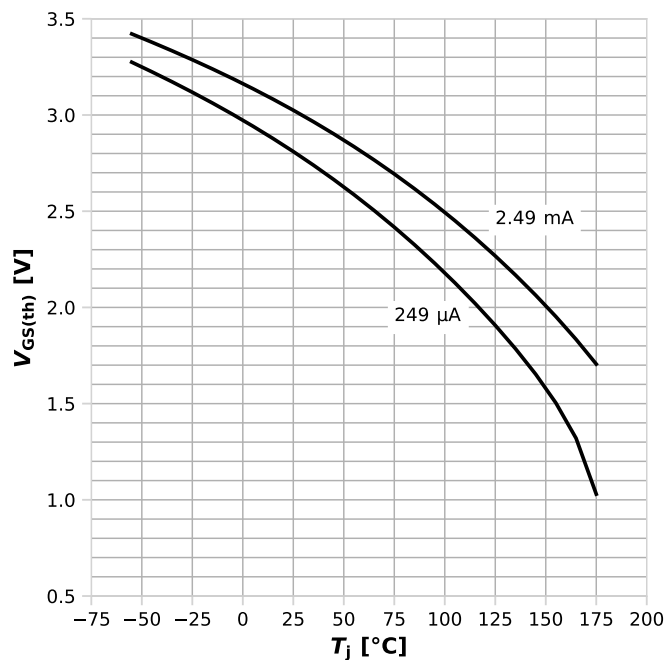
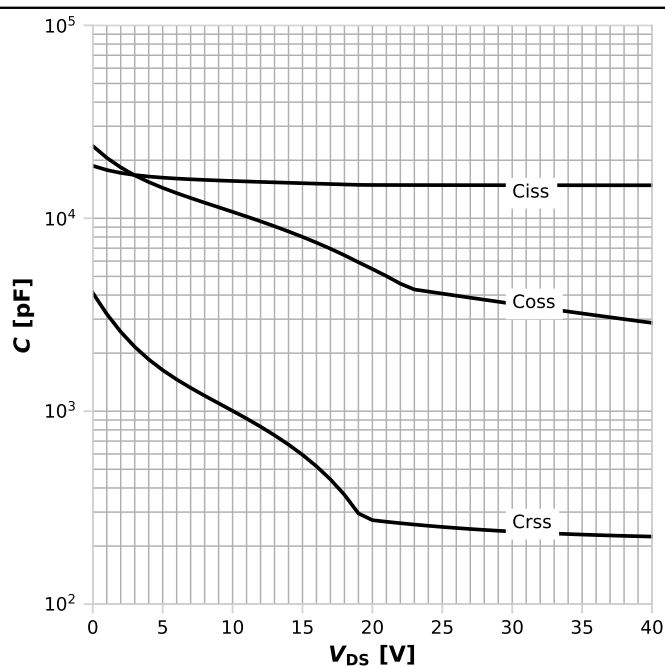


Diagram 9: Normalized drain-source on resistance


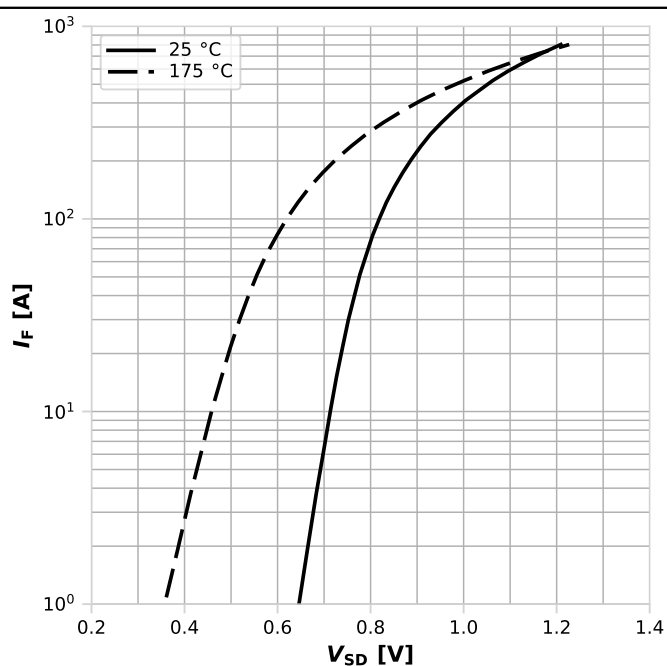
$$R_{DS(on)} = f(T_j), I_D = 100 \text{ A}, V_{GS} = 10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage


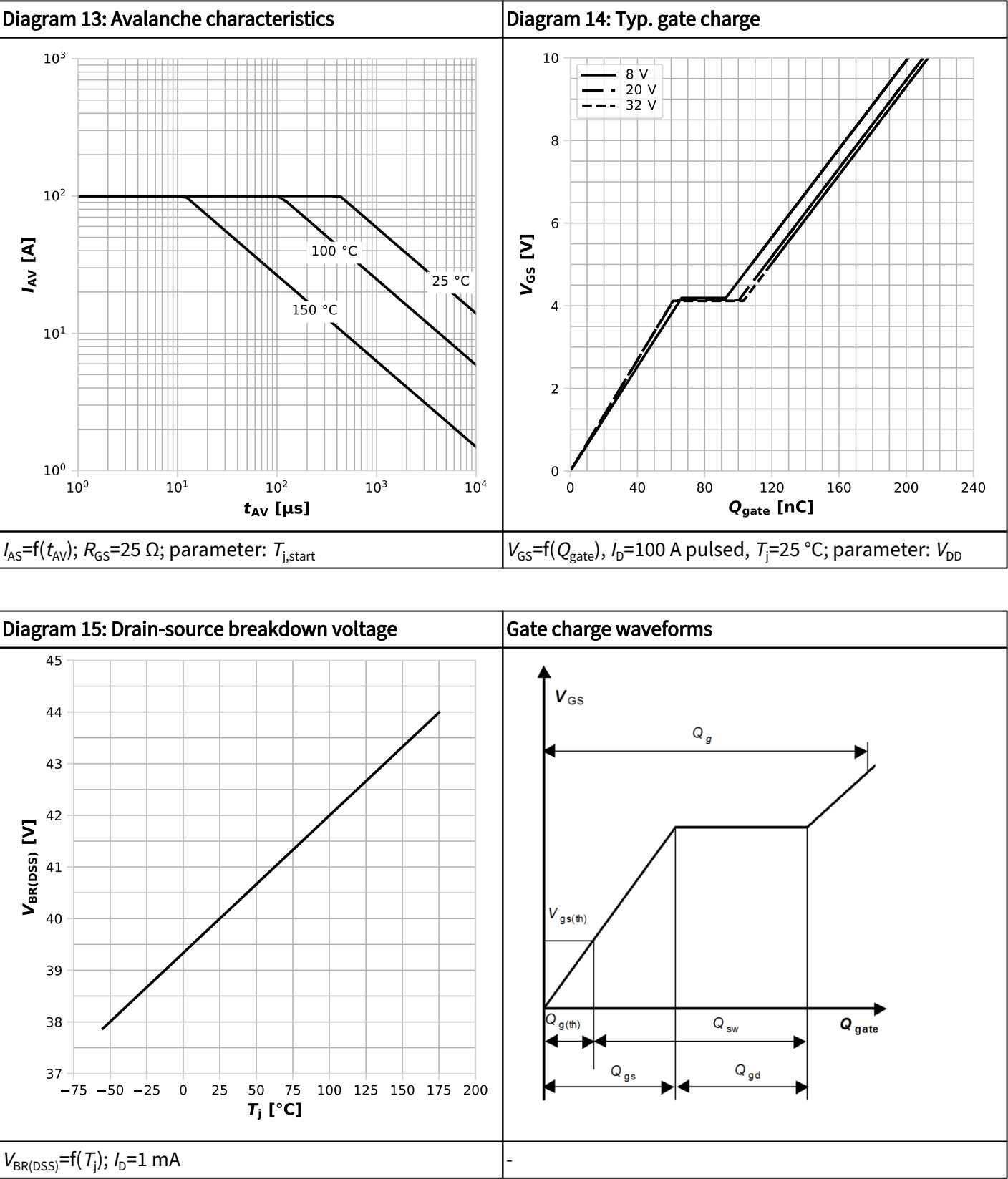
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances


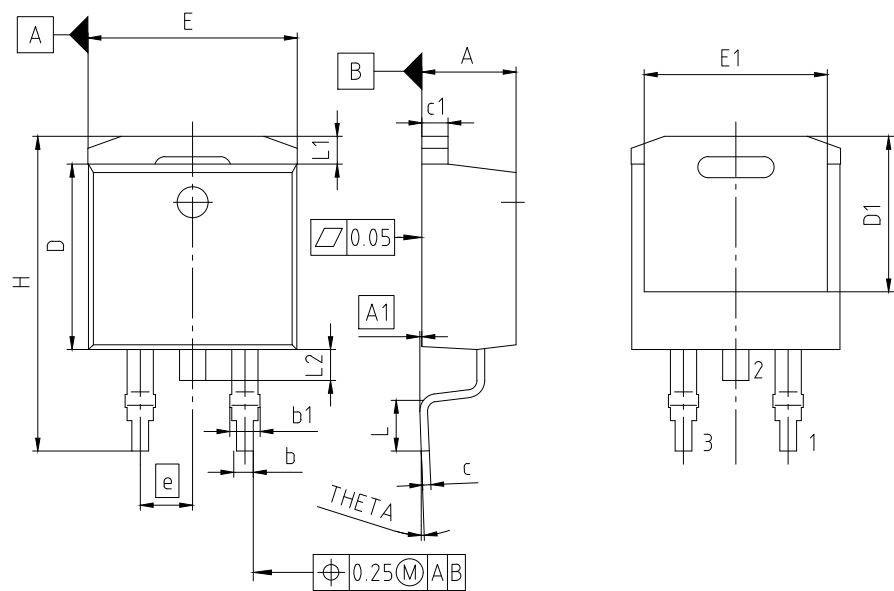
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Typ. forward characteristics of reverse diode


$$I_F = f(V_{SD}); \text{ parameter: } T_j$$



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-T0263-3-U02		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.06	4.83
A1	0.00	0.25
b	0.51	1.00
b1	1.07	1.78
c	0.30	0.73
c1	1.14	1.65
D	8.38	9.65
D1	6.60	7.50
E	9.65	10.67
E1	6.22	8.70
e	2.54	
N	3	
H	14.60	15.88
L	1.52	2.60
L1	1.05	1.68
L2	1.35	1.78
THETA	-9.00°	8.00°

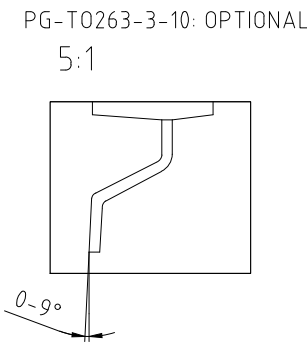


Figure 1 Outline PG-T0263-3, dimensions in mm

Revision History

IPB011N04NF2S

Revision 2024-10-14, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-10-12	Release of final version
2.1	2024-10-14	Added trr and Qrr at diF/dt=100 A/μs

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