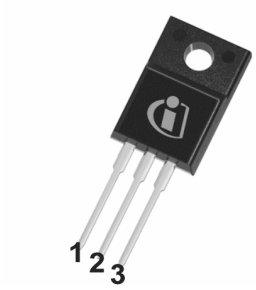
# MOSFET

## StrongIRFET™ 2 Power-Transistor

PG-TO 220 FP

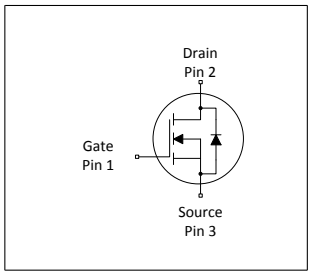



### Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

### Product validation

Qualified according to JEDEC Standard




### Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ | 100 | V |
| $R_{DS(on),max}$ | 8.2 | mΩ |
| $I_D$ | 46 | A |
| $Q_{oss}$ | 38 | nC |
| $Q_G$ | 28 | nC |

| Type / Ordering Code | Package | Marking | Related Links |
|---|---|---|---|
| IPA082N10NF2S | PG-TO220 FullPAK | 082N10NS | - |

## Table of Contents

# 1 Maximum ratings

at $T_A$=25 °C, unless otherwise specified

### Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current[1] | $I_D$ | -<br>- | -<br>- | 46<br>32 | A | $V_{GS}$=10 V, $T_C$=25 °C<br>$V_{GS}$=10 V, $T_C$=100 °C |
| Pulsed drain current[2] | $I_{D,pulse}$ | - | - | 184 | A | $T_A$=25 °C |
| Avalanche energy, single pulse[3] | $E_{AS}$ | - | - | 80 | mJ | $I_D$=40 A, $R_{GS}$=25 Ω |
| Gate source voltage | $V_{GS}$ | -20 | - | 20 | V | - |
| Power dissipation | $P_{tot}$ | - | - | 35 | W | $T_C$=25 °C |
| Operating and storage temperature | $T_j$, $T_{stg}$ | -55 | - | 175 | °C | IEC climatic category; DIN IEC 68-1: 55/175/56 |

# 2 Thermal characteristics

### Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 4.3 | °C/W | - |

# 3 Electrical characteristics

at $T_j$=25 °C, unless otherwise specified

### Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}$=0 V, $I_D$=1 mA |
| Gate threshold voltage | $V_{GS(th)}$ | 2.2 | 3.0 | 3.8 | V | $V_{DS}$=$V_{GS}$, $I_D$=46 µA |
| Zero gate voltage drain current | $I_{DSS}$ | -<br>- | 0.1<br>10 | 1.0<br>100 | µA | $V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=25 °C<br>$V_{DS}$=100 V, $V_{GS}$=0 V, $T_j$=125 °C |
| Gate-source leakage current | $I_{GSS}$ | - | 10 | 100 | nA | $V_{GS}$=20 V, $V_{DS}$=0 V |
| Drain-source on-state resistance[4] | $R_{DS(on)}$ | -<br>- | 7.3<br>8.9 | 8.2<br>10.3 | mΩ | $V_{GS}$=10 V, $I_D$=30 A<br>$V_{GS}$=6 V, $I_D$=15 A |
| Gate resistance | $R_G$ | - | 1.1 | - | Ω | - |
| Transconductance[5] | $g_{fs}$ | 31 | - | - | S | \|$V_{DS}$\|≥2\|$I_D$\|$R_{DS(on)max}$, $I_D$=30 A |

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] See Diagram 3 for more detailed information
[3] See Diagram 13 for more detailed information
[4] $R_{DS(on)}$ is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.
[5] Defined by design. Not subject to production test.

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 2000 | - | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Output capacitance | $C_{oss}$ | - | 320 | - | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 15 | - | pF | $V_{GS}$=0 V, $V_{DS}$=50 V, $f$=1 MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 11 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Rise time | $t_r$ | - | 20 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 16 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |
| Fall time | $t_f$ | - | 5 | - | ns | $V_{DD}$=50 V, $V_{GS}$=10 V, $I_D$=30 A, $R_{G,ext}$=1.6 Ω |

## Table 6 Gate charge characteristics[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 9.3 | - | nC | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Gate charge at threshold | $Q_{g(th)}$ | - | 6.0 | - | nC | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Gate to drain charge | $Q_{gd}$ | - | 6.0 | - | nC | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Switching charge | $Q_{sw}$ | - | 9.3 | - | nC | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Gate charge total[2)] | $Q_g$ | - | 28 | 42 | nC | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Gate plateau voltage | $V_{plateau}$ | - | 4.7 | - | V | $V_{DD}$=50 V, $I_D$=30 A, $V_{GS}$=0 to 10 V |
| Output charge | $Q_{oss}$ | - | 38 | - | nC | $V_{DS}$=50 V, $V_{GS}$=0 V |

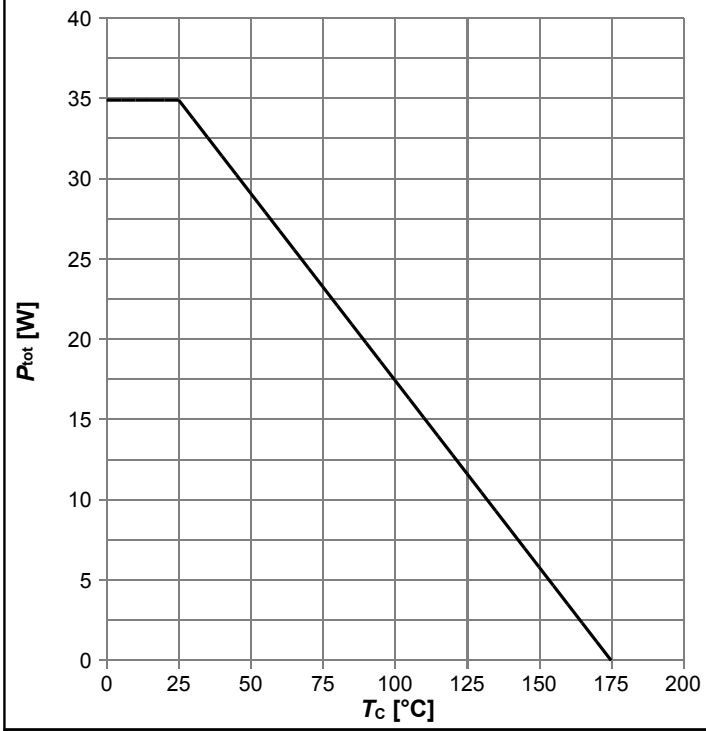
## Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | $I_S$ | - | - | 26 | A | $T_C$=25 °C |
| Diode pulse current | $I_{S,pulse}$ | - | - | 184 | A | $T_C$=25 °C |
| Diode forward voltage | $V_{SD}$ | - | 0.83 | 1.2 | V | $V_{GS}$=0 V, $I_F$=15 A, $T_j$=25 °C |
| Reverse recovery time | $t_{rr}$ | - | 49 | - | ns | $V_R$=50 V, $I_F$=15 A, d$i_F$/d$t$=100 A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 67 | - | nC | $V_R$=50 V, $I_F$=15 A, d$i_F$/d$t$=100 A/µs |

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test.

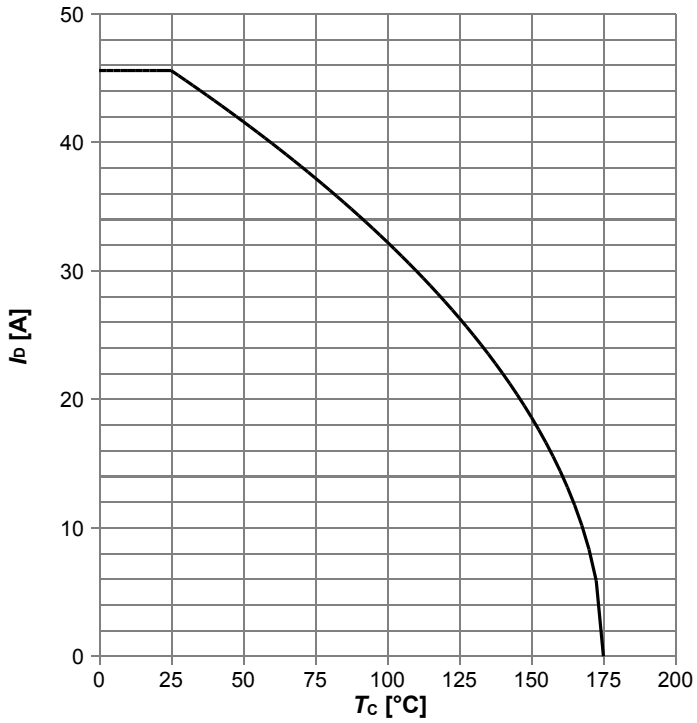
# 4 Electrical characteristics diagrams

**Diagram 1: Power dissipation**



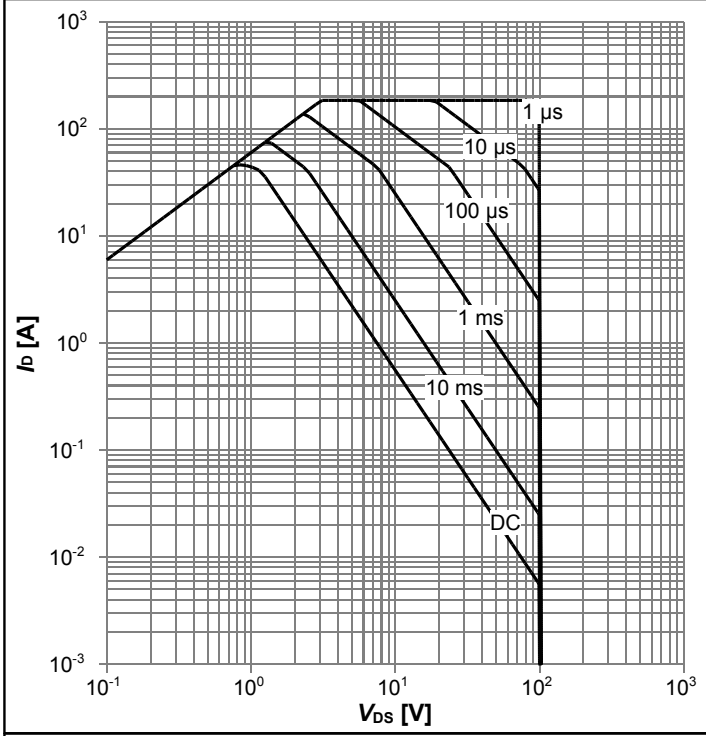

$P_{tot}=f(T_C)$

**Diagram 2: Drain current**



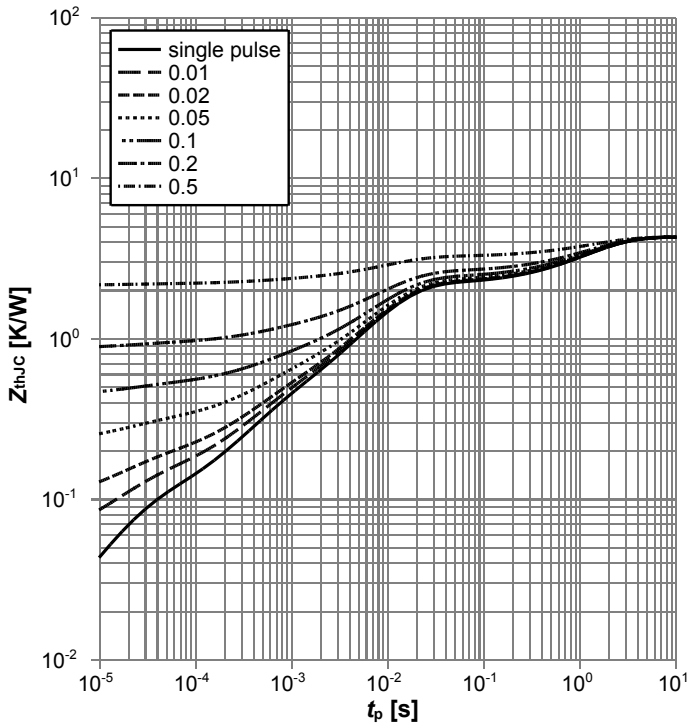

$I_D=f(T_C)$; $V_{GS}\geq 10$ V

**Diagram 3: Safe operating area**



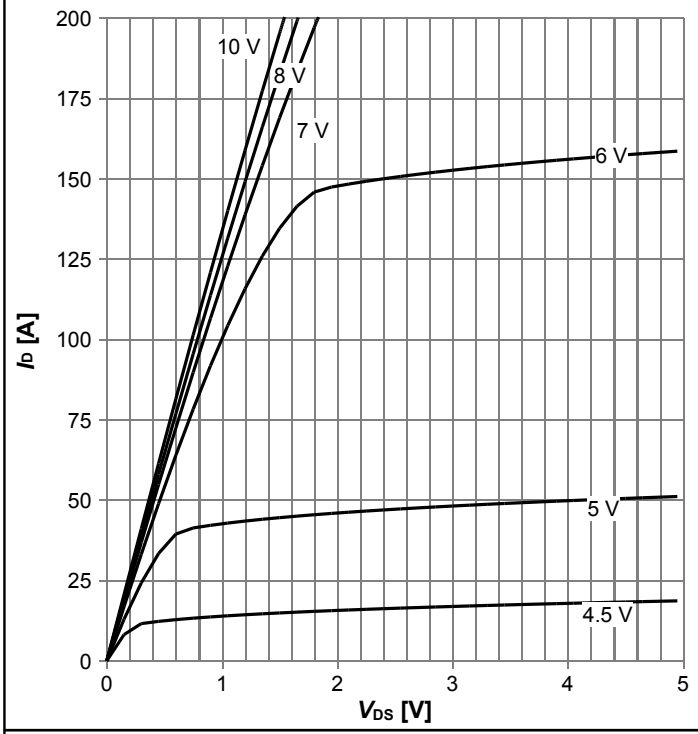

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: $t_p$

**Diagram 4: Max. transient thermal impedance**



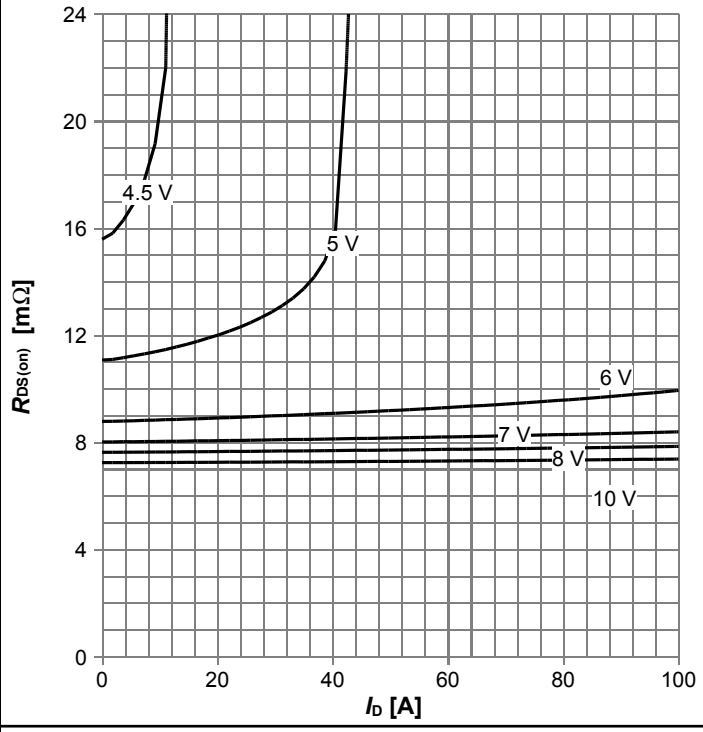

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

**Diagram 5: Typ. output characteristics**



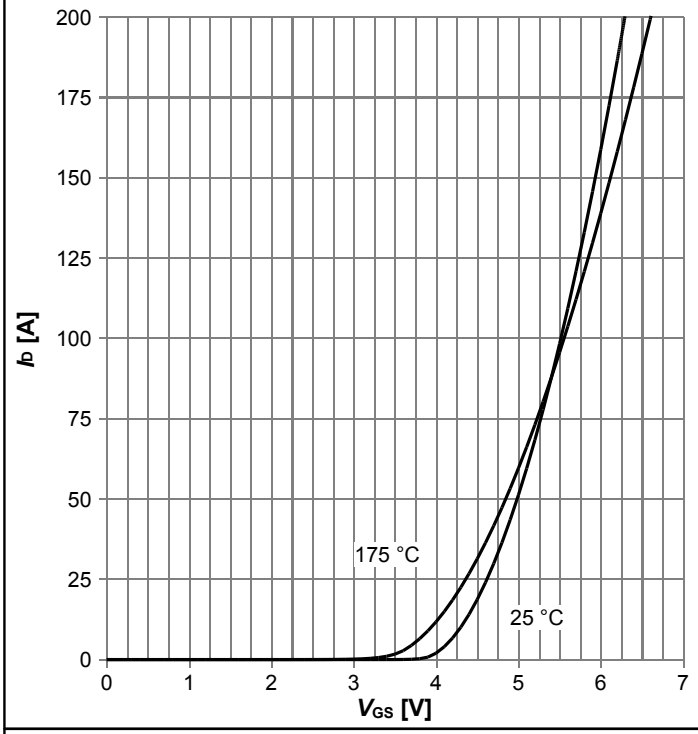

$I_D$=f($V_{DS}$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 6: Typ. drain-source on resistance**



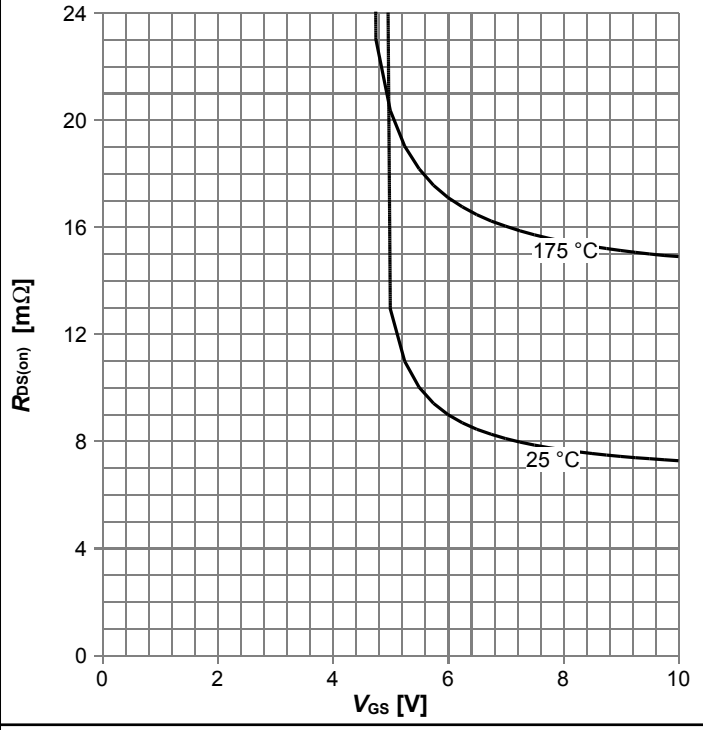

$R_{DS(on)}$=f($I_D$), $T_j$=25 °C; parameter: $V_{GS}$

**Diagram 7: Typ. transfer characteristics**



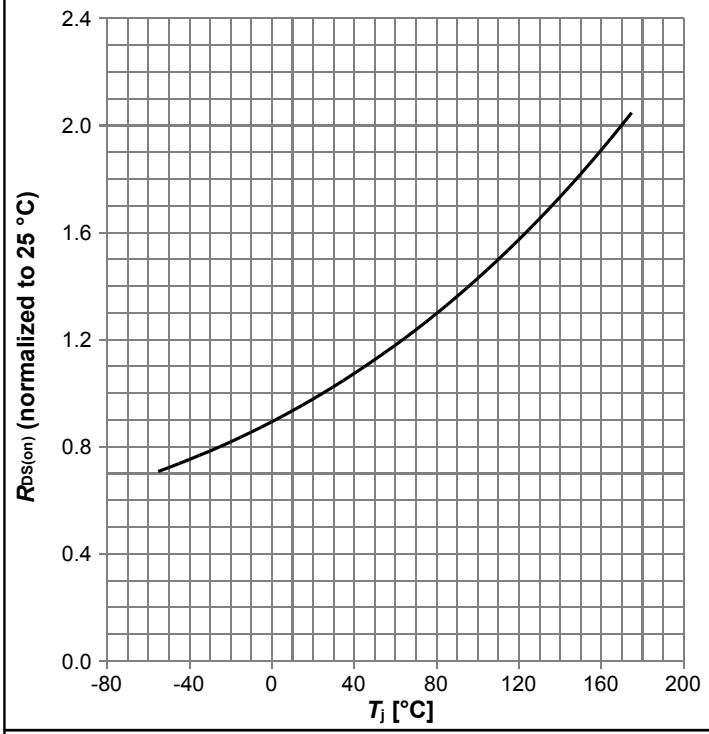

$I_D$=f($V_{GS}$), |$V_{DS}$|>2|$I_D$|$R_{DS(on)max}$; parameter: $T_j$

**Diagram 8: Typ. drain-source on resistance**



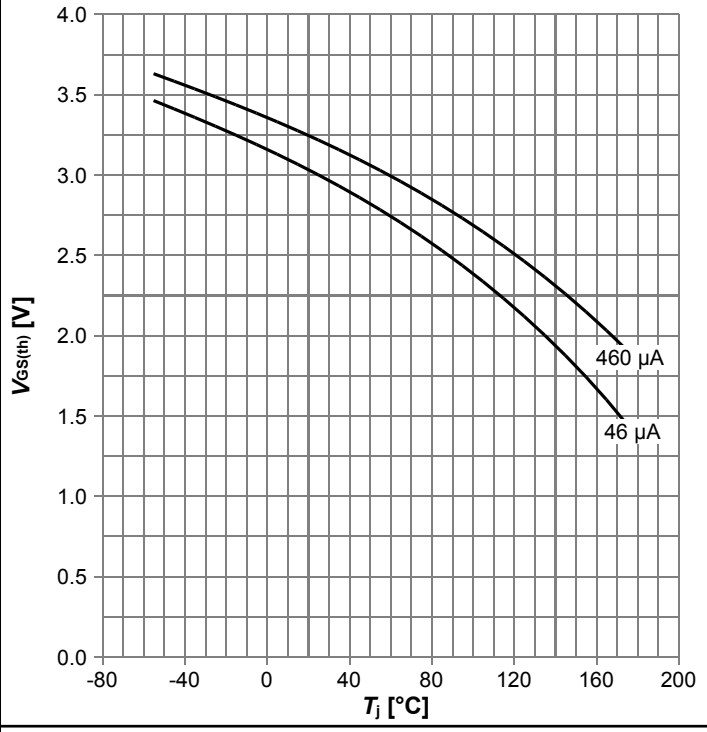

$R_{DS(on)}$=f($V_{GS}$), $I_D$=30 A; parameter: $T_j$

**Diagram 9: Normalized drain-source on resistance**



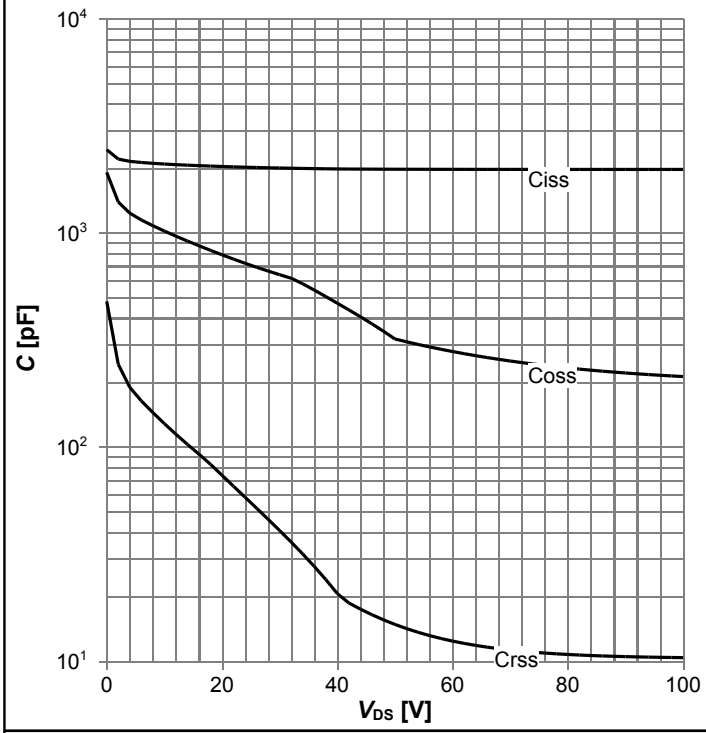

$R_{DS(on)}$=f($T_j$), $I_D$=30 A, $V_{GS}$=10 V

**Diagram 10: Typ. gate threshold voltage**



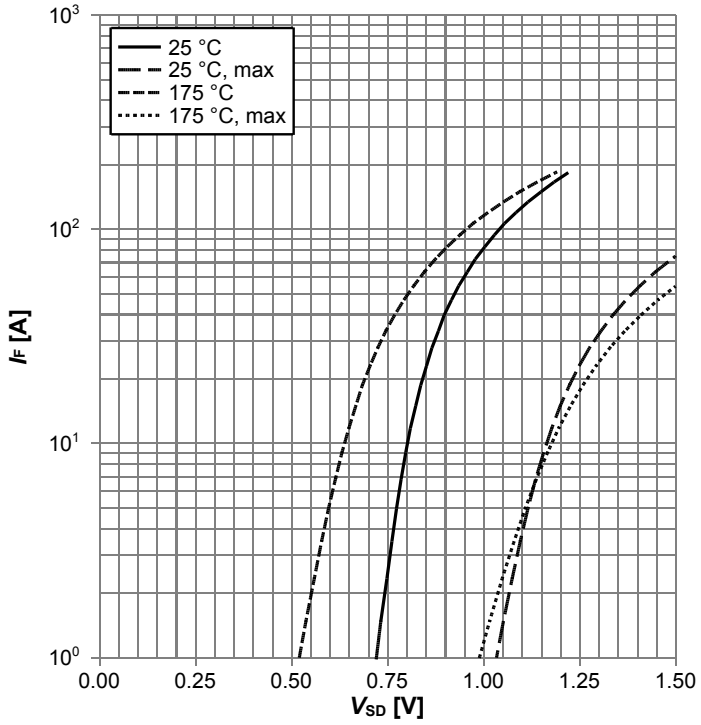

$V_{GS(th}$=f($T_j$), $V_{GS}$=$V_{DS}$; parameter: $I_D$

**Diagram 11: Typ. capacitances**



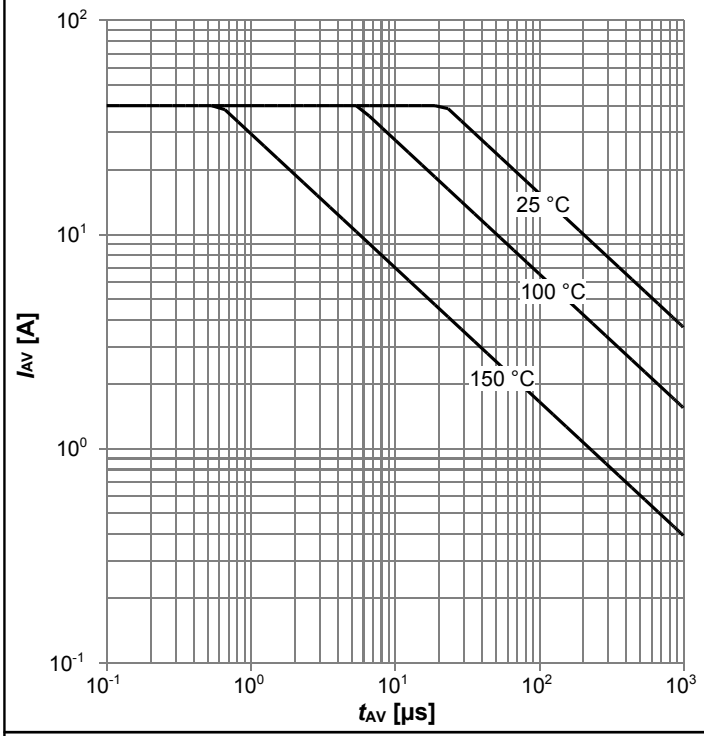

$C$=f($V_{DS}$); $V_{GS}$=0 V; $f$=1 MHz

**Diagram 12: Forward characteristics of reverse diode**



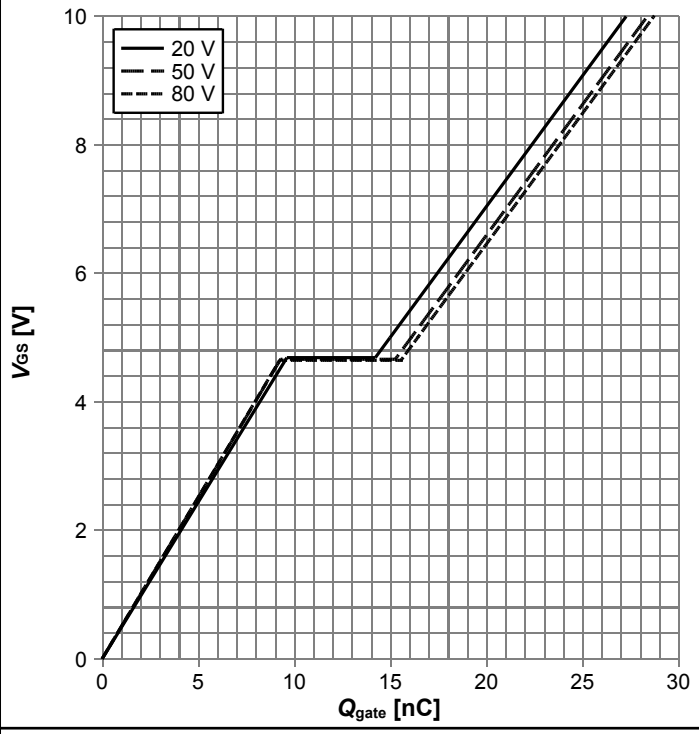

$I_F$=f($V_{SD}$); parameter: $T_j$

**Diagram 13: Avalanche characteristics**



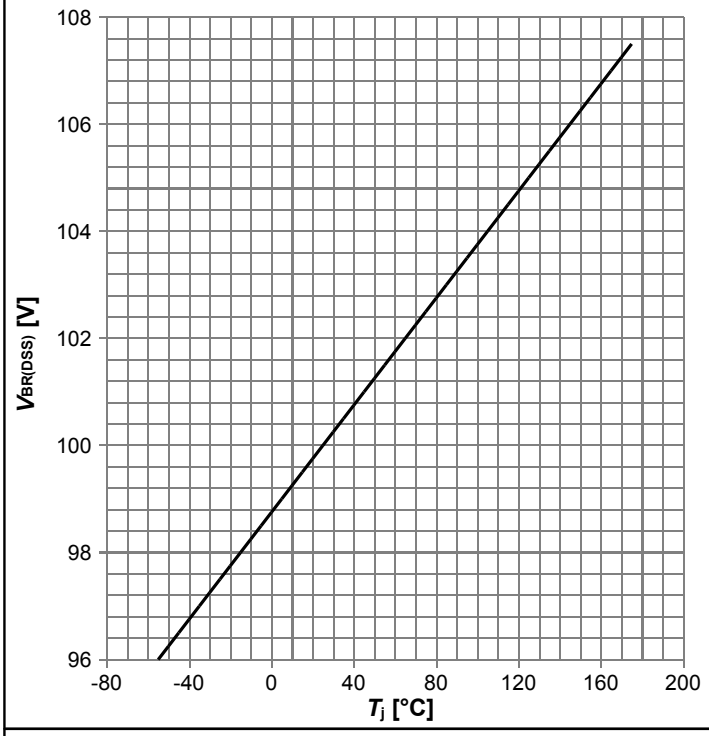

$I_{AS}$=f($t_{AV}$); $R_{GS}$=25 Ω; parameter: $T_{j,start}$

**Diagram 14: Typ. gate charge**



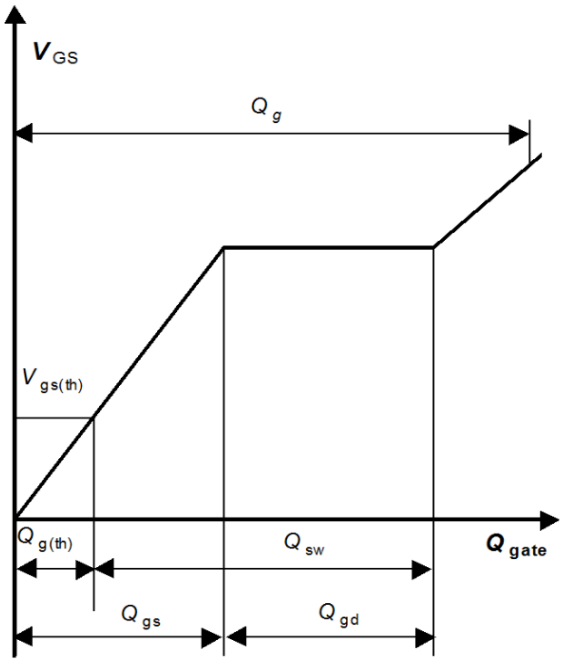

$V_{GS}$=f($Q_{gate}$), $I_D$=30 A pulsed, $T_j$=25 °C; parameter: $V_{DD}$

**Diagram 15: Drain-source breakdown voltage**

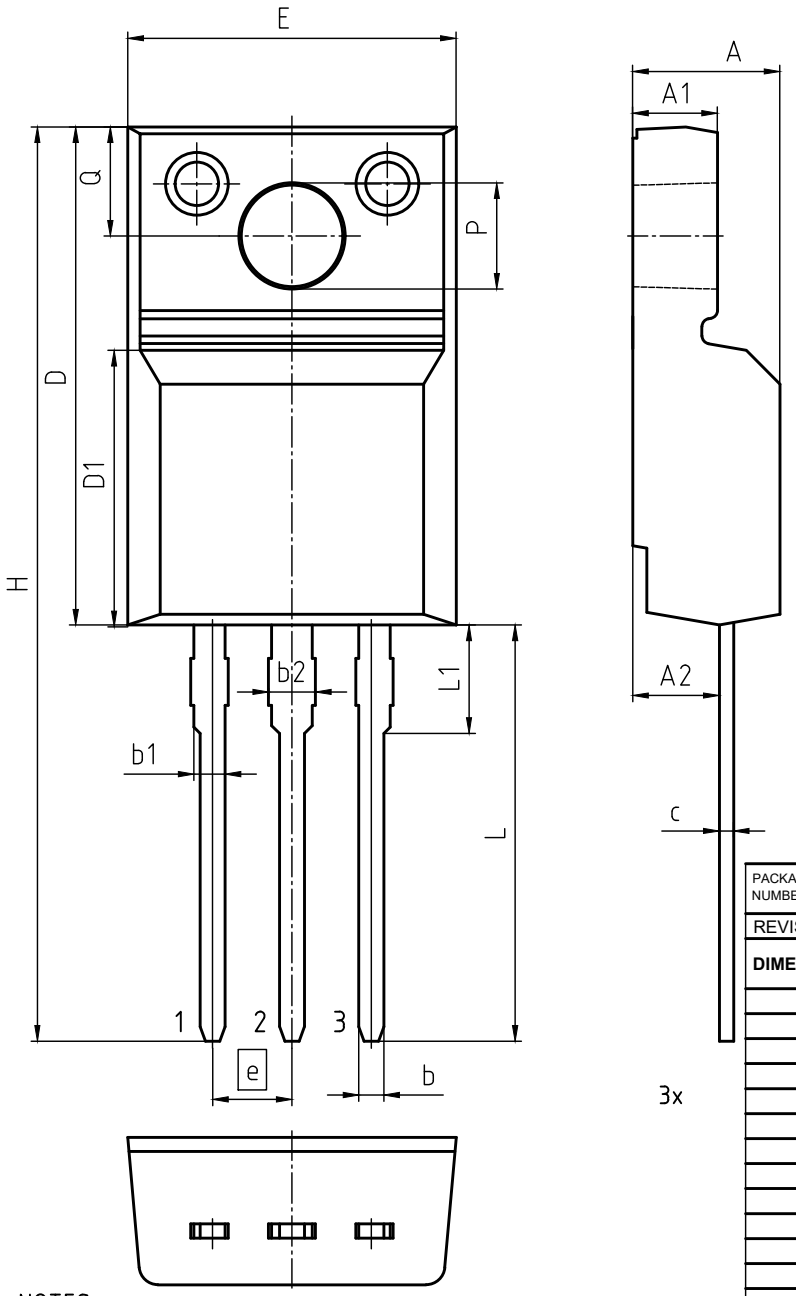



$V_{BR(DSS)}$=f($T_j$); $I_D$=1 mA

**Diagram Gate charge waveforms**



# 5 Package Outlines




| PACKAGE - GROUP NUMBER: | PG-TO220-3-U02 | |
|---|---|---|
| REVISION: 01 | DATE: 02.02.2021 | |
| **DIMENSIONS** | **MILLIMETERS** | |
| | MIN. | MAX. |
| **A** | 4.50 | 4.90 |
| **A1** | 2.34 | 2.85 |
| **A2** | 2.42 | 3.43 |
| **b** | 0.61 | 0.94 |
| **b1** | 0.76 | 1.45 |
| **b2** | 0.95 | 1.52 |
| **c** | 0.33 | 0.63 |
| **D** | 15.67 | 16.15 |
| **D1** | 8.66 | 9.83 |
| **E** | 9.63 | 10.75 |
| **e** | 2.54 | |
| **H** | 29.00 | 29.85 |
| **L** | 12.78 | 13.75 |
| **L1** | 2.83 | 3.67 |
| **øP** | 3.05 | 3.45 |
| **Q** | 3.20 | 3.50 |

NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

**Figure 1 Outline PG-TO220 FullPAK, dimensions in mm**

## Revision History

IPA082N10NF2S

**Revision: 2021-03-16, Rev. 2.0**

| Previous Revision | | |
|---|---|---|
| Revision | Date | Subjects (major changes since last revision) |
| 2.0 | 2021-03-16 | Release of final version |



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