Instrumentation Amplifier Datasheet INSAMPV 2.2

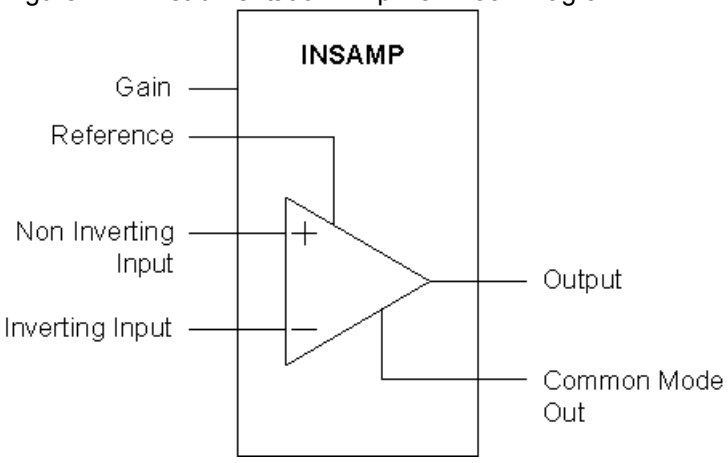
Resources	PSoC® Blocks			API Memory (Bytes)		Pins (per External I/O)
	Digital	Analog CT	Analog SC	flash	RAM	
CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52						
Two Op-Amps	0	2	0	57	0	1
Three Op-Amps	0	2	1	113	0	1

Features and Overview

- User-programmable gain from 2 to 16 with a two opamp topology
- User-programmable gain up to 93 for the three opamp topology (CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52 families only)
- High impedance differential inputs
- Single-ended output
- Selectable reference with the two opamp topology

The INSAMP User Module provides a standard two opamp instrumentation amplifier circuit topology and, for the CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52families of PSoC devices, a standard three opamp topology. This amplifier has high input impedance, good rejection of common mode signals, and wide bandwidth.

Figure 1. Instrumentation Amplifier Block Diagram

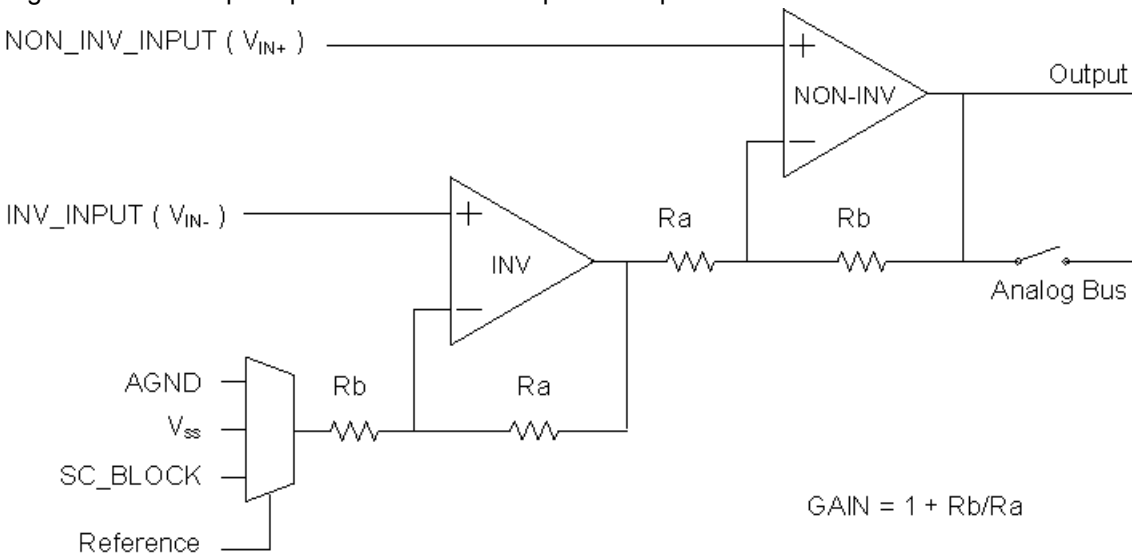


Functional Description

Two Op-Amp Topology

The INSAMP User Module two opamp topology maps onto a pair of analog continuous time (CT) PSoC blocks. This user module converts externally applied differential signals to single-ended signals, referenced to the selected internal analog ground. Its inputs are connected to the input multiplexers. The gain, output reference, and analog output bus connection are set in the Device Editor.

Figure 2. Two Op-Amp Instrumentation Amplifier Simplified Schematic



The gain of the instrumentation amplifier is determined by the setting of programmable taps in resistor arrays, in each of two analog CT PSoC blocks.

The output of INV, the block connected to the inverting input, has the following transfer function.

Equation 1

$$V_{O_{INV}} = V_{IN-} \cdot \left(1 + \frac{R_a}{R_b}\right) - V_{Ref} \frac{R_a}{R_b}$$

The block NON_INV inverts the output of INV and subtracts it, for the following transfer function.

Equation 2

$$V_{O_{NONINV}} = V_{IN+} \cdot \left(1 + \frac{R_b}{R_a}\right) - V_{O_{INV}} \frac{R_b}{R_a}$$

Then the INSAMP User Module has a transfer function as follows.

Equation 3

$$V_O = (V_{IN+} - V_{IN-}) \cdot \left(1 + \frac{R_b}{R_a}\right) + V_{Ref}$$

The user selects analog ground in the global resources section of PSoC Designer. The choices include a fixed value derived from the internal bandgap reference ($2*V_{BandGap}$), and a value ratiometric to the supply voltage ($V_{dd}/2$). In CY8C27xxx, additional analog ground selections are offered: $V_{BandGap}$, which allows connection to fixed-scale ADCs for 3.3V operation and $3.2*V_{BandGap}$, which allows connection to

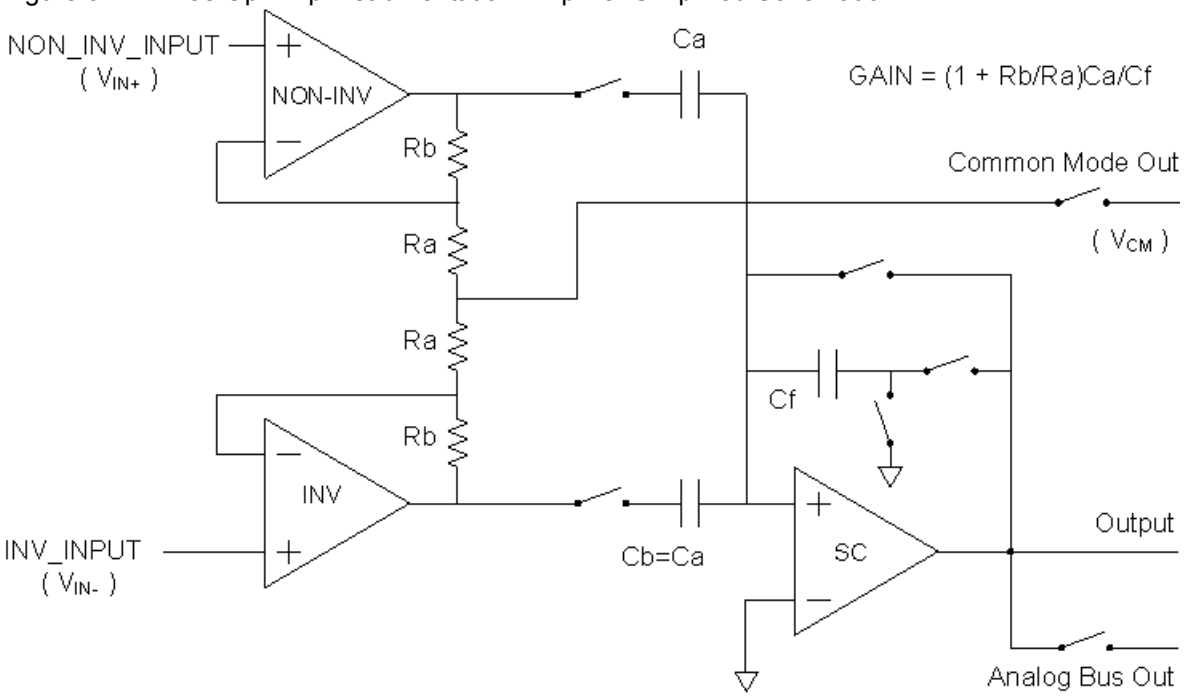
fixed-scale ADCs for 5.0V operation. The selection of analog ground and gain value determine the usable input and output range of each of the blocks. Block INV has higher gains for low user module gains. This places the narrowest limit on the allowed input range. This is shown in graphical form in the specifications section.

Three Op-Amp Topology

The three opamp INSAMP utilizes two continuous time PSoC blocks, designated INV and NON_INV to form an amplifier with differential input and differential output. The two blocks have identical gain and have their bottom resistor multiplexers tied together. The output of the differential amplifier is converted to a single ended voltage referenced to analog ground by a switched capacitor block, designated CONVERT.

In addition to its wide input dynamic range, this input topology is characterized by excellent common mode rejection.

Figure 3. Three Op-Amp Instrumentation Amplifier Simplified Schematic



The INV block and NON_INV block transfer functions are, respectively, as follows.

Equation 4

$$Vout_{INV} = V_{CM} + \left(1 + \frac{R_b}{R_a}\right)\left(\frac{V_{IN+} - V_{IN-}}{2}\right)$$

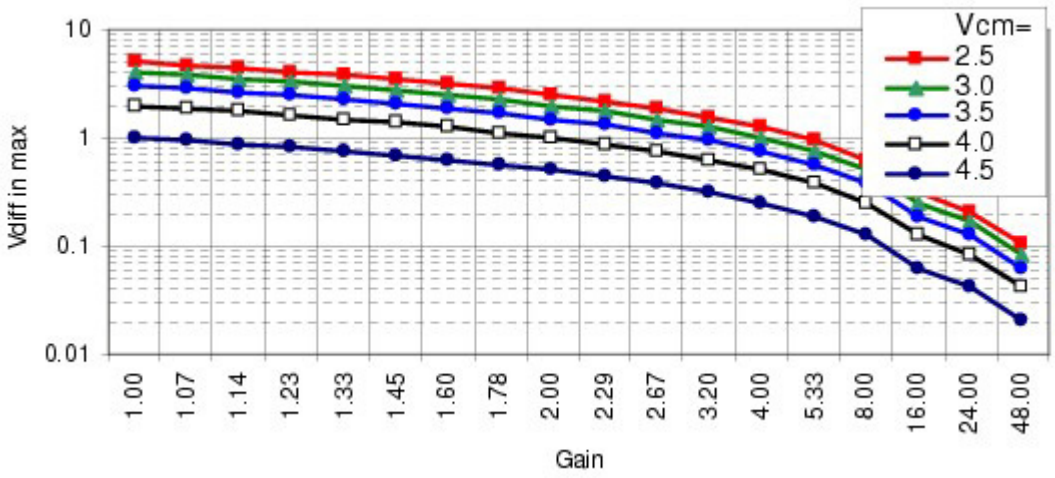
Equation 5

$$Vout_{NONINV} = V_{CM} - \left(1 + \frac{R_b}{R_a}\right)\left(\frac{V_{IN+} - V_{IN-}}{2}\right)$$

The input amplifier has unity common mode gain. This offers a considerable advantage in input common mode range over the two opamp version of the instrumentation amplifier. The maximum differential input range is limited by the output swing of the input opamps and the gain of the amplifiers. Increasing the

common mode voltage or the gain decreases the allowed input signal level, as shown in the following figure:

Figure 4. Maximum Input Level vs. Gain



The input gain limit is symmetrical about analog ground, so that input common mode voltage of 0.5V above Vss has the same input limitation as input common mode voltage 0.5V below Vcc.

The output of block INV drives the B-cap input of CONVERT; the output of block NON_INV drives the A-cap input of CONVERT. The sign of the B-cap input is fixed by block topology to be negative. The sign of the A-cap input is set in the user module firmware to be positive. The A-cap and B-caps have identical values; thus the conversion of the continuous time block outputs is differential and the output of CONVERT is

Equation 6

$$V_{AGND} + (V_{IN+} - V_{IN-})\left(1 + \frac{R_a}{R_b}\right)\frac{C_a}{C_f}$$

The available resistor ratios for Rb and Ra set the useful gain range of the input stage to values between 1.0 and 48.0. Conversion gains in the switched capacitor block can be between 0.032 and 1.9375 (i.e., 1/32 to 31/16). This yields a large number of useful gain settings between 1.0 and 93. Differential Gain and Conversion Gain are set independently by the user as parameters in PSoC Designer and may be changed at run time through the SetGain API function.

DC and AC Electrical Characteristics

Electrical characteristics are different for the two and three opamp topologies.

Three Op-Amp Topology

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25C, Vdd = 5.0V, output referenced to Analog Ground = 2*VBandGap.

Table 1. 5.0V Three Op-Amp DC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=93.0	1.2		%	
Deviation from Nominal at G=48.0	1.4		%	
Deviation from Nominal at G=2.0	0.2		%	
Deviation from Nominal at G=1.0	0.2		%	
Input				
Input Offset Voltage	3.5		mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
CMRR	60		dB	Gain = 48
PSRR	42		dB	
Output Swing	0.05 to Vdd-0.05	--	V	
Operating Current				
Low Power	800		µA	Operating current may be reduced by 50% if Op-Amp Bias is set to Low, but column clock must be reduced.
Med Power	3,000		µA	
High Power	11,900		µA	

Table 2. 5.0V Three Op-Amp AC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate (20% to 80%)[2]				
Low Power	0.5		V/µsec	Gain=2.0, 2.0V step at input
Med Power	1.9		V/µsec	
High Power	6.0		V/µsec	
Settling Time[2]				
Low Power	11		µsec	
Med Power	4		µsec	
High Power	3		µsec	

Parameter	Typical	Limit	Units	Conditions and Notes
Noise[2]				Referred to input
Low Power	625		nV/√Hz	Differential stage gain=4. Op-Amp bias low except at High Power.
Med Power	198		nV/√Hz	
High Power	175		nV/√Hz	

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25C, Vdd = 3.3V, output referenced to Analog Ground = Vdd/2.

Table 3. 3.3V Three Op-Amp DC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=93.0	1.9		%	
Deviation from Nominal at G=48.0	2.1		%	
Deviation from Nominal at G=2.0	0.1		%	
Deviation from Nominal at G=1.0	0.1		%	
Input				
Input Offset Voltage	3.5		mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
CMRR	51		dB	Gain = 48
PSRR	42		dB	
Output Swing	0.05 to Vdd-0.05	--	V	
Operating Current				
Low Power	1200		µA	Operating current may be reduced by 50% if Op-Amp Bias is set to Low, but column clock must be reduced.
Med Power	3,400		µA	
High Power	12,000		µA	

Table 4. 3.3V Three Op-Amp AC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate (20% to 80%)[2]				
Low Power	0.5		V/µsec	Gain=2.0, 2.0V step at input
Med Power	1.8		V/µsec	
High Power	5.7		V/µsec	
Settling Time[2]				
Low Power	12		µsec	
Med Power	4		µsec	
High Power	3		µsec	
Noise[2]				Referred to input
Low Power	625		nV/√Hz	Op-Amp bias low except at High Power.
Med Power	198		nV/√Hz	
High Power	175		nV/√Hz	

Electrical Characteristics Notes

1. Includes I/O pin.Based upon device simulation.

Two Op-Amp Topology

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25C, Vdd = 5.0V, output referenced to Analog Ground = 2*VBandGap, Op-Amp Bias = High, Ref Power = High, UM Power = High, Column clock = 2MHz (sample clock = 500 kHz).

Table 5. 5.0V Two Op-Amp DC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=16.0	2.5		%	
Deviation from Nominal at G=8.0	1.6		%	
Deviation from Nominal at G=4.0	0.4		%	
Deviation from Nominal at G=2.0	0.1		%	
Input				

Parameter	Typical	Limit	Units	Conditions and Notes
Input Offset Voltage	3.1		mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
CMRR	59		dB	Gain = 2
PSRR	62		dB	
Operating Current				
Low Power	284		µA	Operating current may be reduced by 50% if Op-Amp Bias is set to Low.
Med Power	1080		µA	
High Power	4166		µA	

Table 6. 5.0V Two Op-Amp AC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate (20% to 80%)[2]				
Low Power	0.5		V/µsec	Gain=2.0, 2.0V step at input
Med Power	1.9		V/µsec	
High Power	6.0		V/µsec	
Settling Time[2]				
Low Power	11		µsec	
Med Power	4		µsec	
High Power	3		µsec	
Noise[2]				Referred to input
Low Power	354		nV/√Hz	Op-Amp bias low except at High Power.
Med Power	112		nV/√Hz	
High Power	99		nV/√Hz	

The following values are indicative of expected performance and based on initial characterization data. Unless otherwise specified in the following tables, TA = 25C, Vdd = 3.3V, output referenced to Analog Ground = Vdd/2, Op-Amp Bias = High, Ref Power = High, UM Power = High, Column clock = 2MHz (sample clock = 500 kHz).

Table 7. 3.3V Two Op-Amp DC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

Parameter	Typical	Limit	Units	Conditions and Notes
Gain				
Deviation from Nominal at G=16.0	3.2		%	
Deviation from Nominal at G=8.0	1.6		%	
Deviation from Nominal at G=4.0	0.6		%	
Deviation from Nominal at G=2.0	0.1		%	
Input				
Input Offset Voltage	3.9		mV	
Input Voltage Range	--	Vss to Vdd	V	
Leakage[1]	1	--	nA	
Input Capacitance[1]	3	--	pF	
Output Swing	0.05 to Vdd-0.05	--	V	
CMRR	54		dB	Gain = 2
PSRR	42		dB	
Operating Current				
Low Power	270		µA	Operating current may be reduced by 50% if Op-Amp Bias is set to Low.
Med Power	1046		µA	
High Power	4934		µA	

Table 8. 3.3V Two Op-Amp AC Electrical Characteristics, CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52Family of PSoC Devices

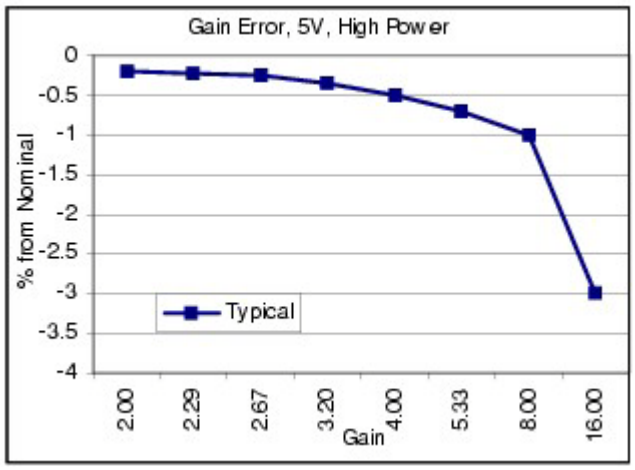
Parameter	Typical	Limit	Units	Conditions and Notes
Slew Rate (20% to 80%)[2]				
Low Power	0.5		V/µsec	Gain=2.0, 2.0V step at input
Med Power	1.8		V/µsec	
High Power	5.7		V/µsec	
Settling Time[2]				
Low Power	12		µsec	
Med Power	4		µsec	
High Power	3		µsec	

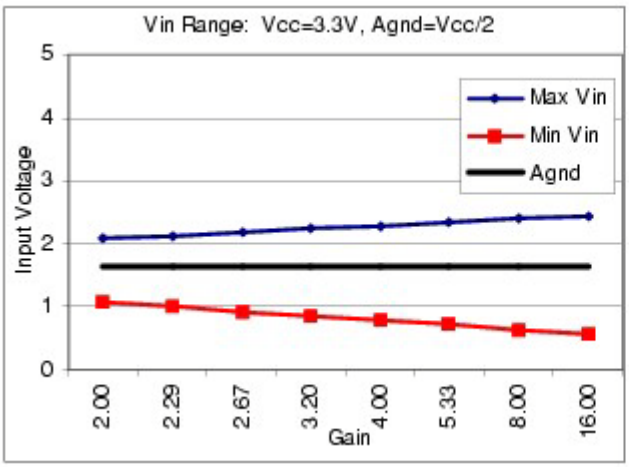
Parameter	Typical	Limit	Units	Conditions and Notes
Noise[2]				Referred to input
Low Power	354		nV/√Hz	Op-Amp bias low except at High Power.
Med Power	112		nV/√Hz	
High Power	99		nV/√Hz	

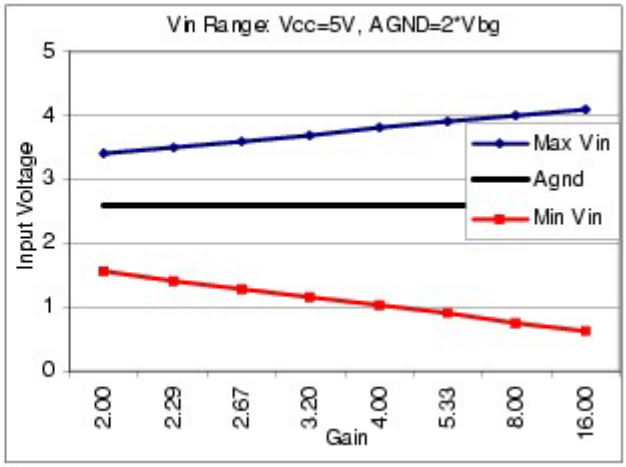
Electrical Characteristics Notes

1. Includes I/O pin.
2. Based upon device simulation.

Two Op-Amp Topology

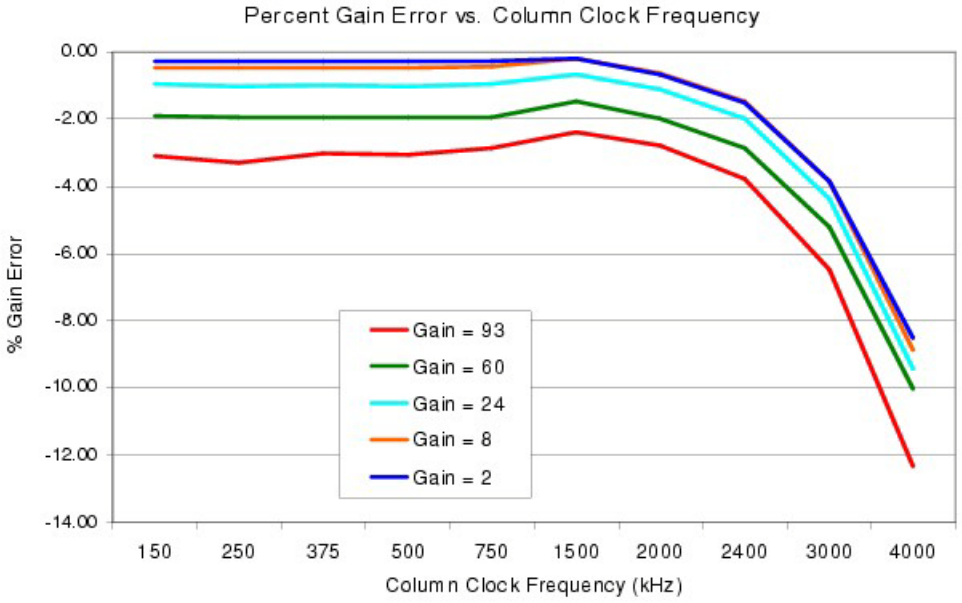






For the three opamp topology a switched capacitor block is used to provide the conversion gain portion of the amplifier. The switched capacitor block is driven by a column clock which is divided internally by four to provide the phases of the clock needed for switched capacitor operation. The chart below is for a CY8C29/27/24xxx, CY8C23x33, CY8CLED04/08/16, CY8CLED0xD, CY8CLED0xG, CY8CTST120, CY8CTMG120, CY8CTMA120, CY8C28x45, CY8CPLC20, CY8CLED16P01, CY8C28x43, CY8C28x52device operating at 5V. It shows the percent error as a function of column clock frequencies

for a variety of gain settings. Two important performance points can be seen from the chart. At 1.2MHz there is a slight change and at around 2.4MHz there is a severe change in performance.



Placement

Two Op-Amp Topology

The NV and NON_INV blocks map onto a pair of continuous time PSoC blocks in columns 0 and 1 (or, if available, in columns 2 and 3) The blocks may be swapped within the column pair for flexible port assignments for the inverting and non-inverting inputs.

Three Op-Amp Topology

The three opamp circuit topology employs a pair of continuous time PSoC blocks and a single switched capacitor PSoC block. The two continuous time blocks, INV and NON_INV, are placed in a pair of columns in the same manner as the two opamp topology. The CONVERT block maps onto a switched capacitor PSoC block immediately underneath one of the two continuous-time blocks. Internal block-to-block connections limit the number of arrangements to three for any given column pair.

Parameters and Resources

Inverting and non-inverting inputs to the instrumentation amplifier are driven by the output of the analog input column multiplexers. These connections are implicit. Configuring the input multiplexors above the INV and NON_INV PSoC blocks must be accomplished directly in the Device Editor or through instances of the AMUX4 User Module.

Gain

The gain values that can be selected for the two opamp circuit topology are 2.00, 2.28, 2.67, 3.20, 4.00, 5.33, 8.00, and 16.00.

Differential Gain and Conversion Gain

The three opamp topology gives a much wider selection. The total gain is the product of the differential gain and the conversion gain. The 18 differential gain settings range from 1.0 to 48.0. They provide

symmetric settings for the continuous time reference and feedback resistors. The 47 conversion gain settings determine the input and feedback capacitor settings of the continuous time block. They range from 0.0313 to 1.938. Thus the total gain product ranges from a minimum of 0.0313 to 93.0.

Reference

The single-ended output of the two opamp instrumentation amplifier is referenced to a value selected by the user. This parameter does not apply to the three opamp topology. The choices include the following.

- **AGND** – Analog ground is most useful for connection to additional signal conditioning for gain, comparators, filters, and analog-to-digital converters.
- **VSS** – Negative supply rail.
- **SC_BLOCK** – Output of an adjacent switched capacitor PSoC block. The specific block available is shown when the user module is placed in Device Editor. Note that this option is useful for providing a controlled reference for offset compensation when the SC_BLOCK connection used is the output of a DAC. The DAC output does not have a sample and hold function. User modules using the output of the INSAMP with the reference driven by a DAC, should have their sample phase synced to the DAC.

AnalogBus

The output of the instrumentation amplifier can be placed on the analog column output bus using the Enable selection of the AnalogBus module parameter. This is generally done to take the output off-chip by routing it onto the bus, through the associated analog output buffer and through the pin to which the buffer is connected. The bus may also be helpful in routing the two opamp output to the bottom row of the analog array, in some cases.

CommonModeOut

This parameter only applies to the three opamp topology. The common mode node connects the two continuous time blocks at the “ends” of their resistor strings (see the figure “Three Op-Amp Instrumentation Amplifier Simplified Schematic”). The common mode voltage derived from this node is useful in many applications for improving noise immunity through shielding by such means as guard traces. This voltage may be connected to the analog column output bus and its associated analog output buffer through either of the CT PSoC blocks, INV or NON_INV, by setting this parameter. In addition to these two options, the CommonModeOut parameter may be set to “None.”

One of the two CT blocks, either INV or NON_INV, will lie in the same analog column as the switched capacitor CONVERT block. If the AnalogBus parameter is set to Enable, either set CommonModeOut to “None” or set it to the block that lies in the column not shared by the CONVERT block. Otherwise, the output of the INSAMP will be connected in a feedback loop to the common mode point and the output behavior will not correspond to expectations.

Application Programming Interface

The Application Programming Interface (API) routines are provided as part of the user module to allow the designer to deal with the module at a higher level. This section specifies the interface to each function together with related constants provided by the “include” files.

Note

In this, as in all user module APIs, the values of the A and X register may be altered by calling an API function. It is the responsibility of the calling function to preserve the values of A and X prior to the call if those values are required after the call. This “registers are volatile” policy was selected for efficiency reasons and has been in force since version 1.0 of PSoC Designer. The C compiler automatically takes care of this requirement. Assembly language programmers must ensure their code observes the policy, too. Though some user module API function may leave A and X unchanged, there is no guarantee they will do so in the future.

For Large Memory Model devices, it is also the caller's responsibility to preserve any value in the CUR_PP, IDX_PP, MVR_PP, and MVW_PP registers. Even though some of these registers may not be modified now, there is no guarantee that will remain the case in future releases.

INSAMP_Start

Description:

Performs all required initialization for this user module and sets the power level for the continuous time PSoC block. Instrumentation amplifier output will be driven.

C Prototype:

```
void  INSAMP_Start(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  INSAMP_Start
```

Parameters:

bPowerSetting: One byte that specifies the power level to both analog PSoC blocks. Following reset and configuration, the PSoC blocks assigned to the instrumentation amplifier are powered down. Symbolic names provided in C and assembly, and their associated values, are given in the following table.

Symbolic Name	Value
INSAMP_NAME_OFF	0
INSAMP_NAME_LOWPOWER	1
INSAMP_NAME_MEDPOWER	2
INSAMP_NAME_HIGHPOWER	3

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

INSAMP_SetPower

Description:

Sets the power level for the continuous time PSoC blocks. May be used to turn the blocks OFF and ON.

C Prototype:

```
void  INSAMP_SetPower(BYTE bPowerSetting)
```

Assembler:

```
mov   A, bPowerSetting
lcall  INSAMP_SetPower
```

Parameters:

bPowerSetting: Same as the PowerSetting used for the Start function.

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

INSAMP_SetGain

Description:

Sets the gain for the continuous time PSoC block. This function only applies to the two opamp circuit topology.

C Prototype:

```
void  INSAMP_SetGain(BYTE bGainSetting)
```

Assembler:

```
mov   A, bGainSetting
lcall  INSAMP_SetGain
```

Parameters:

bGainSetting: Symbolic names provided in C and assembly, and their associated values, are given in the following table. The value is passed directly to the NON_INV block. The value for the INV block is calculated in the .asm routine. Programmed gain of 16.0 uses the declared name of ....G16_0.

Symbolic Name	Value
INSAMP_G16_0	00h
INSAMP_G8_00	10h
INSAMP_G5_33	20h
INSAMP_G4_00	30h

Symbolic Name	Value
INSAMP_G3_20	40h
INSAMP_G2_67	50h
INSAMP_G2_27	60h
INSAMP_G2_00	70h

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

INSAMP_Set2StageGain

Description:

Sets the total gain for the three opamp instrumentation amplifier. The total gain is the product of the gain settings applied to the input (differential) and output (conversion) stages. Both stages are set by this function.

C Prototype:

```
void INSAMP_Set2StageGain(BYTE bInGain, BYTE bOutGain);
```

Assembler:

```
mov   A,  IN_GAIN_CONSTANT
mov   X, OUT_GAIN_CONSTANT
lcall  INSAMP_Set2StageGain
```

Parameters:

bInGain (IN_GAIN_CONSTANT): Specifies the gain of the differential (input) section of the instrumentation amplifier. This section is implemented by the two continuous time PSoC blocks, INV and NON_INV. Symbolic names for gain constants are defined by the C and assembly language include files and listed in the following table.

Symbolic Name	Gain FactorT	Value
INSAMP_INGAIN_48	48	01h
INSAMP_INGAIN_24	24	11h
INSAMP_INGAIN_16	16	00h
INSAMP_INGAIN_8	8	10h
INSAMP_INGAIN_5_33	$5\ ^{1}/_{3}$	20h
INSAMP_INGAIN_4	4	30h
INSAMP_INGAIN_3_20	$3\ ^{1}/_{5}$	40h
INSAMP_INGAIN_2_67	$2\ ^{2}/_{3}$	50h

Symbolic Name	Gain FactorT	Value
INSAMP_INGAIN_2_29	$2\ ^{2}/_{7}$	60h
INSAMP_INGAIN_2	2	70h
INSAMP_INGAIN_1_78	$1\ ^{7}/_{9}$	80h
INSAMP_INGAIN_1_60	$1\ ^{6}/_{10}$	90h
INSAMP_INGAIN_1_45	$1\ ^{5}/_{11}$	A0h
INSAMP_INGAIN_1_33	$1\ ^{4}/_{12}$	B0h
INSAMP_INGAIN_1_23	$1\ ^{3}/_{13}$	C0h
INSAMP_INGAIN_1_14	$1\ ^{2}/_{14}$	D0h
INSAMP_INGAIN_1_07	$1\ ^{1}/_{15}$	E0h
INSAMP_INGAIN_1	1	F0h

bOutGain (OUT_GAIN_CONSTANT): Specifies the gain of the conversion (output) section of the instrumentation amplifier implemented by the switched capacitor PSoC block. Symbolic names are provided by the C and assembly include files. Their associated values are given in the following table.

Symbolic Name	Gain Factor	Value	Symbolic Name	Gain Factor	Value
INSAMP_OUTGAIN_1_94	$1\ ^{15}/_{16}$	1.9375	INSAMP_OUTGAIN_0_72	$^{23}/_{32}$	0.7188
INSAMP_OUTGAIN_1_88	$1\ ^{14}/_{16}$	1.8750	INSAMP_OUTGAIN_0_69	$^{22}/_{32}$	0.6875
INSAMP_OUTGAIN_1_81	$1\ ^{13}/_{16}$	1.8125	INSAMP_OUTGAIN_0_66	$^{21}/_{32}$	0.6563
INSAMP_OUTGAIN_1_75	$1\ ^{12}/_{16}$	1.7500	INSAMP_OUTGAIN_0_63	$^{20}/_{32}$	0.6250
INSAMP_OUTGAIN_1_69	$1\ ^{11}/_{16}$	1.6875	INSAMP_OUTGAIN_0_59	$^{19}/_{32}$	0.5938
INSAMP_OUTGAIN_1_63	$1\ ^{10}/_{16}$	1.6250	INSAMP_OUTGAIN_0_56	$^{18}/_{32}$	0.5625
INSAMP_OUTGAIN_1_56	$1\ ^{9}/_{16}$	1.5625	INSAMP_OUTGAIN_0_53	$^{17}/_{32}$	0.5313
INSAMP_OUTGAIN_1_50	$1\ ^{8}/_{16}$	1.5000	INSAMP_OUTGAIN_0_50	$^{16}/_{32}$	0.5000
INSAMP_OUTGAIN_1_44	$1\ ^{7}/_{16}$	1.4375	INSAMP_OUTGAIN_0_47	$^{15}/_{32}$	0.4688
INSAMP_OUTGAIN_1_38	$1\ ^{6}/_{16}$	1.3750	INSAMP_OUTGAIN_0_44	$^{14}/_{32}$	0.4375
INSAMP_OUTGAIN_1_31	$1\ ^{5}/_{16}$	1.3125	INSAMP_OUTGAIN_0_41	$^{13}/_{32}$	0.4063

Symbolic Name	Gain Factor	Value	Symbolic Name	Gain Factor	Value
INSAMP_OUTGAIN_1_25	$1\ ^{4}/_{16}$	1.2500	INSAMP_OUTGAIN_0_38	$^{12}/_{32}$	0.3750
INSAMP_OUTGAIN_1_19	$1\ ^{3}/_{16}$	1.1875	INSAMP_OUTGAIN_0_34	$^{11}/_{32}$	0.3438
INSAMP_OUTGAIN_1_13	$1\ ^{2}/_{16}$	1.1250	INSAMP_OUTGAIN_0_31	$^{10}/_{32}$	0.3125
INSAMP_OUTGAIN_1_06	$1\ ^{1}/_{16}$	1.0625	INSAMP_OUTGAIN_0_28	$^{9}/_{32}$	0.2813
INSAMP_OUTGAIN_1_00	$^{16}/_{16}$	1.0000	INSAMP_OUTGAIN_0_25	$^{8}/_{32}$	0.2500
INSAMP_OUTGAIN_0_97	$^{31}/_{32}$	0.9688	INSAMP_OUTGAIN_0_22	$^{7}/_{32}$	0.2188
INSAMP_OUTGAIN_0_94	$^{30}/_{32}$	0.9375	INSAMP_OUTGAIN_0_19	$^{6}/_{32}$	0.1875
INSAMP_OUTGAIN_0_91	$^{29}/_{32}$	0.9063	INSAMP_OUTGAIN_0_16	$^{5}/_{32}$	0.1563
INSAMP_OUTGAIN_0_88	$^{28}/_{32}$	0.8750	INSAMP_OUTGAIN_0_13	$^{4}/_{32}$	0.1250
INSAMP_OUTGAIN_0_84	$^{27}/_{32}$	0.8438	INSAMP_OUTGAIN_0_09	$^{3}/_{32}$	0.0938
INSAMP_OUTGAIN_0_81	$^{26}/_{32}$	0.8125	INSAMP_OUTGAIN_0_06	$^{2}/_{32}$	0.0625
INSAMP_OUTGAIN_0_78	$^{25}/_{32}$	0.7813	INSAMP_OUTGAIN_0_03	$^{1}/_{32}$	0.0313
INSAMP_OUTGAIN_0_75	$^{24}/_{32}$	0.7500			

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

INSAMP_Stop

Description:

Powers the user module OFF. Outputs will not be driven.

C Prototype:

```
void  INSAMP_Stop(void)
```

Assembler:

```
lcall  INSAMP_Stop
```

Parameters:

None

Return Value:

None

Side Effects:

The A and X registers may be altered by this function.

Sample Firmware Source Code

Using the instrumentation amplifier API is trivial. If the gain is established at configuration time, it is necessary only to call the INSAMP_Start function. If dynamic re-configuration is used, INSAMP_Start must be called following every call to the LoadConfiguration function that creates the “overlay” in which the INSAMP is placed.

Example 1: Two Op-Amp Topology

In the following C language code, the SetGain function establishes a gain of 3.2 at run time. Later, if the INSAMP is no longer required, it may be stopped to save power, as shown.

```
INSAMP_Start(INSAMP_HIGHPOWER);
INSAMP_SetGain(INSAMP_G3_20);
...
INSAMP_Stop();
```

The equivalent code in assembly language looks like this:

```
mov   A, INSAMP_HIGHPOWER
call  INSAMP_Start
mov   A, INSAMP_G3_20
call  INSAMP_SetGain
...
call  INSAMP_Stop
```

Example 2: Three Op-Amp Topology

In this C language example, the Set2StageGain function establishes a gain of 5 (4 times 1.25) at run time. Again, if the INSAMP is not required at some later time, it may be stopped in the same manner as before.

```
INSAMP_Start(INSAMP_HIGHPOWER);
INSAMP_Set2StageGain(INSAMP_INGAIN_4, INSAMP_OUTGAIN_1_25);
...
INSAMP_Stop();
```

The equivalent code in assembly language looks like this:

```
mov   A, INSAMP_HIGHPOWER
call  INSAMP_Start
mov   A, INSAMP_INGAIN_4
mov   X, INSAMP_OUTGAIN_1_25
call  INSAMP_Set2StageGain
...
call  INSAMP_Stop
```

Configuration Registers

Two Op-Amp Topology

Table 9. NON_INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	Gain				1	1	0	0
CR1	ABus	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	

Table 10. NON_INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	Gain				1	1	0	0
CR1	ABus	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	
CR3	0	0	0	0	0	0	0	0

Gain sets the gain value per selection. This value represents the inverse value of the Gain bitfield in the INV block.

ABus determines whether the COMP PSoC block drives the analog bus. The value of this bitfield is determined by the choice made in the Interconnect View of the Device Editor subsystem.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, and Stop entry points in the API.

Table 11. INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	Gain				0	1	Reference	
CR1	0	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	

Table 12. INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	Gain				0	1	Reference	
CR1	0	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	
CR3	0	0	0	0	0	0	0	0

Gain sets the gain value per selection. This value represents the inverse value of the Gain bitfield in the NON_INV block.

Reference sets the reference point (effective “ground”) for gain.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, and Stop entry points in the API.

Three Op-Amp Topology

Table 13. NON_INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	DifferentialGain				1	1	0	0
CR1	0	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	
CR3	0	0	0	0	0	CMO	1	ExGain

DifferentialGain reflects the gain setting established at configuration time by the DifferentialGain parameter or at run time by the API function, INSAMP_Set2StageGain. This value always matches the DifferentialGain setting in the INV block, below.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, and Stop entry points in the API.

CMO is determined at configuration time by the value of the CommonModeOut parameter.

ExGain is determined at configuration time by the value of the DifferentialGain parameter.

Table 14. INV PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	DifferentialGain				0	1	0	0
CR1	0	0	1	0	0	0	0	1
CR2	0	0	1	0	0	0	Power	
CR3	0	0	0	0	0	CMO	1	ExGain

DifferentialGain reflects the gain setting established at configuration time by the DifferentialGain parameter or at run time by the API function, INSAMP_Set2StageGain. This value always matches the DifferentialGain setting in the NON_INV block, above.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, and Stop entry points in the API.

CMO is determined at configuration time by the value of the CommonModeOut parameter.

ExGain is determined at configuration time by the value of the DifferentialGain parameter.

Table 15. CONVERSION PSoC Block Registers

Reg/Bit	7	6	5	4	3	2	1	0
CR0	FCap	0	0	ConversionGain				
CR1	NIConnect			ConversionGain				
CR2	ABus	0	1	0	0	0	0	0
CR3 [1]	0	0	1	1	InvConnect		Power	
CR3 [2]	0	0	1	1	1	InvConnect	Power	

This format applies when the conversion block is mapped onto a switched capacitor SCC PSoC block.
This format applies when the conversion block is mapped onto a switched capacitor SCD PSoC block.

FCap reflects the value of the feedback capacitor. This value is determined at configuration time by the ConversionGain parameter or at run time by the API function, INSAMP_Set2StageGain.

ConversionGain reflects the gain setting established at configuration time by the ConversionGain parameter or at run time by the API function, INSAMP_Set2StageGain. The values in the CR0 and CR1 registers are always exactly matched.

NIConnect and **InvConnect** are established by the placement location of the user module. They establish the connections from the outputs of the INV and NON_INV PSoC blocks to the inputs of the CONVERT block.

ABus reflects the configuration time setting of the AnalogBus parameter.

Power is set to ‘Off’ following device reset and configuration. It is modified by calling Start, SetPower, and Stop entry points in the API.

Version History

Version	Originator	Description
2.2	DHA	Added Version History

Note PSoC Designer 5.1 introduces a Version History in all user module datasheets. This section documents high level descriptions of the differences between the current and previous user module versions.