IMD111T/IMD112T - iMOTION™ driver for motor control

Motor controller with integrated high-voltage gate driver

IMD111T/IMD112T

Features

- Motion Control Engine (MCE) as a ready-to-use control solution for variable speed drives
- Integrated script engine for application control customization
- Integrated drive and system protection features
- Field oriented control (FOC) for permanent magnet synchronous motor (PMSM)
- Flexible space vector PWM for sinusoidal voltage control
- Current sensing via single or leg shunt
- Sensorless operation
- Hall sensor operation using analog or digital Hall
- Integrated analog comparators for over-current protection
- Built-in temperature sensor
- Power factor correction (PFC) control (optional)
- Flexible control input options: UART, Frequency, duty cycle or analog signal
- Certified drive safety functions according to IEC/UL 60730-1 'Class B'
- High voltage three phase gate driver with 600 V blocking voltage
- 15V supply voltage for gate driver
- Thin-film-SOI-technology with negative transient robustness
- Ultra fast integrated boot strap diodes
- Integrated 5 V voltage regulator for controller supply
- External 5 V output available
- Small LQFP-40 package with improved clearance & creepage
- Footprint derived from LQFP-48

Potential applications

- Small and major home appliances
- Fans, Pumps, Compressors
- General purpose variable speed drives

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

iMOTION™IMD110-6 is a family of highly integrated ICs for the control of variable speed drives. It integrates a motor controller with a high voltage three phase gate driver and a voltage regulator.

The motor controller uses the Motion Control Engine (MCE) to create a ready-to-use solution to perform control of a permanent magnet synchronous motor (PMSM) providing the shortest time to market for any motor system at the lowest system and development cost. The integrated script engine allows to add application flexibility without interfering with the motor and PFC control algorithm.
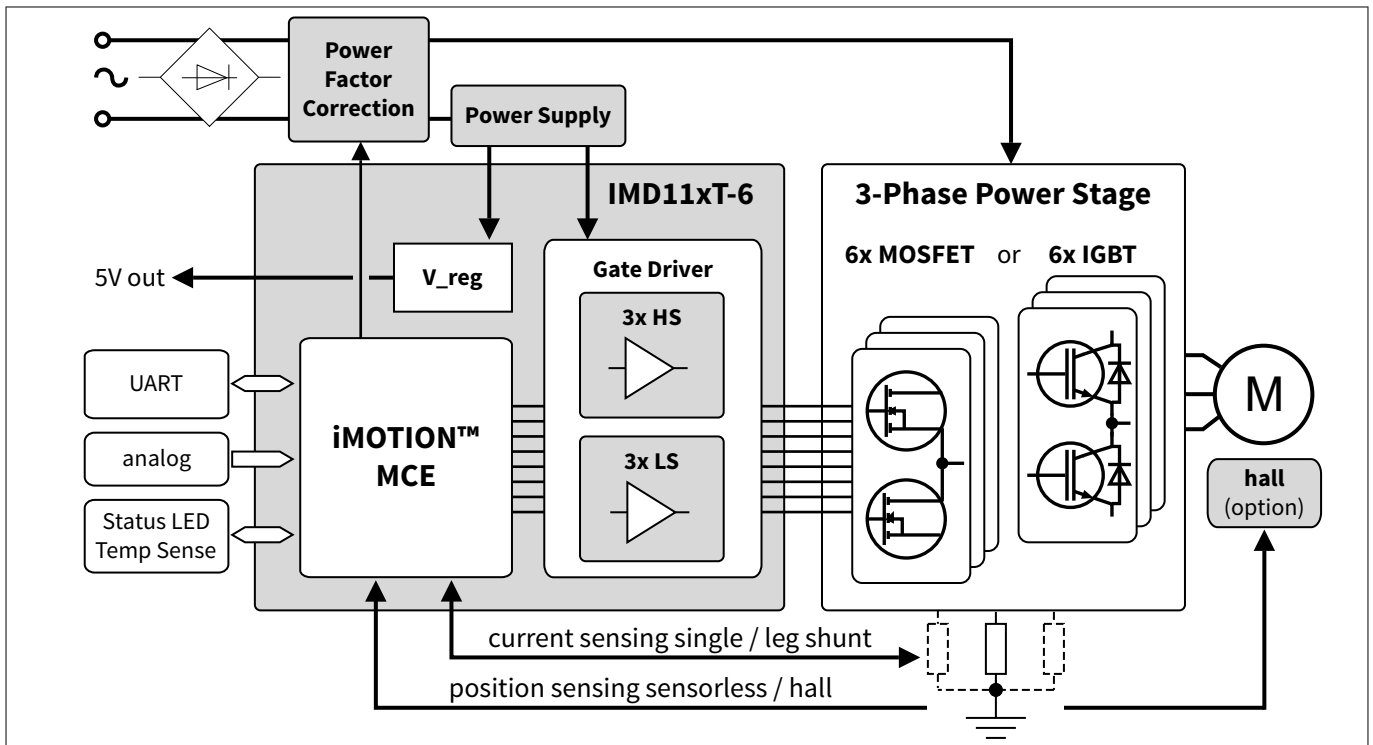
Figure 1   **Application block diagram**

Ordering information

Product type	Control function integrated	Package
IMD111T-6F040	iMOTION™ Motor control	PG-LQFP-40-1
IMD112T-6F040	iMOTION™ Motor + PFC control	PG-LQFP-40-1

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1 Block diagram reference

Figure 2   **Block diagram reference**

2 Pin configuration

2.1 Pin types and pad structure

The pin type is specified as follows:

- P - power
- I - digital input
- O - digital output
- IO – digital input or output
- AIN - analog input
- AO - analog output

Figure 3 shows the pad structure and pin function control configuration for the input and output pins of the controller integrated.

The pin function, type and pull up/pull down circuit configuration are all controlled by the Motion Control Engine. Digital input, output or analog input signals that are not assigned to MCE functions can be assigned to the script engine.The gate driver outputs are controlled by MCE PWM signals internally connected to the gate driver inputs.
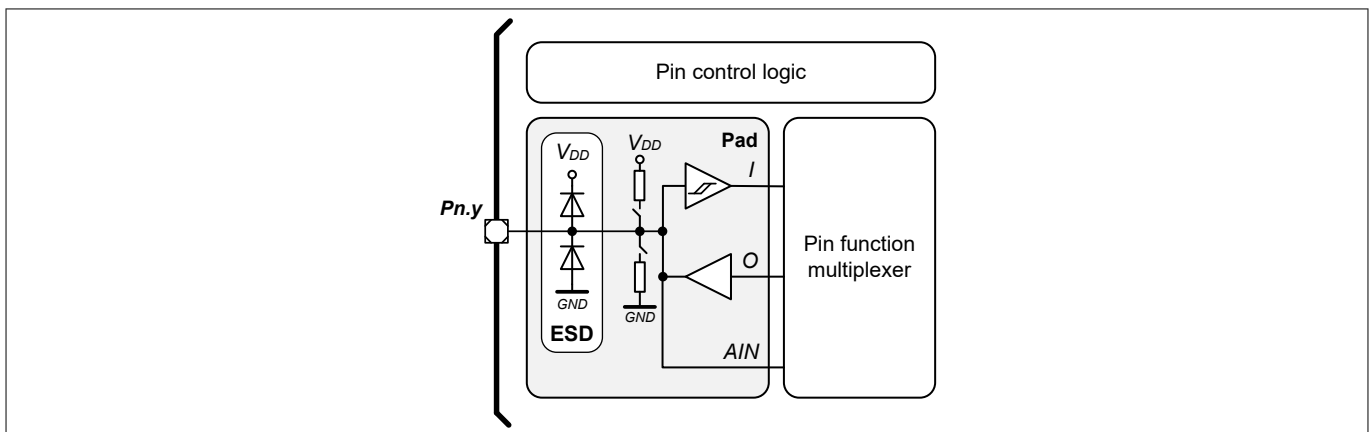
Figure 3   **Pin Pad and Function Configuration**

The pin function table given below refers to the standard configuration. The pin control or interface functions are defined by the version of software downloaded to the device and may change. Some of the input pins can be configured to have pull up or pull down resistor and some output pins can be configured to push-pull or open drain. This is described in the respective software reference manual.

Pins can serve multiple functions and have to be configured accordingly. Please also refer to the respective pin configuration drawings in this data sheet and the description in the MCE software reference manual.

Pins that do not have any signal assigned are reserved for future use. These pins should be left unconnected and neither be connected to ground nor to the positive supply.

Note: All required reference voltages are generated by an internal DAC, therefore the AO pins like IREF, REFU, REFV, and REFW only require a blocking capacitor.

2.2 Pin definitions and functions

Table 1 **Pin definitions and functions**

Signal	Type	IMD111T	IMD112T	Description
Supply				
VCC1	Power	8	8	Control supply voltage input to the voltage regulator
VCC	Power	22	22	Gate drive supply voltage
VDD	Power	5	5	Digital controller voltage (this 5V LDO output must be blocked with a ceramic capacitor)
VSS	Power	6, 7, 23	6, 7, 23	Ground
Motor control				
COM	P	9	9	Low side gate driver return
LO1	O	12	12	Low side gate driver output - phase 1
LO2	O	11	11	Low side gate driver output - phase 2
LO3	O	10	10	Low side gate driver output - phase 3
VS1	P	19	19	High side gate driver return - phase 1
HO1	O	20	20	High side gate driver output - phase 1
VB1	P	21	21	High side gate driver positive power supply - phase 1
VS2	P	16	16	High side gate driver return - phase 2
HO2	O	17	17	High side gate driver output - phase 2
VB2	P	18	18	High side gate driver positive power supply - phase 2
VS3	P	13	13	High side gate driver return - phase 3
HO3	O	14	14	High side gate driver output - phase 3
VB3	P	15	15	High side gate driver positive power supply - phase 3
VDC	AIN	36	36	DC bus sensing input
ISS/IU	AIN	40	40	Current sense input single shunt / phase U
IV	AIN	37	37	Current sense input phase V / analog input
IW	AIN	33	33	Current sense input phase W / analog input
REFU[1]	O	39	39	Itrip single shunt/phase U reference DAC output
REFV	AIN	38	38	Itrip phase V reference / analog input
REFW	AIN	32	32	Itrip phase W reference / analog input
Hall sensor inputs				
AHALL1+	AIN	32	32	Analog Hall Element input 1 (+)
AHALL1-	AIN	33	33	Analog Hall Element input 1 (-)
AHALL2+	AIN	38	38	Analog Hall Element input 2 (+)
AHALL2-	AIN	37	37	Analog Hall Element input 2 (-)
HALL1	I	28	28	Digital Hall sensor input 1

(table continues...)

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[1] This pin must have a filter capacitor connected to ground

2 Pin configuration

Table 1   (continued) Pin definitions and functions

Signal	Type	IMD111T	IMD112T	Description
HALL2	I	29	29	Digital Hall sensor input 2
HALL3	I	30	30	Digital Hall sensor input 3
Power factor correction				
PFCG0	O	-	24	PFC gate drive 0
PFCG1	O	-	25	PFC gate drive 1 (totem-pole PFC only)
IPFC	AIN	-	34	PFC current sensing
PFCREF	AIN	-	3	PFC Itrip comparator reference input
PFCITRIP	AIN	-	4	PFC Itrip comparator input
VAC1	AIN	-	2	VAC sense input line 1
VAC2	AIN	-	1	VAC sense input line 2
Interface				
DUTYFREQ	I	29	29	Duty/Frequency input
VSP	AIN	31	31	Analog speed reference input
PGOUT	O	25	25	Pulse output
PARAM	AIN	34	-	Parameter table selection, analog
NTC	AIN	35	35	External thermistor input
DIR	I	24	30	CW/CCW rotation direction input
RXD0	I	26	26	Serial port 0, device programming, receive input
TXD0	O	27	27	Serial port 0, device programming, transmit output
RXD1	I	1	-	Serial port 1, user communication, receive input
TXD1	O	2	-	Serial port 1, user communication, transmit output
Scripting[2]				
GPIO1	I/O	25	25	Digital I/O
GPIO2	I/O	28	28	Digital I/O
GPIO3	I/O	29	29	Digital I/O
GPIO4	I/O	30	-	Digital I/O
GPIO6	I/O	24	30	Digital I/O
GPIO7	I/O	1	-	Digital I/O
GPIO8	I/O	2	-	Digital I/O
GPIO9	I/O	3	-	Digital I/O
GPIO10	I/O	4	-	Digital I/O
AIN0	AIN	31	31	Analog input
AIN1	AIN	32	32	Analog input
AIN2	AIN	33	33	Analog input
AIN3	AIN	34	-	Analog input

(table continues…)

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2   GPIO29 is an internal MCE output connected to the gate driver enable input

2 Pin configuration

Table 1 **(continued) Pin definitions and functions**

Signal	Type	IMD111T	IMD112T	Description
AIN4	AIN	35	35	Analog input
AIN7	AIN	38	38	Analog input
AIN10	AIN	1	-	Analog input
AIN11	AIN	2	-	Analog input
TRIN0	I	25	25	TRIAC control input
TRIN1	I	34	-	TRIAC control input
TROUT0	O	4	-	TRIAC control output
TROUT1	O	30	30	TRIAC control output
SCL	O	26	26	I2C interface serial clock
SDA	I/O	27	27	I2C interface serial data
IR0	I	26	26	IR interface
IR1	I	1	-	IR interface
IR2	I	31	31	IR interface

2.3 Pin configuration drawing IMD111T

The drawings give the position of the functional pins for the available packages. Only the primary function of the respective pin is shown. Depending on the version of the Motion Control Engine (MCE) used pins might provide additional functionality which is given in the respective pin configuration tables.
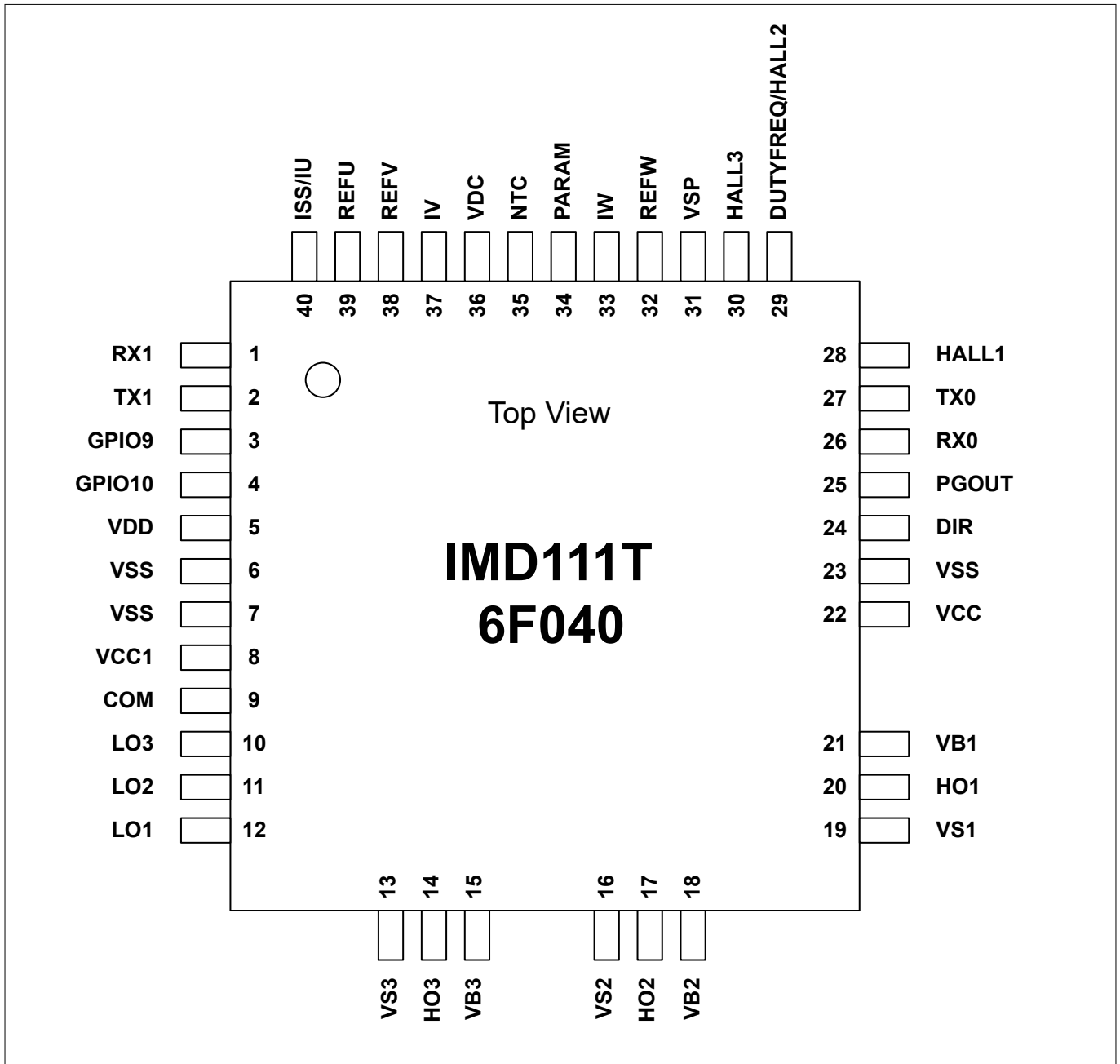
Figure 4   **IMD111T-6F040**

Pins that do not have any signal assigned are reserved for future use. Unused pins should be left unconnected and neither be connected to ground nor to the positive supply.

2.4 Pin configuration drawing IMD112T

The drawings give the position of the functional pins for the available packages. Only the primary function of the respective pin is shown. Depending on the version of the Motion Control Engine (MCE) used pins might provide additional functionality which is given in the respective pin configuration tables.
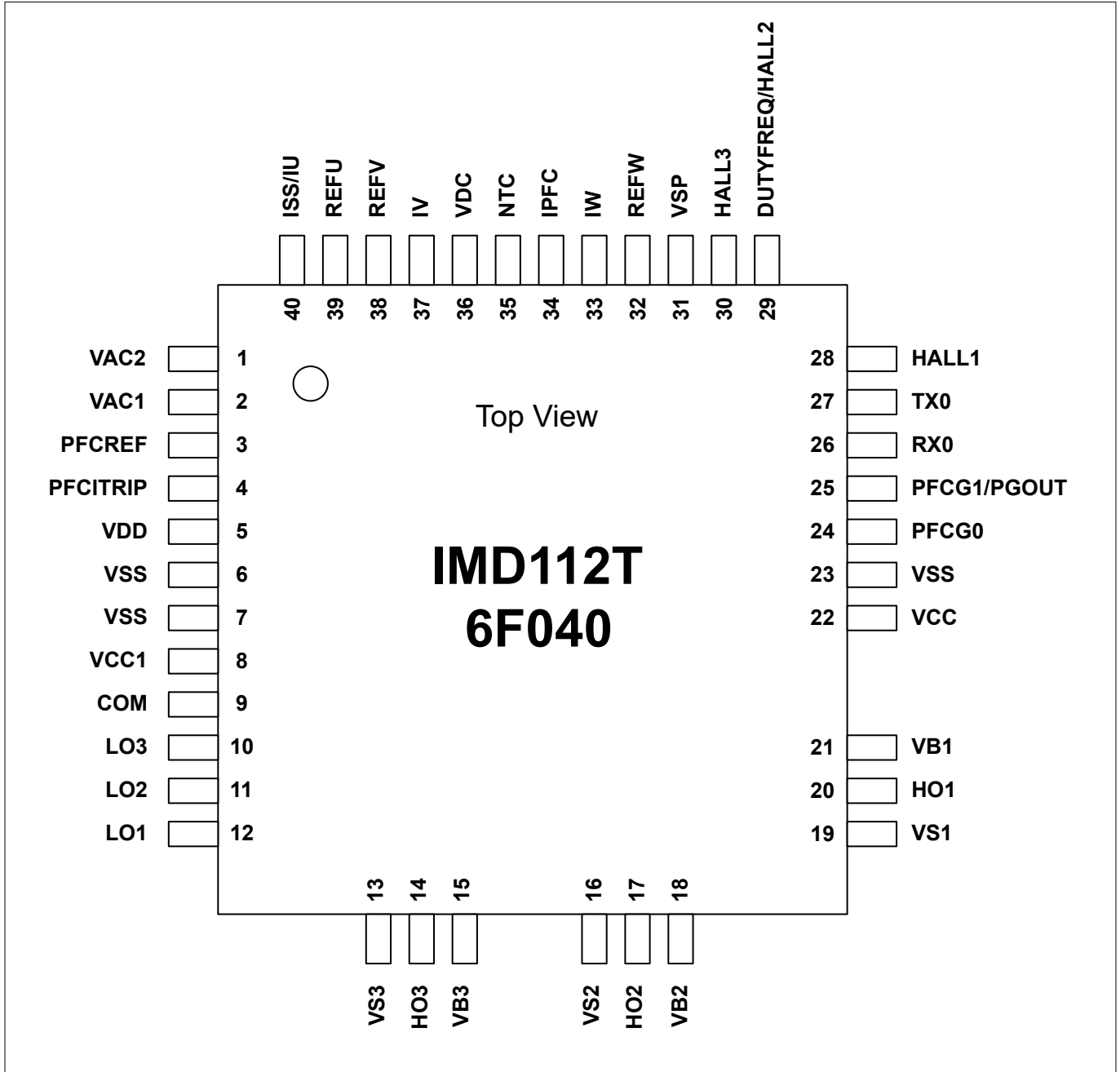

Figure 5   **IMD112T-6F040**

Pins that do not have any signal assigned are reserved for future use. Unused pins should be left unconnected and neither be connected to ground nor to the positive supply.

3 Functional description

3.1 Overview

The IMD111T/IMD112T integrates a controller, a high-voltage three-phase gate driver and a voltage regulator in a single package. The controller PWM outputs are internally connected to the gate driver inputs. Two controller digital pins are also connected to the gate driver enable input and fault output of the gate driver..

The integrated voltage regulator generates the controller 5V supply and can share the same 15V supply rail as the gate driver.

The package PG-LQFP-40-1 is footprint compatible to an industry standard LQFP-48 with pins removed for improved clearance and creepage.

3.2 Motion Control Engine

iMOTION™ IMD111T/IMD112T use the latest generation of the Motion Control Engine (MCE). The MCE is a ready-to-use solution for variable speed drives and contains all control functions to perform closed loop control of a three phase motor. Optionally, control of a power factor correction (PFC) is provided running in parallel to the motor.

Multiple configurable protections like over- and under-voltage, over current or rotor lock are integrated protecting the power stage as well as the motor itself.

iMOTION™ IMD111T/IMD112T supports the use in applications requiring functional safety according to IEC/UL 60730-1 ('Class B')

Using the MCE does not require any software development. Instead the MCE is configured for the concrete power stage configuration and motor type using PC based tools. Following parameter creation the behavior of the motor control loop can be monitored and fine tuned in real time. The respective tools are available for download from the iMOTION™ web pages.

For improved application flexibility the MCE contains a scripting engine running user scripts in the background task. Writing, downloading and monitoring scripts is supported by the above mentioned tools.

The MCE is driven by an internal temperature compensated oscillator that supports peripheral operation at 96 MHz and data processing at 48 MHz.

This data sheet provides all electrical, mechanical, thermal and quality parameters of the IMD111T/IMD112T. A more detailed description of the features and functionality of the MCE can be found in the respective reference manual. The MCE software images are made available for download from the Infineon web site. A special secure boot algorithm assures that these MCE software images can only be installed onto the matching hardware derivative, i.e. the product variant for which the software has been tested for.

3.3 Gate Driver

The integrated gate driver provides three high side and three low side drivers to control power devices like MOS-transistors or IGBTs in 3-phase systems such as variable speed drives. The gate drivers are based on SOI-technology which provides excellent ruggedness to transient voltages. The devices do not have parasitic thyristor structures so parasitic latch-up does not occur for any temperature or voltage condition.

The six independent drivers are controlled from the MCE PWM generator though internal connections. The device includes an under-voltage detection unit that monitors the driver voltage supplies. An under-voltage condition causes the driver to shut off all six switches. The error signal provided by the driver is internally connected to the MCE controller GK input pin to trip the MCE PWM generator. The gate driver enable input EN is internally connected to the MCE which allows the SW to manage the device power up sequencing.

The typical output currents can be up to 165 mA for pull-up and 375 mA for pull down. The MCE PWM generator introduces a deadtime between the high and low side signals but the gate driver introduces a fail safe 310 ns minimum dead time. The monolithic integrated bootstrap diode structures between pins VCC and VBx can be used to create the power supply for the high side circuits.

3.4 Low Side Supply (VCC, VSS and COM)

In the figure below, VCC is the low side supply for the gate driver which powers both the input logic and the low side output power stage. The under-voltage detection circuit Input logic is referenced to VSS ground. Output power stage is referenced to COM ground. COM ground is floating respect to VSS ground with a maximum range of operation of +/-5.7 V. A back-to-back zener structure protects grounds from noise spikes.

The under-voltage circuit enables the device to operate when the VCC supply voltage is higher than V_{CCUV+} . The IC shuts down all the gate drivers power outputs, when the VCC supply voltage is below V_{CCUV-}. This prevents the external power switches from critically low gate voltage levels during on-state and therefore from excessive power dissipation.
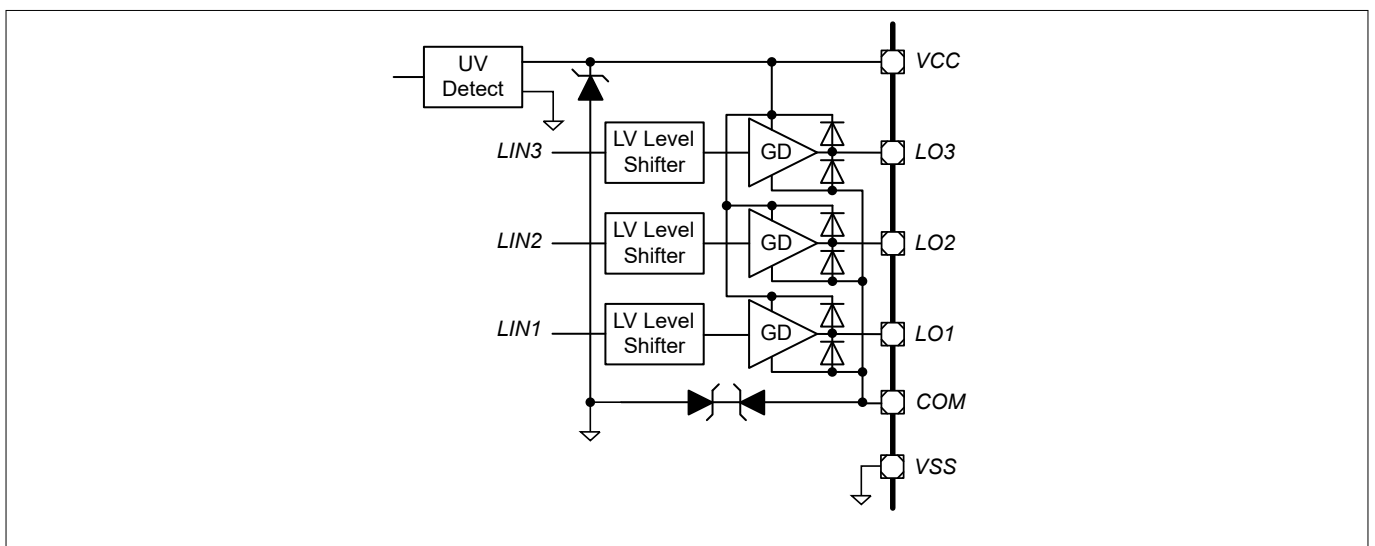
Figure 6   Low Side Driver circuit

3.5 High Side Supplies (VB1,2,3 and VS1,2,3)

Figure 7 shows the high side gate driver output circuit. VB to VS is the supply voltage supply for the high side gate driver. Each of the three high side circuits can float with respect to VSS following the external high side power device emitter/source voltage. The floating driver stage can be supplied by bootstrap topology using the internal diode connected between VB and VCC.

The device operating area as a function of the supply voltage is given in the Timing diagrams section under AC characteristics.
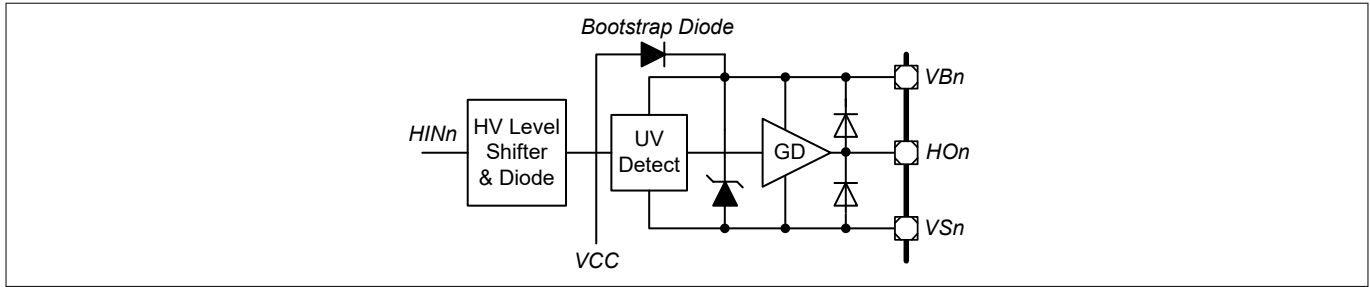
Figure 7   **High Side Driver circuit**

3.6   Low and High Side Outputs (LO1,2,3 and HO1,2,3)

Low side and high side power outputs are specifically designed for pulse operation such as gate drive of IGBT and MOSFET devices. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are edge triggered by the respective inputs. In particular, after an under voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after a under voltage condition of the VCC supply, the low side outputs switch to the state of their respective inputs.

3.7   Internal Voltage Regulator

The IMD111T/IMD112T contains a linear voltage regulator that can be used to generate the controller supply voltage from the gate driver supply. The regulator can also supply external components like sensors. The maximum current capability must be respected.

In order to maintain the stability of the control loop the regulator output requires an output capacitor CQ of at least 3.3 µF with a maximum permissible ESR of 2 Ω. It is recommended to use a multi layer ceramic capacitor for CQ with a nominal capacitance of 4.7 µF. Aluminum electrolytic as well as tantalum capacitors do not cover the required ESR range over the full operating temperature range. At the input of the regulator an input capacitor is necessary for compensating line influences (100 nF ceramic capacitor recommended). A resistor of approx. 1 Ω in series with CI can dampen oscillations that could occur due to the input inductivity and the input capacitor. If the regulator is sourced via long input lines of several meters it is recommended to place an additional electrolytic capacitor ≥ 47 µF at the input.

In case the integrated controller is supplied from an external source, the internal regulator can be disabled by connecting the respective input to ground.

3 Functional description
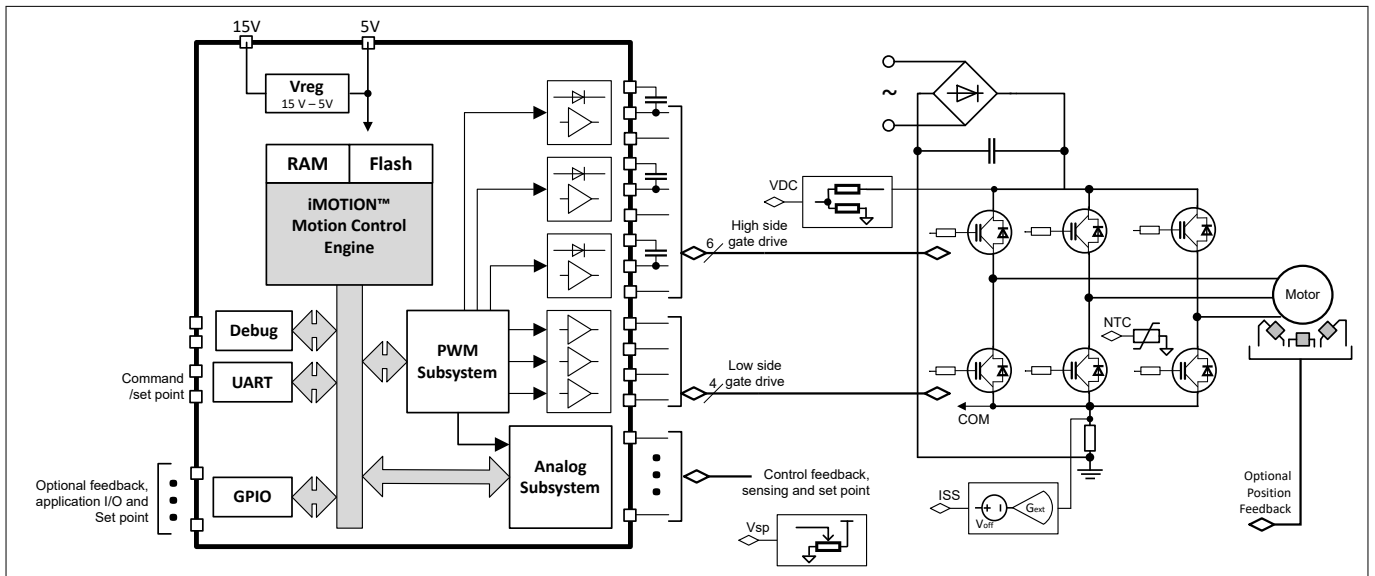
3.8 Application diagrams

Figure 8   **Application diagram single shunt**

4 Electrical characteristics and parameters

4.1 General parameters

4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the IMD111T/IMD112T and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**

  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the IMD111T/IMD112T and must be regarded for a system design.

- **SR**

  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the IMD111T/IMD112T is designed in.

4.1.2 Absolute maximum ratings

Stresses above the values listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2   **Absolute maximum ratings**

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	**Max.**		
Ambient temperature	T_A SR	-40	105	°C	
Junction temperature	T_J SR	-40	115	°C	Digital controller
		-40	125	°C	Gate driver, power transistors
Storage temperature	T_{ST} SR	-40	125	°C	
Lead temperature (soldering, 30 seconds)	T_L SR	---	260	°C	
Digital Controller voltage	V_{DD} SR	-0.3	6	V	
Controller digital and analog pin voltage	V_{ID} SR	-0.3	V_{DD}+0.3	V	
Input current on any controller pin during overload condition	I_{IN} SR	-10	10	mA	
Absolute sum of all controller input currents during overload condition	ΣI_{IN} SR	-50	50	mA	

(table continues...)

Table 2 **(continued) Absolute maximum ratings**

Parameter	Symbol	Values		Unit	Note or Test Condition
		Min.	**Max.**		
High side return offset voltage [3]	V_S SR	V_{CC}-V_{BS}-6	600	V	Voltage on high side gate driver return pins relative to the COM pin
High side return offset voltage (t_p< 500 ns, [3])	V_S SR	V_{CC} -V_{BS} – 50		V	
High side supply offset voltage [3]	V_B SR	V_{CC} – 6	620	V	Voltage on high side gate driver supply pins relative to the COM pin
High side supply offset voltage (t_p< 500 ns, [3])	V_B SR	V_{CC} – 50		V	
High side floating supply voltage (V_B vs. V_S) (internally clamped)	V_{BS} SR	-1	20	V	
High side output voltage (V_{HO} vs. V_S)	V_{HO} SR	-0.5	V_B + 0.5	V	
Gate drive low side supply voltage (internally clamped)	V_{CC} SR	-1	20	V	
Low side supply voltage ($_{VCC}$ vs. V_{COM})	V_{CCCOM} SR	-0.5	25	V	
Gate driver ground	V_{COM} SR	-5.7	5.7	V	relative to V_{SS}
Low side output voltage (V_{LO} vs. V_{COM})	V_{LO} SR	-0.5	V_{COM} + 0.5	V	
Offset voltage slew rate [4]	dV_S/dt CC	–	50	V/ns	

Note: *Characterized, not tested at manufacturing.*

Note: *Voltages referenced to V_{SS} if not stated otherwise*

4.1.3   Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The table below defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

•   full operation life-time is not exceeded
•   Operating Conditions are met for
     -    pad supply levels (V_{DD})
     -    temperature

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[3]   In case V_{CC} > V_B there is an additional power dissipation in the internal bootstrap diode between pins VCC and VBx. Insensitivity of bridge output to negative transient voltage up to –50V is not subject to production test – verified by design / characterization.

[4]   Not subject of production test, verified by characterization

4 Electrical characteristics and parameters

If a pin current is outside of the Operating Conditions but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 3   Overload Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	**Typ.**	**Max.**		
Input current on analog port pins during overload condition	I_{OVA} SR	-3	–	3	mA	
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input currents during overload condition	I_{OVS} SR	–	–	25	mA	

Figure 9 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DD} and ground are a simplified representation of these ESD protection structures.
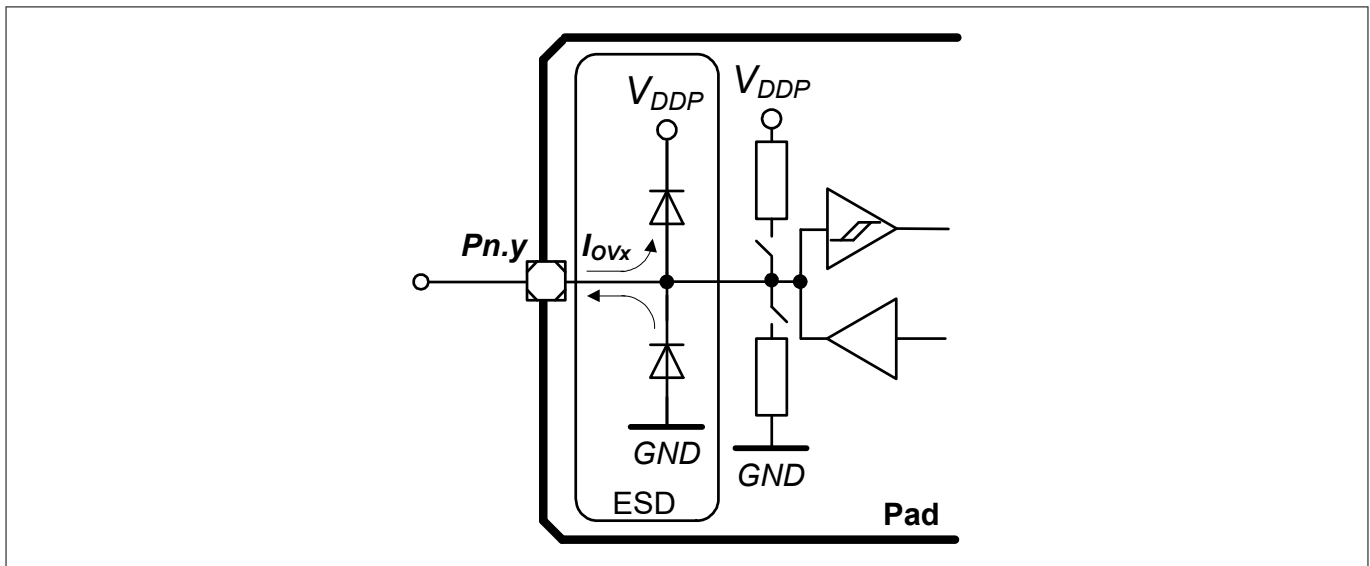
Figure 9   Input Overload Current via ESD structures

Table 4 and Table 5 list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the Absolute maximum ratings must not be exceeded during overload.

Table 4   PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DD} +(0.3 ... 0.5)$ V $V_{AIN} = V_{DD} + 0.5$ V $V_{AREF} = V_{DD} + 0.5$ V

Table 5   **PN-Junction Characterisitics for negative Overload**

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS}$ - (0.3 … 0.5) V
	$V_{AIN} = V_{SS}$ - 0.5 V
	$V_{AREF} = V_{SS}$ - 0.5 V

4.1.4   Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the IMD111T/IMD112T. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 6   **Recommended Operating Conditions**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	**Typ.**	**Max.**		
Ambient Temperature	T_A SR	-40	–	105	°C	
Junction temperature	T_J SR	-40	–	115	°C	
Positive DC Bus Input Voltage	V_{DCP} SR	12	-	400	V	
Gate Driver High Side Floating Supply Voltage	$V_{B1,2,3}$ SR	V_S + 5	-	V_S + 18	V	
Gate Driver Low Side Supply Voltage	V_{CC} SR	12	-	16.5	V	
Digital supply voltage[5]	V_{DD} SR	3.0	3.3	5.5	V	Internal voltage regulator disabled
Voltage regulator input voltage	V_{CC1} SR	5.5	–	20	V	

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5   All supply pins must be driven with the same voltage.

4.2 DC characteristics

4.2.1 Input/Output Characteristics

The table below provides the characteristics of the input/output pins of the controller.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.*

Table 7 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	$0.19 \times V_{DD}$	V	CMOS Mode
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DD}$	–	V	CMOS Mode
Input low voltage on port pins (Large Hysteresis, scripting pins only)	V_{ILPL}	SR	–	$0.08 \times V_{DD}$	V	CMOS Mode
Input high voltage on port pins (Large Hysteresis, scripting pins only)	V_{IHPL}	SR	$0.85 \times V_{DD}$	–	V	CMOS Mode
Output low voltage on port pins	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output high voltage on port pins	V_{OHP}	CC	V_{DD} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DD} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Rise/fall time on standard pad	t_R, t_F	CC	–	12	ns	50 pF @ 5 V
			–	15	ns	50 pF @ 3.3 V.
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up/-down resistor on port pins (if enabled in software)	R_{PUP}	CC	20	50	kΩ	$V_{IN} = V_{SS}$

(table continues...)

4 Electrical characteristics and parameters

Table 7   **(continued) Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input leakage current [6]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DD}$, T_A 105°C
Maximum current per pin standard pin	I_{MP}	SR	-10	11	mA	–
Maximum current into V_{DD} / out of V_{SS}	I_{MVDD} / I_{MVSS}	SR	–	260	mA	

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6   An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.

4.2.2 Analog to Digital Converter (ADC)

The following table shows the Analog to Digital Converter (ADC) characteristics. This specification applies to all analog input including the analog Hall sensor interface input (AHALLx+/AHALLx-, where x=1,2) as given in the pin configuration list.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 8 ADC Characteristics (Operating Conditions apply)[7]

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage range	V_{DD} SR	3.0	–	5.5	V	
Analog input voltage range	V_{AIN} SR	V_{SS}- 0.05	–	V_{DD}+ 0.05	V	
Conversion time	t_{C12} CC	–	1.0	–	µs	Defined by SW
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	
Sample time	t_{sample} CC	–	333	–	ns	Defined by SW
RMS noise	EN_{RMS} CC	–	1.5	–	LSB12	
DNL error	EA_{DNL} CC	–	±2.0	–	LSB12	
INL error	EA_{INL} CC	–	±4.0	–	LSB12	
Gain error	EA_{GAIN} CC	–	±0.5	–	%	
Offset error	EA_{OFF} CC	–	±8.0	–	mV	

4.2.3 Analog comparator characteristics

The table below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 9 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note or Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	includes common mode and differential input voltages
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	Defined by SW

---

[7] All parameters are defined for the full supply range if not stated otherwise.

4.2.4 Power Supply Current Controller

The total power supply current defined below consists of a leakage and a switching component for the voltage regulator and the controller through the V_{CC1} pin. The V_{CC} supply current is listed under the gate driver parameters.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 10   Power supply parameter table; V_{CC1} = 15V

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Active mode current motor control only	I_{DD1} CC	–	12	20	mA	$T_a = 25^oC$
Active mode current motor control plus PFC	I_{DD2} CC	–	16	20	mA	$T_a = 25^oC$

4.2.5 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 11   Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Data Retention Time	t_{RET} CC	10			years	Max. 100 erase / program cycles
Erase Cycles	N_{ECYC} CC			$5*10^4$	cycles	Sum of page and sector erase cycles a page sees
Total Erase Cycles	N_{TECYC} CC			$2*10^6$	cycles	

4 Electrical characteristics and parameters

4.2.6 Static parameters gate driver

Note: $V_{CC} = V_{BS} = 15V$ unless otherwise specified. All parameters valid for $T_a = 25\ ^oC$

Table 12 **Static parameter**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
High level output voltage, LO1,2,3	V_{OH}	–	V_{CC} -0.7		V	I_O = 20mA
High level output voltage, HO1,2,3			V_B -0.7		V	I_O = 20mA
Low level output voltage , LO1,2,3	V_{OL}	–	V_{COM}+ 0.2		V	I_O = -20mA
Low level output voltage , HO1,2,3	V_{OL}	–	V_S+ 0.2		V	I_O = -20mA
V_{CC} and V_{BS} supply undervoltage positive going threshold	V_{CCUV}+ V_{BSUV}+	8.3	9	9.8	V	–
V_{CC} and V_{BS} supply undervoltage negative going threshold	V_{CCUV}− V_{BSUV}−	7.5	8.1	8.8	V	–
V_{CC} and V_{BS} supply undervoltage lockout hysteresis	V_{CCUVH} V_{BSUVH}	0.5	0.9		V	V_S = 600V
High side leakage current betw. VS and VSS	I_{LVS+}	–	1	12.5	µA	V_S = 600V
High side leakage current betw. VS and VSS [8]	I_{LVS+}		10	–	µA	T_J = 125 ^oC, V_S = 600V
High side leakage current between VSx and VSy (x=1,2,3 and y=1,2,3)	I_{LVS-}	–	10	–	µA	T_J = 125 ^oC, $V_{Sx} – V_{Sy}$ = 600V
Quiescent current V_{BS} supply (VB only)	I_{QBS}	–	210	400	µA	–
Quiescent current V_{CC} supply (VCC only)	I_{QCC}	–	0.75	1.5	mA	
Mean output current for load capacity charging in range from 3 V (20%) to 6 V (40%)	I_{O+}	120	165	–	mA	C_L=10 nF
Peak output current turn on (single pulse) [8]	I_{Opk+}	–	240	–	mA	R_L = 0 Ω, t_p <10 µs
Mean output current for load capacity discharging in range from 12 V (80%) to 9 V (60%)	I_{O-}	250	375	–	mA	C_L=10 nF
Peak output current turn off (single pulse) [8]	I_{Opk-}	–	420		mA	R_L = 0 Ω, t_p <10 µs

(table continues...)

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[8] Not subject of production test, verified by characterization

Table 12 (continued) Static parameter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Bootstrap diode forward voltage between VCC and VB	$V_{F,BSD}$	–	1.0	1.3	V	I_F=0.5 mA
Bootstrap diode forward current between VCC and VB	$I_{F,BSD}$	-	50	-	mA	V_F=4 V
Bootstrap diode resistance	R_{BSD}	24	40	60	Ω	V_{F1}=4 V, V_{F2}=5 V

4.2.7 Static parameters voltage regulator

Table 13 Static parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input Voltage	V_{CC1}	5.5		20	V	
Output Voltage	V_Q	4.80	5.00	5.20	V	1 mA ≤ I_Q ≤ 30 mA
Output Current Limitation	I_{QExt}			10	mA	Total regulator output for external devices
Dropout Voltage[9]	V_{dr}	-	250	300	mV	I_Q = 20 mA
Output capacitor	C_Q	3.3	-	-	µF	ESR ≤ 2 Ω at 10 kHz
Load Regulation	ΔV_Q	-	17	50	mV	1 mA < I_Q < 25 mA; T_j = 25°C;
Line Regulation	ΔV_Q	-	10	25	mV	V_I = ($V_{Q,nom}$ + 0.5 V) to 36 V; I_Q = 1 mA; T_j = 25°C
Power Supply Ripple Rejection	PSRR	-	60	-	dB	f_r = 100 kHz ; V_r = 0.5 Vpp

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9   Measured when the output voltage VQ has dropped 100 mV from the nominal value.

4.3 AC characteristics

4.3.1 Testing Waveforms
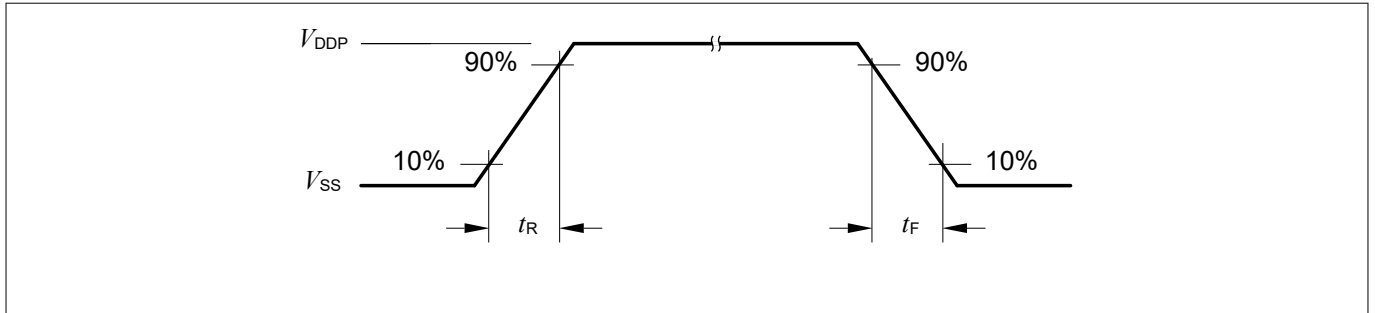

Figure 10   **Rise/Fall Time Parameters**

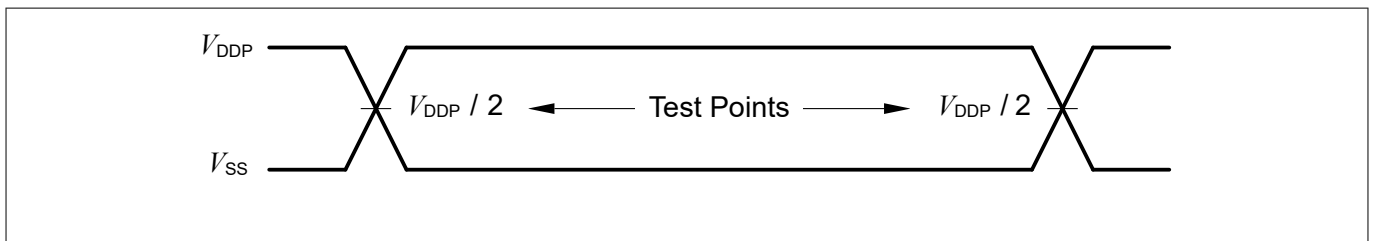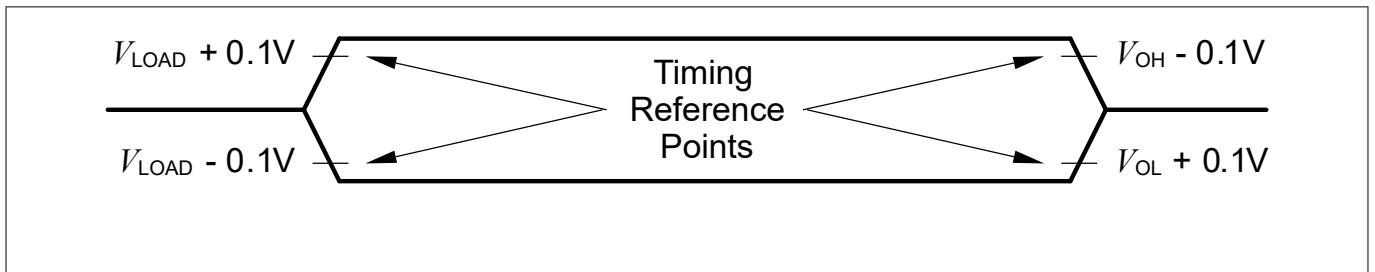**Figure 11**   **Testing Waveform, Output Delay**

Figure 12   **Testing Waveform, Output High Impedance**

4.3.2 Power-Up and Supply Threshold Characteristics

This chapter provides the characteristics of the supply threshold for the controller.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DD} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: *These parameters are not subject to production test, but verified by design and/or characterization.*

Note: *Operating Conditions apply.*

4 Electrical characteristics and parameters

Table 14　　　　　**Power-Up and Supply Threshold Parameters**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	**Typ.**	**Max.**		
V_{DD} ramp-up time	t_{RAMPUP} SR	$V_{DD}/S_{VDDrise}$	–	10^7	µs	
V_{DD} slew rate	S_{VDDOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDD10} SR	0	–	10	V/µs	Slope during fast transient within +/-10% of V_{DD}
	$S_{VDDrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDfall}$[10] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[11]
V_{DD} prewarning voltage	V_{DDPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B
V_{DD} brownout reset voltage	V_{DDBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DD} voltage to ensure defined pad states	V_{DDA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} CC	–	260	–	µs	Time to the first user code instruction[12]
Start-up time to PWM on	t_{PWMON} CC	5.2	-	360	ms	Time to PWM enabled

Figure 13　　　　　**Supply Threshold Parameters**

---

[10] A capacitor of at least 100 nF has to be added between VDD and VSS to fulfill the requirement as stated for this parameter.

[11] Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

[12] This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 48 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

4.3.3 On-Chip Oscillator Characteristics

Table 15 provides the characteristics of the 96 MHz digital controlled oscillator DCO1. The DCO1 is used as the time base during normal operation.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 15   96 MHz DCO1 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	**Typ.**	**Max.**		
Nominal frequency	f_{NOM} CC	-	96	-	MHz	under nominal conditions after trimming
Accuracy with adjustment algorithm [13] based on temperature sensor	Δf_{LTTS} CC	-0.6	–	+0.6	%	with respect to f_{NOM}(typ), T_A from 0°C to 105°C
		-1.9	–	+1.0	%	with respect to f_{NOM}(typ), T_A from -25 °C to 105°C
		-2.6	–	+1.3	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C
Accuracy	Δf_{LT} CC	-1.7	–	+3.4	%	with respect to f_{NOM}(typ), T_A from 0 ° C to 85 °C
		-3.9	–	+4.0	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C

Table 16 provides the characteristics of the 32 kHz digital controlled oscillator used internally as a secondary clock source for the internal watchdog.

Table 16   32 kHz DCO2 Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	**Typ.**	**Max.**		
Nominal frequency	f_{NOM} CC	-	32.75	-	kHz	under nominal conditions[14] after trimming
Accuracy	Δf_{LT} CC	-1.7	–	+3.4	%	with respect to f_{NOM}(typ), T_A from 0 ° C to 85 °C
		-3.9	–	+4.0	%	with respect to f_{NOM}(typ), T_A from -40° C to 105 °C

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[13]   MCE version newer or equal to V1.03.00, clock adjustment algorithm for improved accuracy enabled
[14]   The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25°C.

4.3.4 Dynamic parameters gate driver

$V_{CC} = V_{BS} = 15$ V, $V_S = V_{SS} = V_{COM}$ unless otherwise specified. All parameters are valid for $T_a = 25$ °C.

Table 17 **Dynamic parameters**

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	**Typ.**	**Max.**		
Turn-on propagation delay	t_{on}	400	530	800	ns	
Turn-off propagation delay	t_{off}	400	530	800	ns	
Turn-on rise time	t_r	–	60	100	ns	$C_L = 1$ nF
Turn-off fall time	t_f	–	26	45	ns	$C_L = 1$ nF
Dead time	DT	150	310	–	ns	
Matching delay ON, max(ton)-min(ton), ton are applicable to all 6 driver outputs	MT_{ON}	–	20	100	ns	
Matching delay OFF, max(toff)-min(toff), toff are applicable to all 6 driver outputs	MT_{OFF}	–	40	100	ns	
Output pulse width matching. P_{win}-P_{Wout}	PM	–	10	100	ns	

4 Electrical characteristics and parameters

4.3.5 Timing diagrams
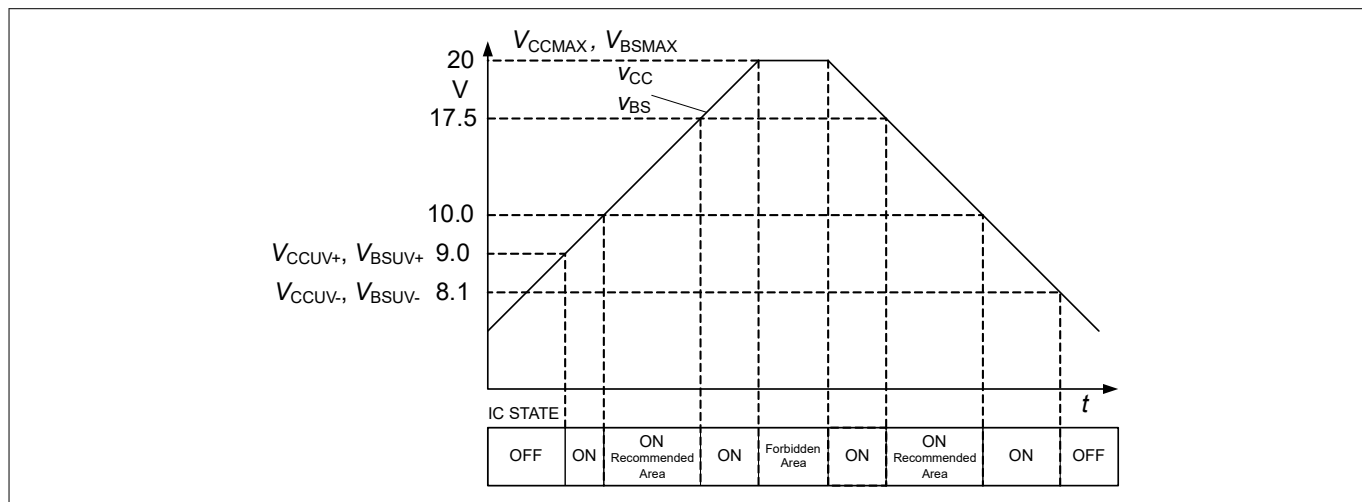
Figure 14   **Operating Areas**

4.4 Motor Control Parameters

The following values are given for reference only. Concrete parameters are defined in the iMOTION™ Motion Control Engine (MCE) software.

4.4.1 PWM Characteristics

Table 18   **Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Motor PWM Frequency[15]	f_{PWM}	5	16	40	kHz	

4.4.2 Current Sensing

Table 19   **Motor Current Sensing**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Input range	I_{PWM}	V_{SS}-0.05	-	V_{DD}+0.05	V	
Configurable analog gain		-	1/ 3/ 6/ 12	-		
Itrip input range	$I_{PWMTRIP}$	V_{SS}-0.05	-	V_{DD}+0.05	V	
Itrip offset		-	±8	-	mV	
Input capacitance	C_{REF}	-	-	10	pF	REFU, REFV, REFW capacitor

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[15]   Actual min. and max. limits defined in resp. software version

4.4.3   Fault Timing
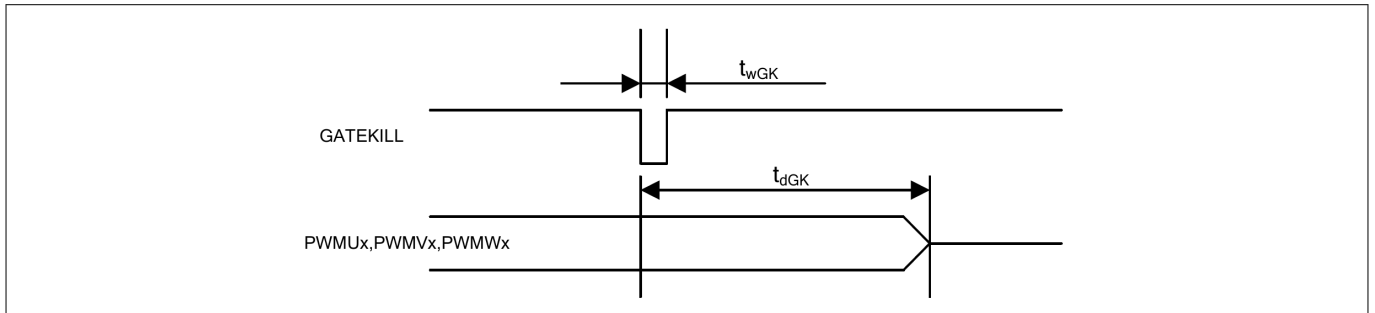
Figure 15   Fault timing

Table 20   Gatekill timing

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
GK pulse width	t_{wGK}	1	-	-	µs	
GK input to PWM shutoff	t_{GK}	-	1.3	-	µs	
Motor Fault reset timing	t_{RESET}	-	1.84	-	ms	fault reset command via UART to PWM reactivation
MCE digital ITRIP filter window	t_{PWMOFF}	0.075	1.0	10	µs	Configurable in software

Note: The ITRIP filter window must be configured according to the rated short circuit withstand time of the respective power stage taking into consideration any delay in external circuitry. For iMOTION™ devices with integrated power stage the value is specified in the Absolute maximum ratings of the device.

4.5 Power Factor Correction (PFC) parameters

The parameters specified for the power factor correction only refer to products that have the respective control algorithm integrated. The PFC switching frequency is configurable and the range depends on the concrete firmware version.

4.5.1 Boost PFC characteristics

Table 21   **Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	20	50	kHz	MCE rev. 1.3
		-	40	120	kHz	MCE rev. 5.1

4.5.2 Totem Pole PFC characteristics

Table 22   **Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
PFC frequency	f_{PFC}	-	40		kHz	Max defined by SW

4.5.3 PFC Current Sensing

The current sensing specification applies to both PFC algorithms, boost mode and totem pole.

Table 23   **PFC Current Sensing**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Input range	I_{PFC}	V_{SS}- 0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Configurable analog gain		-	1/ 3/ 6/ 12	-		
PFC Itrip input range	$I_{PFCTRIP}$	V_{SS}-0.05	-	V_{DD}+ 0.05	V	V_{DD}= 3.3 or 5.0 V
Itrip offset		-	± 3	-	mV	Input voltage difference > 200mV
Input capacitance	C_{REF}	-	-	10	pF	PFCREF capacitor

4.5.4 PFC Fault Timing

Table 24   **PFC Fault timing**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Itrip to PFC PWM shutoff	t_{PFCOFF}	-	1.18	-	µs	

(table continues…)

4 Electrical characteristics and parameters

Table 24   **(continued) PFC Fault timing**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
PFC fault reset timing	t$_{RESET}$	-	1.0	-	ms	fault reset command via UART to PWM reactivation

4.6 Device Interfaces

iMOTION™ devices provide several interfaces to either control the motor drive in the application or report back its status. The availability of a specific interface depends upon the concrete device chosen as well as the version of the Motion Control Engine (MCE) applied. The following sections and tables specify these interfaces as well as the respective limits. The configuration settings for these interfaces are described in the MCE Reference Manual.

Note: *These parameters are not subject to production test, but verified by design and/or characterization. Operating conditions apply.*

4.6.1 UART Interface

The UART interface is configured as given below.

Table 25   **Electrical characteristics**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
UART baud rate		1200	57600	-	Bps	
UART mode		-	8-N-1	-		data-parity-stop bit
UART sampling filter period [16]	$T_{UARTFIL}$	-	1/16	-	T_{BAUD}	
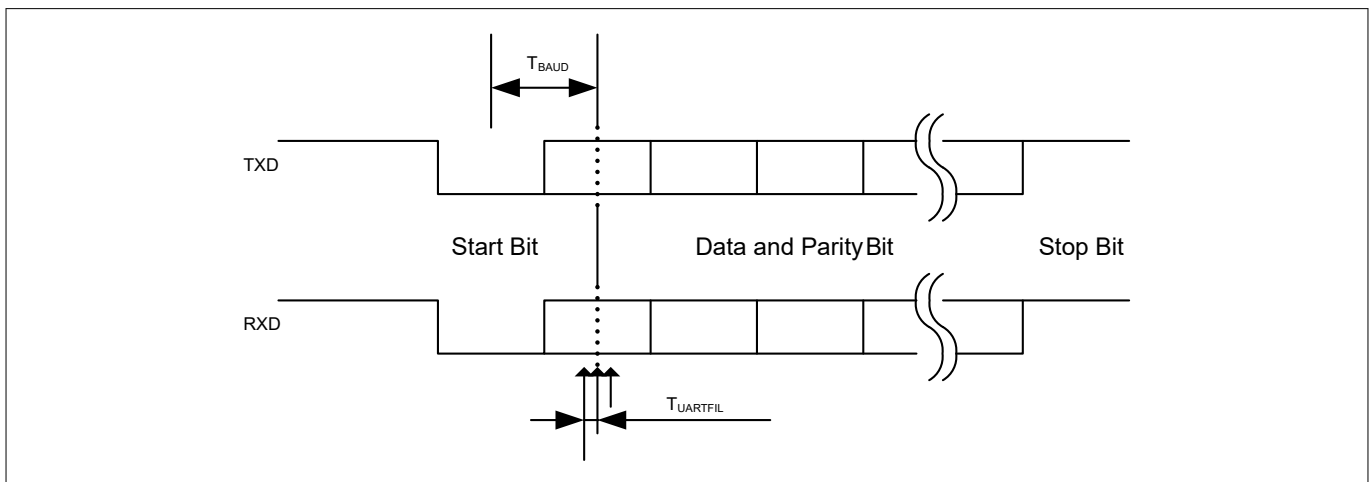
Figure 16   **UART timing**

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[16]   Each bit including start and stop bit is sampled three times at center of a bit at an interval of 1/16 T_{BAUD}. If three sampled values do not agree, then UART noise error is generated.

4 Electrical characteristics and parameters

4.6.2 Analog Speed Input
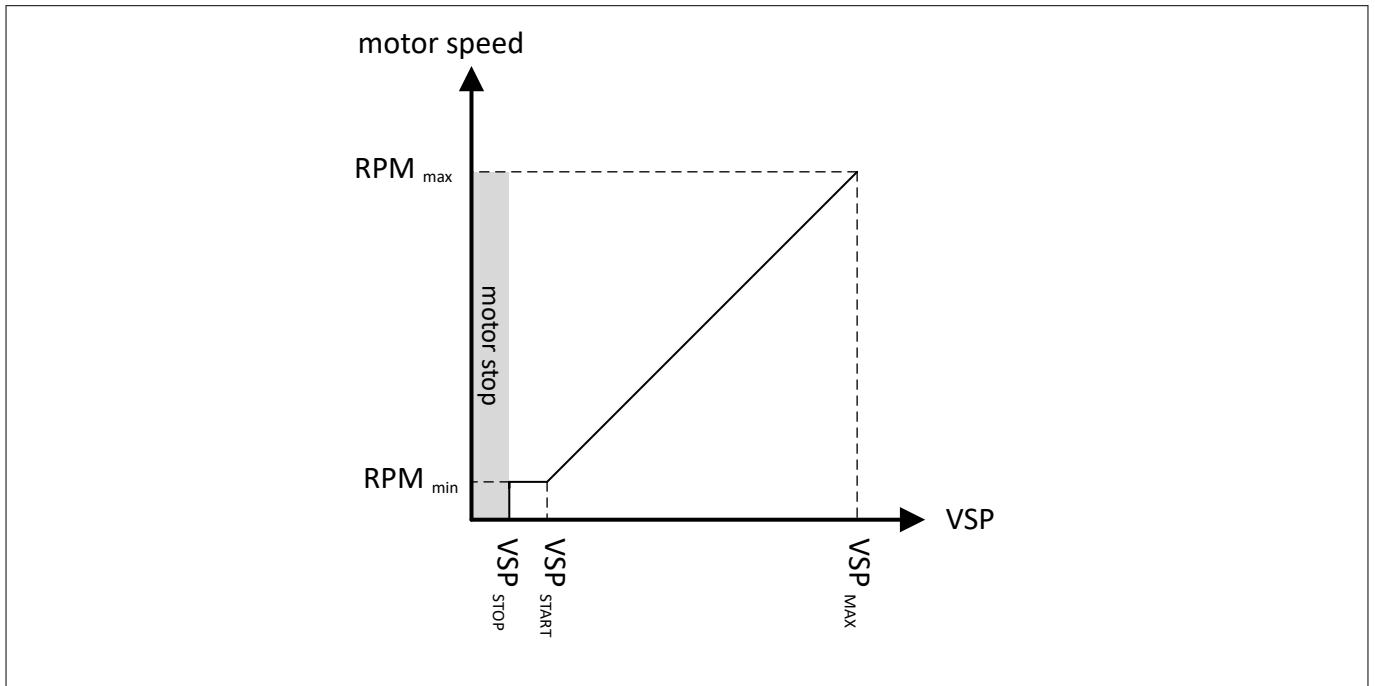
Figure 17 VSP analog control mode

Table 26 Analog Speed Control Voltage (VSP)

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Motor start voltage	VSP_{START}	-	1.2	-	V	Configured VSP_{START}=1.0V
Motor stop voltage	VSP_{STOP}	-	1.0	-	V	Configured VSP_{STOP}=1.0V
Motor max voltage	VSP_{MAX}	-	4.9	4.95	V	V_{DD}=5.0V
VSP active to PWM start	t_{START}	-	44	-	ms	
VSP inactive to PWM stop	t_{STOP}	-	16	-	ms	

4.6.3 Frequency Input

In frequency input control mode, the motor operations like motor start, motor stop and speed change are controlled by applying a square wave frequency signal on a digital input pin.
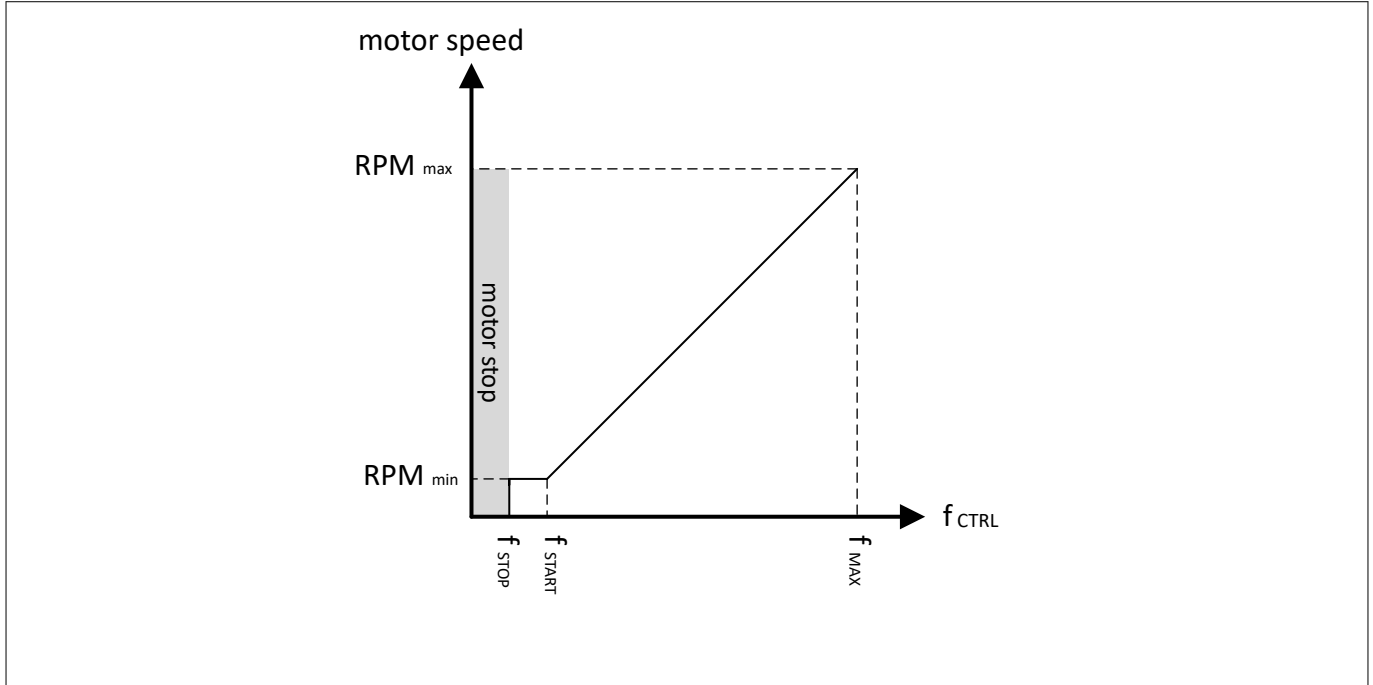
Figure 18   **Frequency input control mode**

Table 27   **Frequency Control Mode**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Motor start frequency	f_{START}	-	100	360	Hz	$f_{START} > f_{STOP}$
Motor stop frequency	f_{STOP}	-	50	-	Hz	
Motor max speed frequency	f_{MAX}	-	-	1000	Hz	
Frequency input duty cycle	T_{DUTY}	10	-	90	%	

4.6.4 Duty Cycle Input

In duty cycle input control mode, the motor operations like motor start, stop and speed change are controlled by varying the duty cycle of a rectangular wave signal on a digital input pin.
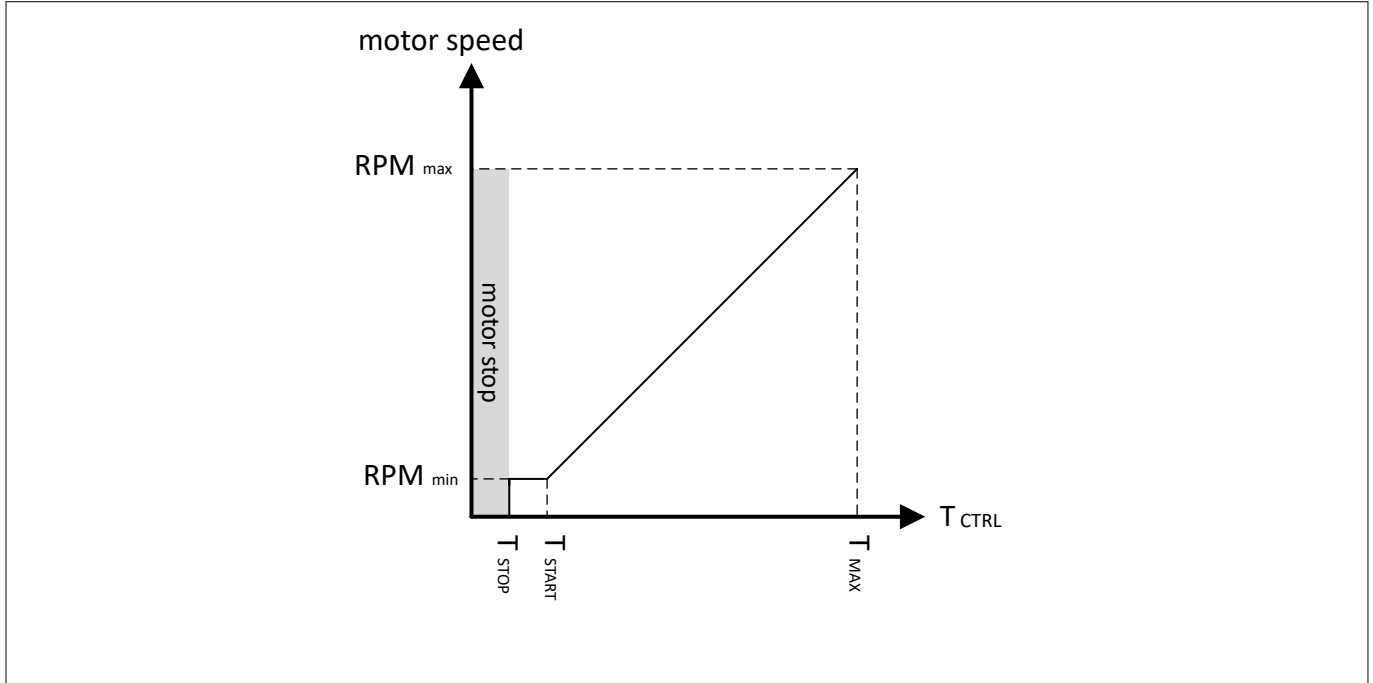
Figure 19 **Duty cycle input control mode**

Table 28 **Duty Cycle Control Mode**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Input signal frequency	f_{DUTY}	5	1000	20000	Hz	
Motor start duty cycle	T_{START}	-	10	-	%	$T_{START} > T_{STOP}$
Motor stop duty cycle	T_{STOP}	-	5	-	%	
Motor max duty cycle	T_{MAX}	-	95	-	%	

4.6.5 Over Temperature Input

The over temperature input can be used to continuously monitor an external temperature sensor like an NTC.

Table 29   **Over Temperature Input**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Over Temperature to PWM shutdown	t_{OT}		1.0	2.1	ms	

4.6.6 Pulse Output

The IMD111T/IMD112T series can generate a square wave pulse output in sync with the motor rotation which can be used to monitor the motor speed. The number of pulses to be generated for a full rotation can be configured.

Table 30   **Pulse Output**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Pulses per Rotation	PPR	4	-	24		
Pulse duty cycle	t_{PPR}	-	50	-	%	

4.6.7 LED Output

The IMD111T/IMD112T series provides an output that can be connected to an LED to give a visual indication of the status of the motor drive.

Table 31   **LED Output**

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	**Typ.**	**Max.**		
Fault to LED delay	$t_{LEDFAULT}$	-	53	-	ms	
Fault reset to LED delay	$t_{LEDRESET}$	-	1.84	-	ms	
LED blinking frequency	f_{LED}	1		1000	Hz	
LED blinking duty cycle	t_{LED}	5		95	%	

5 Device and package specifications

5.1 Quality declaration

Table 32 **Quality Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	**Max.**		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	2000	V	ANSI/ESDA/JEDEC-JS-001
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	–	1000	V	ANSI/ESDA/JEDEC-JS-002
Moisture sensitivity level	MSL CC	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	260	°C	JEDEC J-STD-020D

5.2 SBSL and Chip-IDs

The table below gives the IDs for the individual devices in the IMD111T/IMD112T family. Depending upon the mode either the SBSL-ID (secure boot loader) or the Chip-ID should be used to identify the device. For details refer to the Reference Manual or the iMOTION™ Programming Manual.

Table 33 **SBSL-IDs and Chip-IDs**

Product Type	Package	Chip-ID	SBSL-ID
IMD111T-6F040	LQFP-40	0x21110007	0242dca3b8d9690b68bf429211856693
IMD112T-6F040	LQFP-40	0x21120007	02309452a88ab5cb112fc4cfa84dcedc

5.3 Thermal considerations

Table 34 **Thermal characteristics of the packages**

Parameter	Symbol	Limit values		Unit	Package types
		Min.	**Max.**		
Thermal resistance Junction-Ambient[17]	$R_{\Theta JA}$ CC	-	100.0	K/W	PG-LQFP-40-1

When operating the IMD111T/IMD112T in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed the value specified under Absolut Maximum Ratings.

The difference between junction temperature and ambient temperature is determined by

$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as

$P_{INT} = V_{DD} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as

$P_{IOSTAT} = \Sigma((V_{DD} - V_{OH}) \times I_{OH}) + \Sigma(V_{OL}I_{OL})$

---

[17] Device mounted on a 4-layer JEDEC board (JESD 51-5).

5 Device and package specifications

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

• Reduce V_{DD}, if possible in the system
• Reduce the system frequency
• Reduce the number of output pins
• Reduce the load on active output drivers

5.4 Package Outline PG-LQFP-40-1
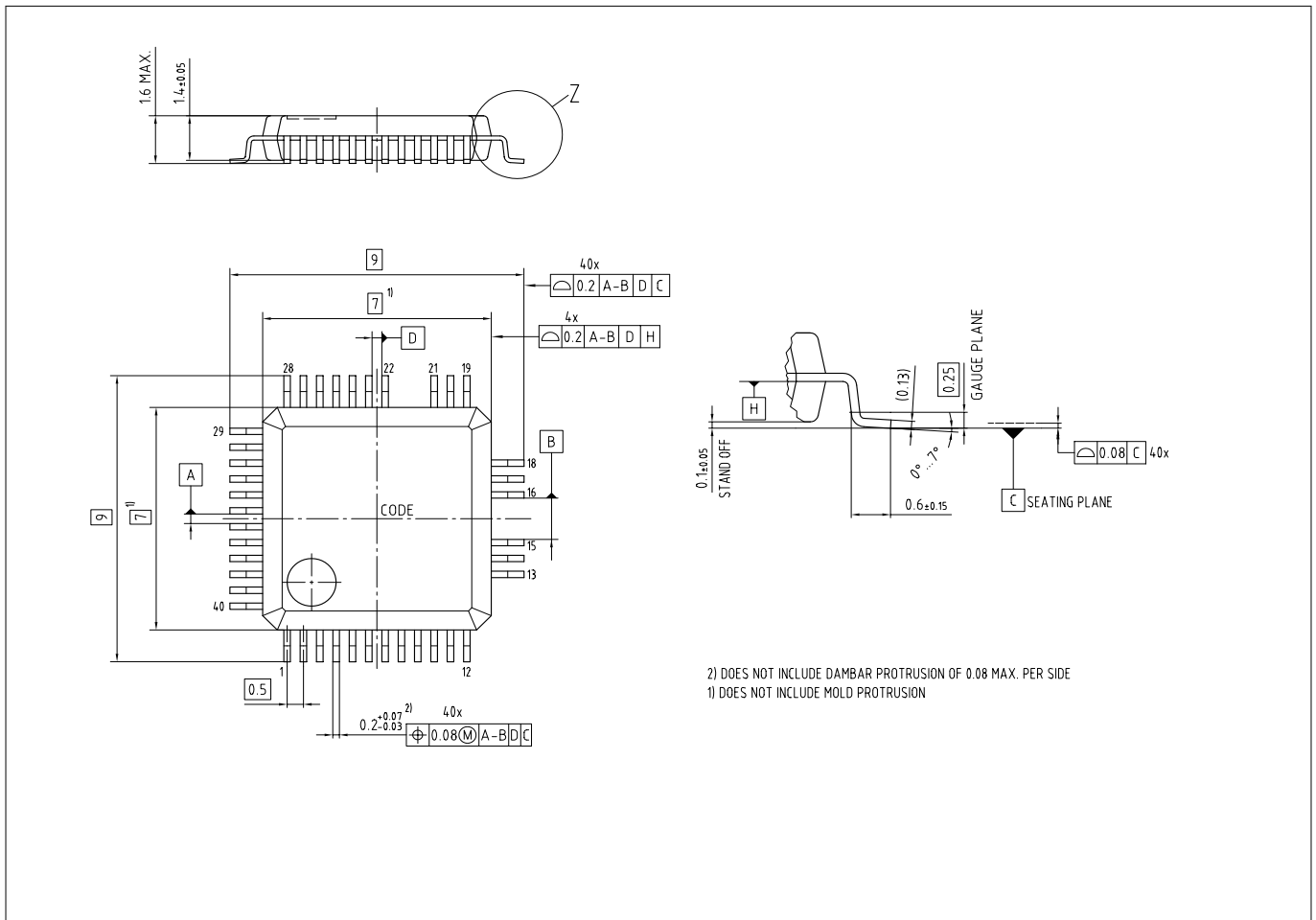
Figure 20 **PG-LQFP-40-1**

5.5 Part marking information
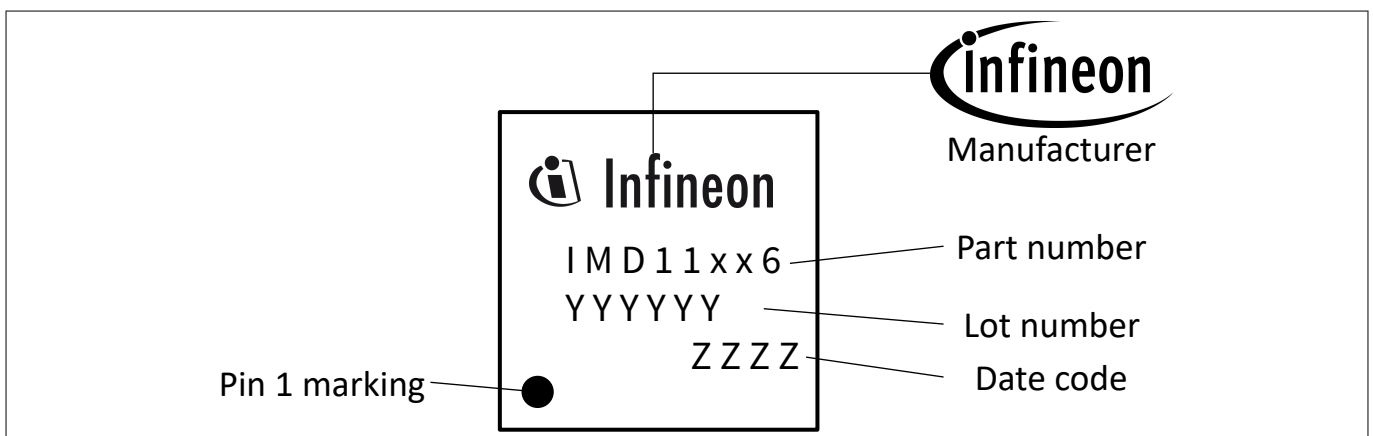
Figure 21 **Part marking**

Revision history

Document version	Date of release	Description of changes
1.0	2020-12-4	• Initial release
1.1	2023-09-13	• Infrared pins added • peak output currents not measured in production • $I_{F,BSD}$ only typical value (PCN-2023-154-A) • New features pin mapping of TRIAC/I2C/IR added

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