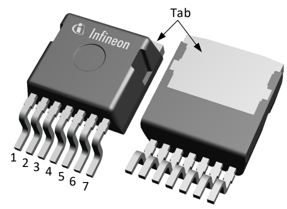
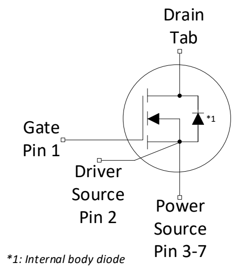
CoolSiC™ M1

CoolSiC™ MOSFET 650 V G1

PG-TO263-7



The 650 V CoolSiC™ is built over the solid silicon carbide technology developed in Infineon in more than 20 years. Leveraging the wide bandgap SiC material characteristics, the 650V CoolSiC™ MOSFET offers a unique combination of performance, reliability and ease of use. Suitable for high temperature and harsh operations, it enables the simplified and cost effective deployment of the highest system efficiency.



Features

- Optimized switching behavior at higher currents
- Commutation robust fast body diode with low Q_{fr}
- Superior gate oxide reliability
- $T_{j,max}$=175°C and excellent thermal behavior
- Lower $R_{DS(on)}$ and pulse current dependency on temperature
- Increased avalanche capability
- Compatible with standard drivers
- Kelvin source provides up to 4 times lower switching losses

Benefits

- Unique combination of high performance, high reliability and ease of use
- Ease of use and integration
- Suitable for topologies with continuous hard commutation
- Higher robustness and system reliability
- Efficiency improvement
- Reduced system size leading to higher power density

Potential applications

- Telecom and Server SMPS
- UPS (uninterruptable power supplies)
- Solar PV inverters
- EV charging infrastructure
- Energy storage and battery formation
- Class D amplifiers

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ T_J = 25 °C	650	V
$R_{DS(on),typ}$	57	mΩ
$R_{DS(on),max}$	74	mΩ
$Q_{G,typ}$	28	nC
$I_{DM,max}$	84	A
Q_{oss} @ 400 V	65	nC
E_{oss} @ 400 V	9.8	µJ

Type/Ordering Code	Package	Marking	Related Links
IMBG65R057M1H	PG-TO263-7	65R057M1	see Appendix A

Table of Contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Note: for optimum lifetime and reliability, Infineon recommends operating conditions that do not exceed 80% of the maximum ratings stated in this datasheet.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous DC drain current [1]	I_{DDC}	-	-	39 28	A	T_c = 25 °C T_c = 100 °C
Peak drain current [2]	I_{DM}	-	-	84	A	T_c = 25 °C, V_{GS} = 18 V
Avalanche energy, single pulse	E_{AS}	-	-	142	mJ	I_D = 5.3 A, V_{DD} = 50 V; see table 11
Avalanche energy, repetitive	E_{AR}	-	-	0.71	mJ	I_D = 5.3 A, V_{DD} = 50 V; see table 11
Avalanche current, single pulse	I_{AS}	-	-	5.3	A	-
MOSFET *dv/dt* ruggedness	*dv/dt*	-	-	200	V/ns	V_{DS}= 0...400 V
Gate source voltage (static) [3]	V_{GS}	-5	-	23	V	-
Gate source voltage (transient)	V_{GS}	-7	-	25	V	$t_{pulse} \leq$ 1% duty cycle/f_{sw}
Power dissipation	P_{tot}	-	-	161	W	T_c = 25 °C
Storage temperature	T_{stg}	-55	-	150	°C	-
Operating junction temperature	T_j	-55	-	175	°C	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous reverse drain current [1]	I_{SDC}	-	-	39 26	A	V_{GS} = 18 V, T_c = 25 °C V_{GS} = 0 V, T_c = 25 °C
Peak reverse drain current [2]	I_{SM}	-	-	84	A	T_c = 25 °C, $t_p \leq$ 250 ns
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms}, T_c = 25 °C, t = 1 min

[1] Limited by $T_{j,max}$.

[2] Pulse width t_{pulse} limited by $T_{j,max}$.

[3] The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{th(j-c)}$	-	-	0.93	°C/W	-
Thermal resistance, junction - ambient	$R_{th(j-a)}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient, SMD version	$R_{th(j-a)}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

3 Operating range

Table 4 Operating range

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate-source voltage operating range including undershoots [4)]	V_{GS}	-2	-	20	V	-
Recommended turn-on voltage	$V_{GS(on)}$	-	18	-	V	-
Recommended turn-off voltage	$V_{GS(off)}$	-	0	-	V	-

4)

Important notice: If the gate source voltage of the device in application exceeds the operating range (Table 4), the device $R_{DS,on}$ and $V_{GS(th)}$ might exceed the maximum value stated in the datasheet at the end of the lifetime of the device. In order to ensure sound operation of the device over the planned lifetime, the maximum ratings (Table 2) and the CoolSiC™ MOSFET 650V M1 trench power device application note AN_1907_PL52_1911_144109 must be considered.

4 Electrical characteristics

at T_j = 25 °C, unless otherwise specified

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source voltage	V_{DSS}	650	-	-	V	V_{GS} = 0 V, I_D = 0.5 mA
Gate threshold voltage [5]	$V_{GS(th)}$	3.5	4.5	5.7	V	V_{DS} = V_{GS}, I_D = 5 mA
Zero gate voltage drain current	I_{DSS}	-	1 3	100 -	µA	V_{DS} = 650 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 650 V, V_{GS} = 0 V, T_j = 175 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS} = 20 V, V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	57 80	74 -	mΩ	V_{GS} = 18 V, I_D = 16.7 A, T_j = 25 °C V_{GS} = 18 V, I_D = 16.7 A, T_j =175 °C
Internal gate resistance	$R_{G,int}$	-	8.0	-	Ω	f = 1 MHz

5) Tested after 1 ms pulse at V_{GS} = +20 V.

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	930	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Reverse transfer capacitance	C_{rss}	-	10.7	-	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Output capacitance [6]	C_{oss}	-	107	139	pF	V_{GS} = 0 V, V_{DS} = 400 V, f = 250 kHz
Output charge [6]	Q_{oss}	-	65	84	nC	calculation based on C_{oss}
Effective output capacitance, energy related [7]	$C_{o(er)}$	-	122	-	pF	V_{GS} = 0 V, V_{DS} = 0...400 V
Effective output capacitance, time related [8]	$C_{o(tr)}$	-	162	-	pF	I_D = constant, V_{GS} = 0 V, V_{DS} = 0...400 V
Turn-on delay time	$t_{d(on)}$	-	6.4	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 16.7 A, $R_{G,ext}$ = 1.8 Ω; see table 10
Rise time	t_r	-	8.8	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 16.7 A, $R_{G,ext}$ = 1.8 Ω; see table 10
Turn-off delay time	$t_{d(off)}$	-	13.6	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 16.7 A, $R_{G,ext}$ = 1.8 Ω; see table 10
Fall time	t_f	-	7.0	-	ns	V_{DD} = 400 V, V_{GS} = 0/18 V, I_D = 16.7 A, $R_{G,ext}$ = 1.8 Ω; see table 10

6) Maximum specification is defined by calculated six sigma upper confidence bound.

7) $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V.

8) $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Plateau gate to source charge	$Q_{GS(pl)}$	-	7	-	nC	V_{DD} = 400 V, I_D = 16.7 A, V_{GS} = 0 to 18 V
Gate to drain charge	Q_{GD}	-	6	-	nC	V_{DD} = 400 V, I_D = 16.7 A, V_{GS} = 0 to 18 V
Total gate charge	Q_G	-	28	-	nC	V_{DD} = 400 V, I_D = 16.7 A, V_{GS} = 0 to 18 V

Table 8 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source reverse voltage	V_{SD}	-	4.0	-	V	V_{GS} = 0 V, I_S = 16.7 A, T_j = 25 °C
MOSFET forward recovery time	t_{fr}	-	19.4	-	ns	V_{DD} = 400 V, I_S = 16.7 A, di_S/dt = 1000 A/µs; see table 9
MOSFET forward recovery charge [9]	Q_{fr}	-	69	-	nC	V_{DD} = 400 V, I_S = 16.7 A, di_S/dt = 1000 A/µs; see table 9
MOSFET peak forward recovery current	I_{frm}	-	6.7	-	A	V_{DD} = 400 V, I_S = 16.7 A, di_S/dt = 1000 A/µs; see table 9

9) Q_{fr} includes Q_{oss}.

5 Electrical characteristics diagrams

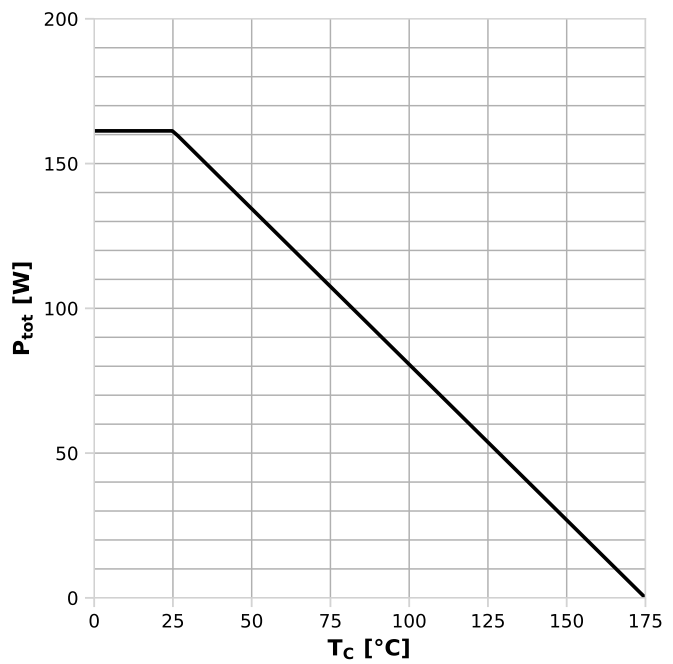
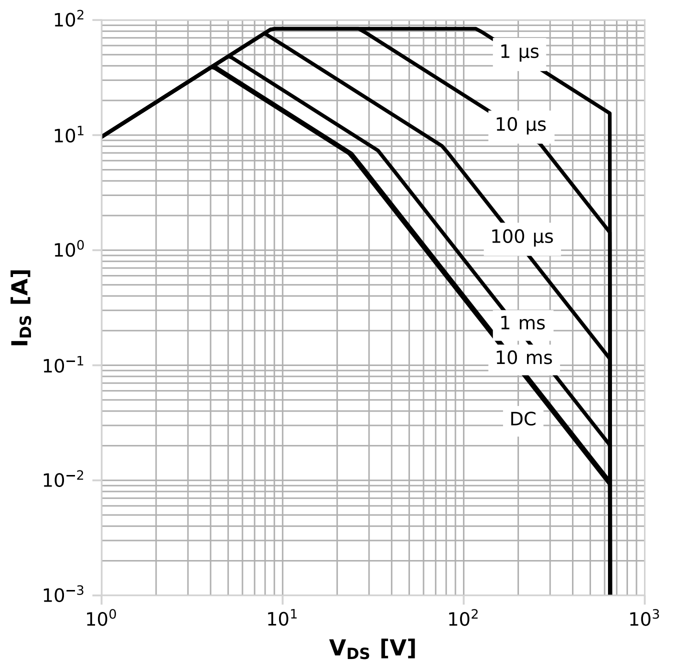
Diagram 1: Power dissipation	Diagram 2: Safe operating area
	
$P_{tot}=f(T_C)$	$I_{DS}=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

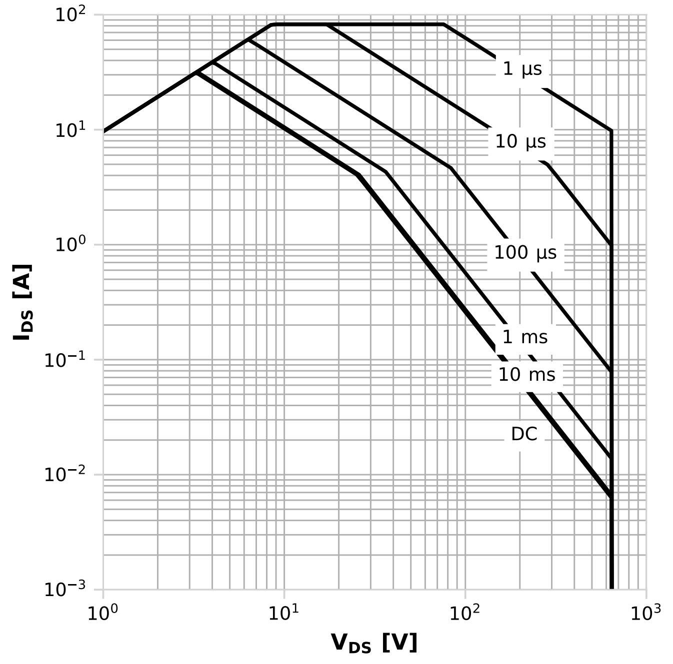
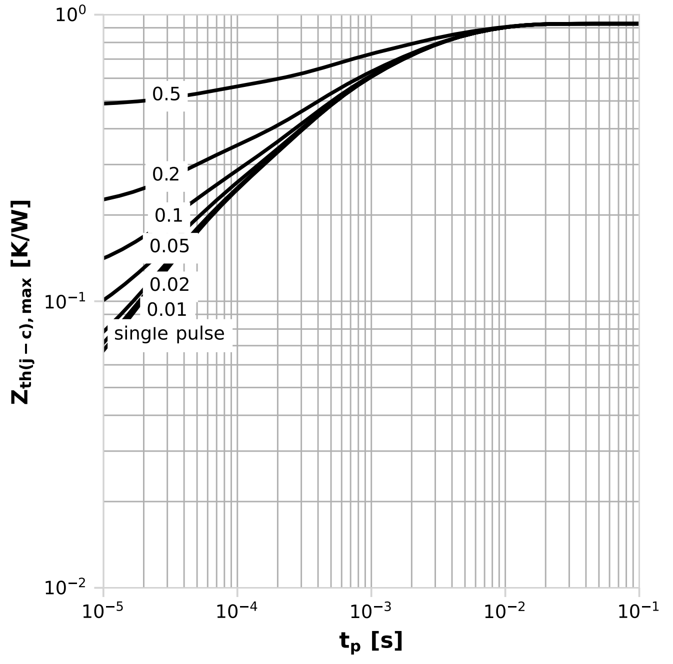
Diagram 3: Safe operating area	Diagram 4: Max. transient thermal impedance
	
$I_{DS}=f(V_{DS})$; T_C=80 °C; D=0; parameter: t_p	$Z_{th(j-c),max}=f(t_p)$; parameter: D=t_p/T

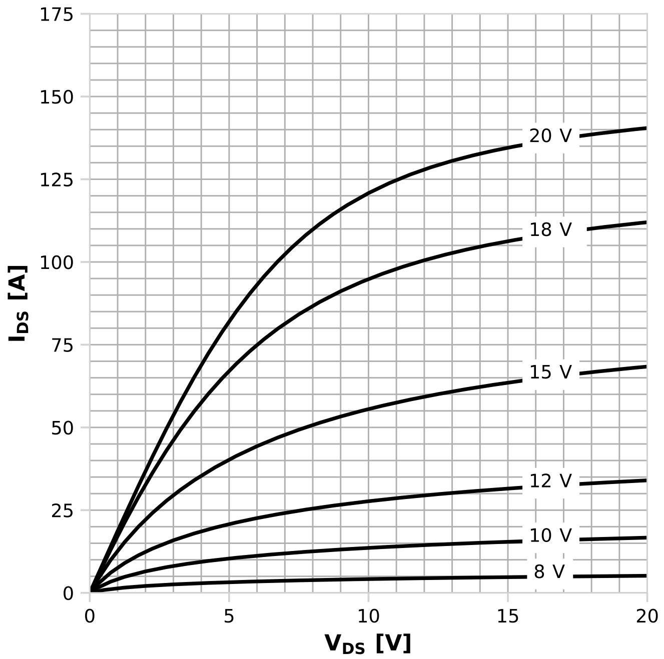
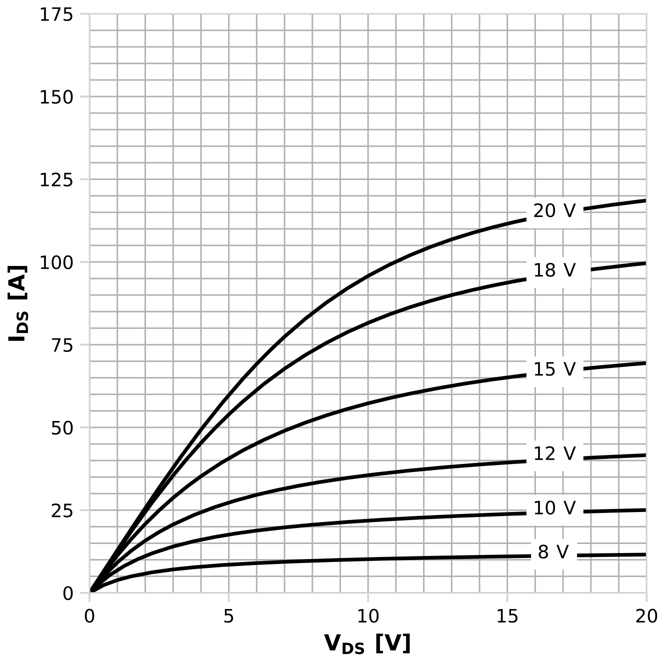
Diagram 5: Typ. output characteristics	Diagram 6: Typ. output characteristics
	
I_{DS}=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	I_{DS}=f(V_{DS}); T_j=175 °C; parameter: V_{GS}

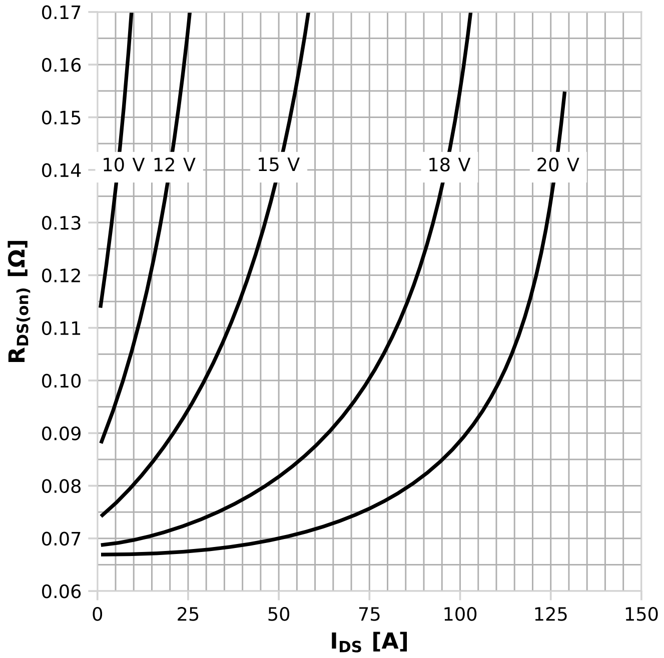
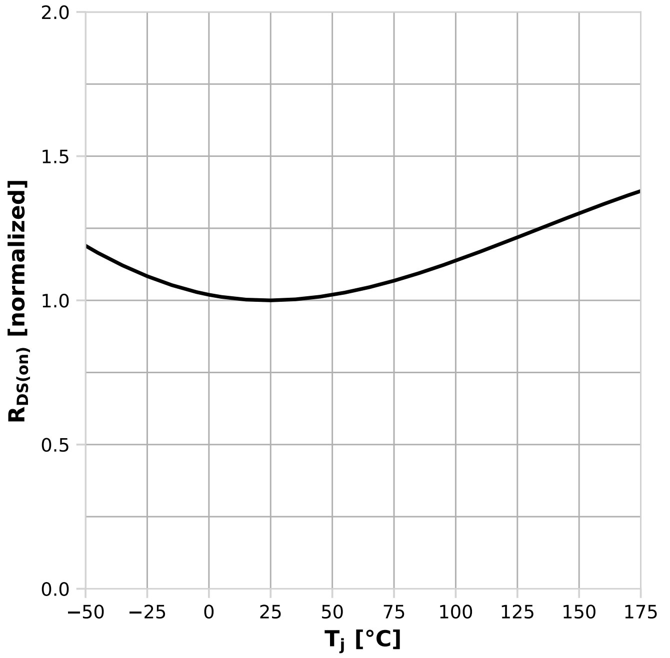
Diagram 7: Typ. drain-source on-state resistance	Diagram 8: Drain-source on-state resistance
	
$R_{DS(on)}$=f(I_{DS}); T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}$=f(T_j); I_D=16.7 A; V_{GS}=18 V

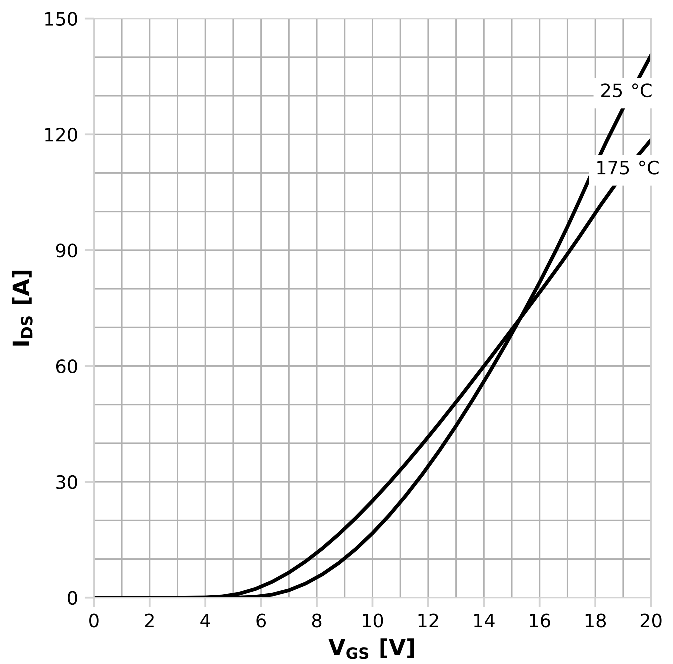
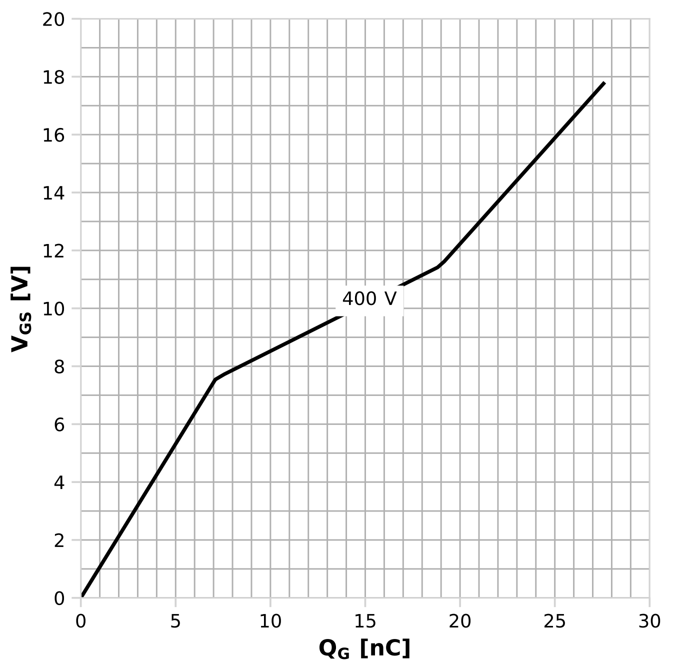
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_{DS}=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_G); I_D=16.7 A pulsed; parameter: V_{DD}

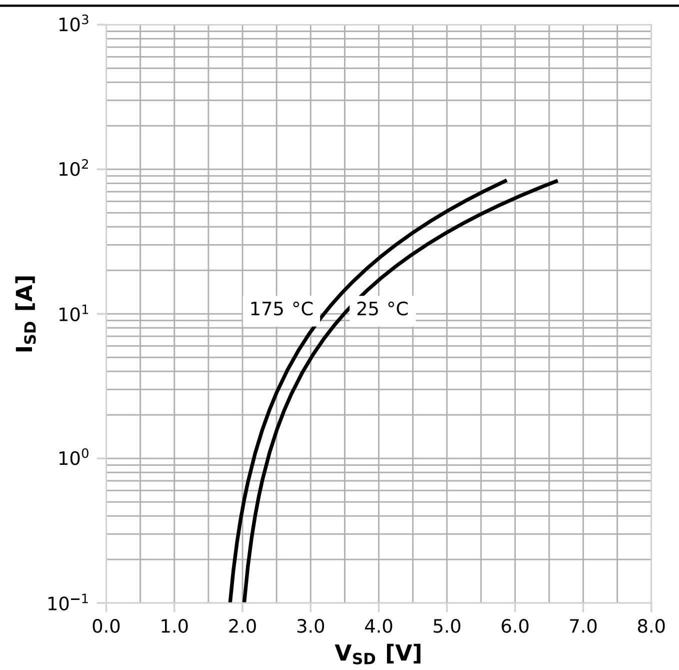
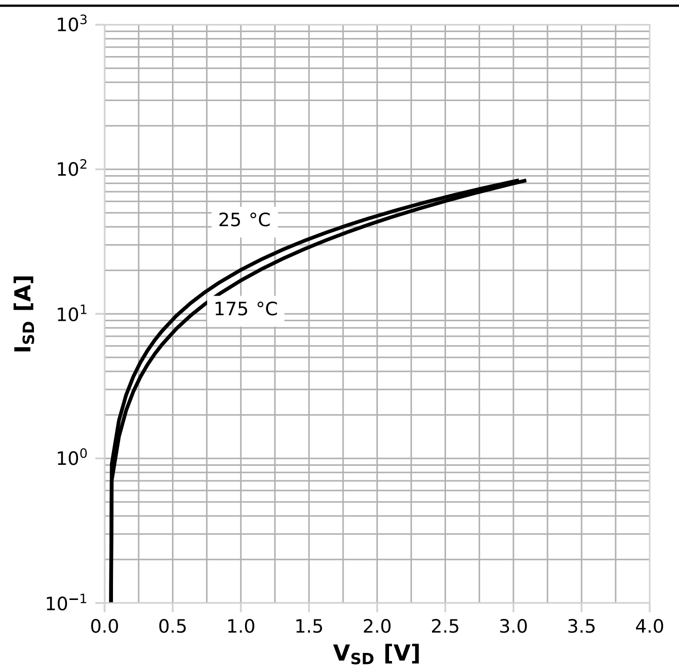
Diagram 11: Typ. reverse drain current characteristics	Diagram 12: Typ. reverse drain current characteristics
	
I_{SD}=f(V_{SD}); V_{GS}=0 V; parameter: T_j	I_{SD}=f(V_{SD}); V_{GS}=18 V; parameter: T_j

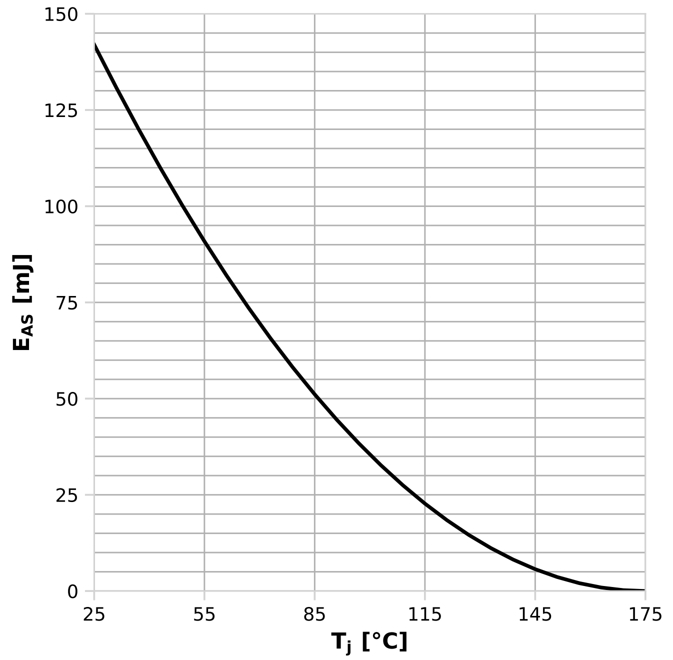
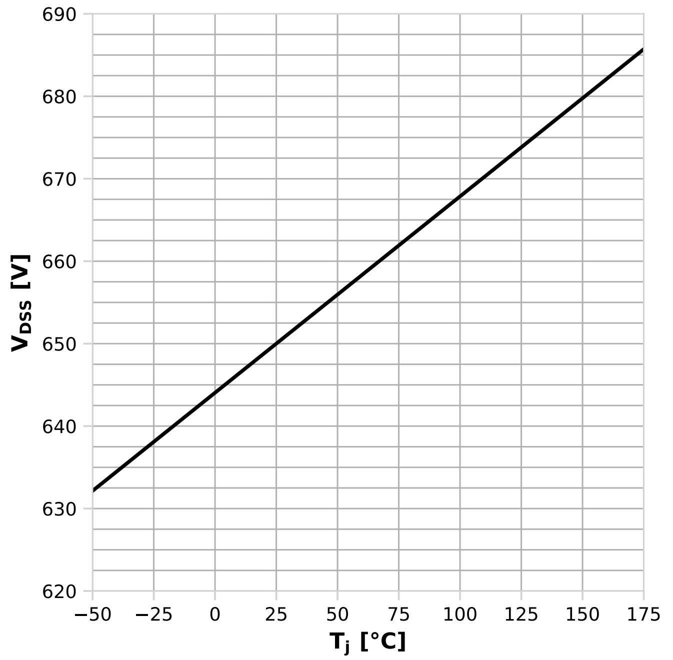
Diagram 13: Avalanche energy	Diagram 14: Drain-source breakdown voltage
	
$E_{AS}=f(T_j)$; $I_D=5.3$ A; $V_{DD}=50$ V	$V_{DSS}=f(T_j)$; $I_D=0.5$ mA

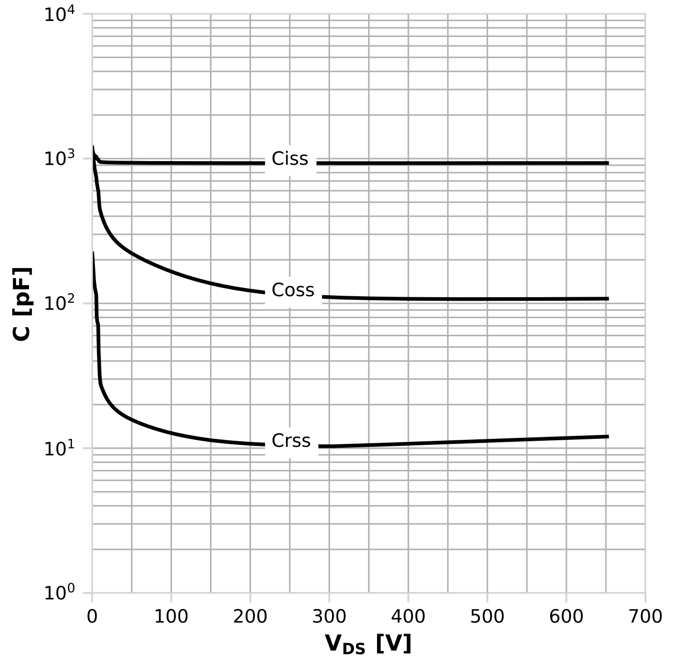
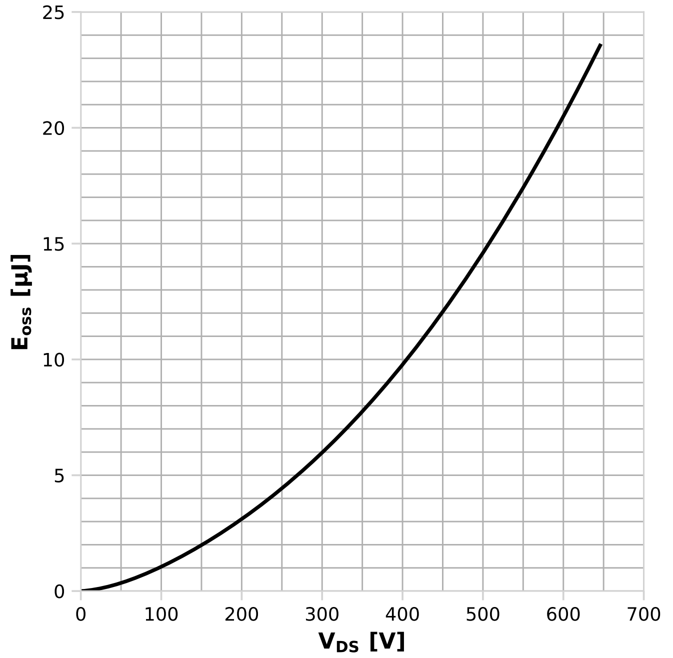
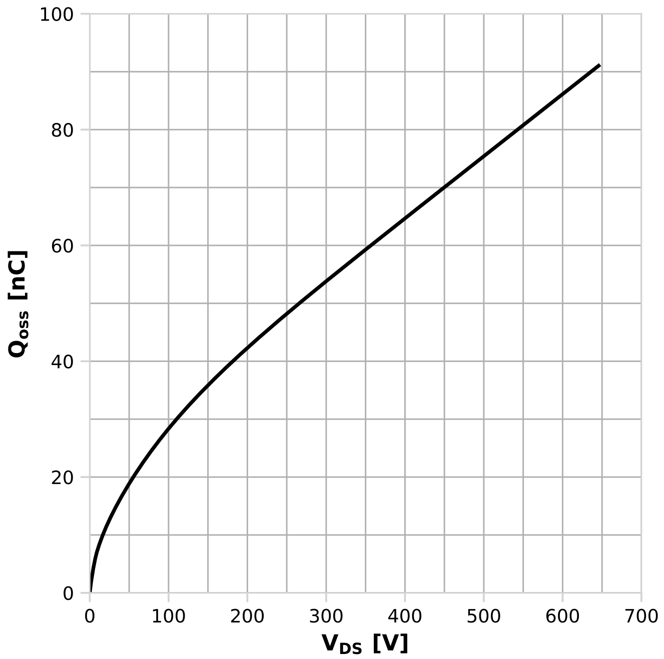
Diagram 15: Typ. capacitances	Diagram 16: Typ. Coss stored energy
	
$C=f(V_{DS})$; $V_{GS}=0$ V; f=250 kHz	$E_{oss}=f(V_{DS})$

Diagram 17: Typ. Qoss output charge



Q_{oss}=f(V_{DS})

6 Test Circuits

Table 9 Body diode characteristics (CoolSiC)

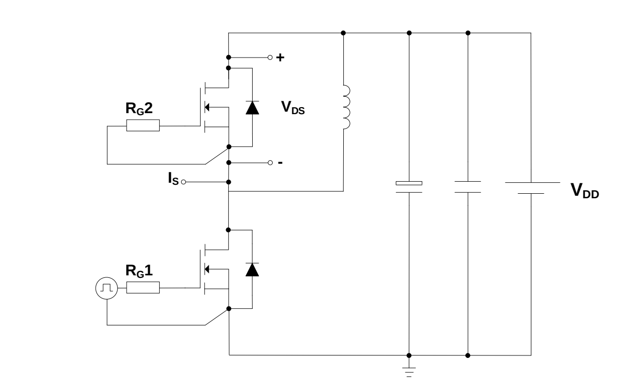
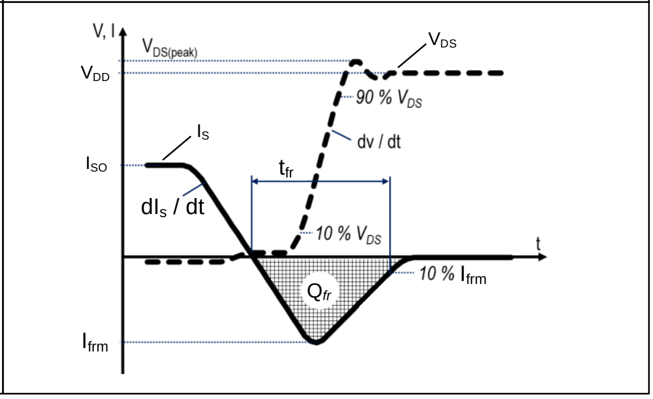
Test circuit for body diode characteristics	Body diode recovery waveform
	

Table 10 Switching times (CoolSiC)

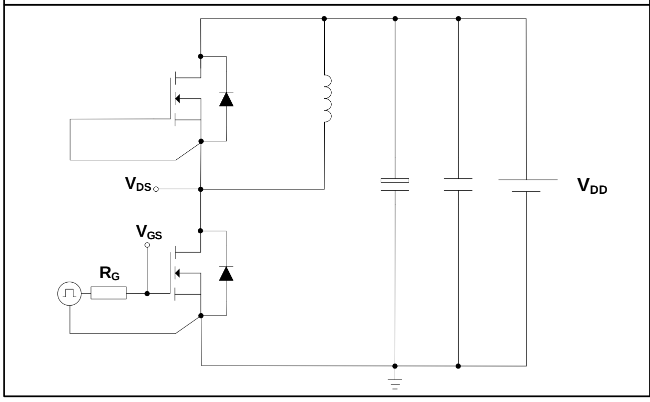
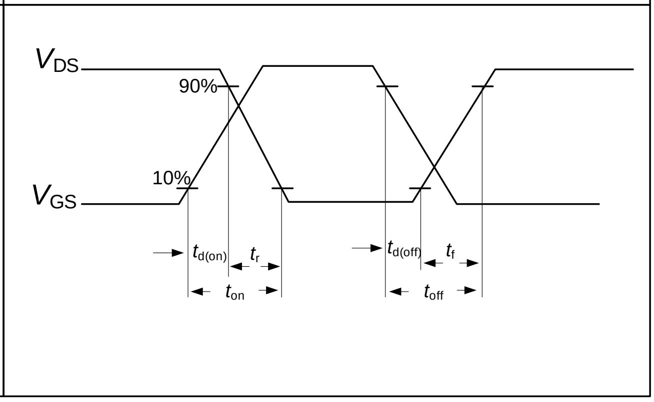
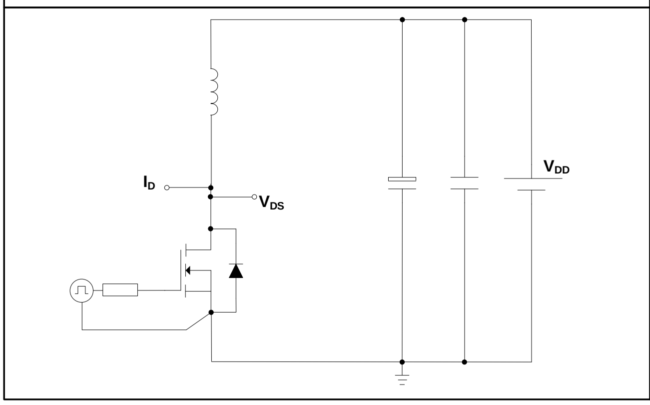
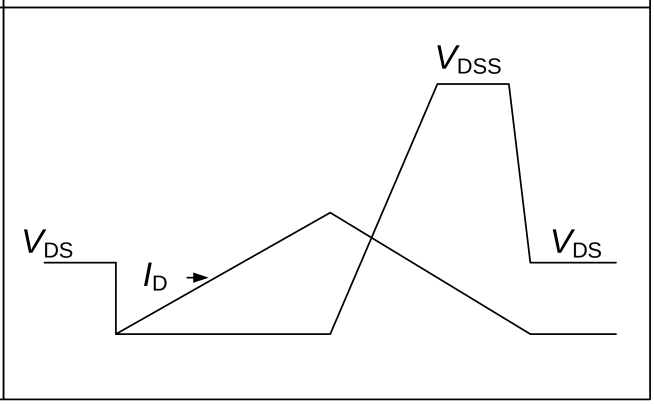
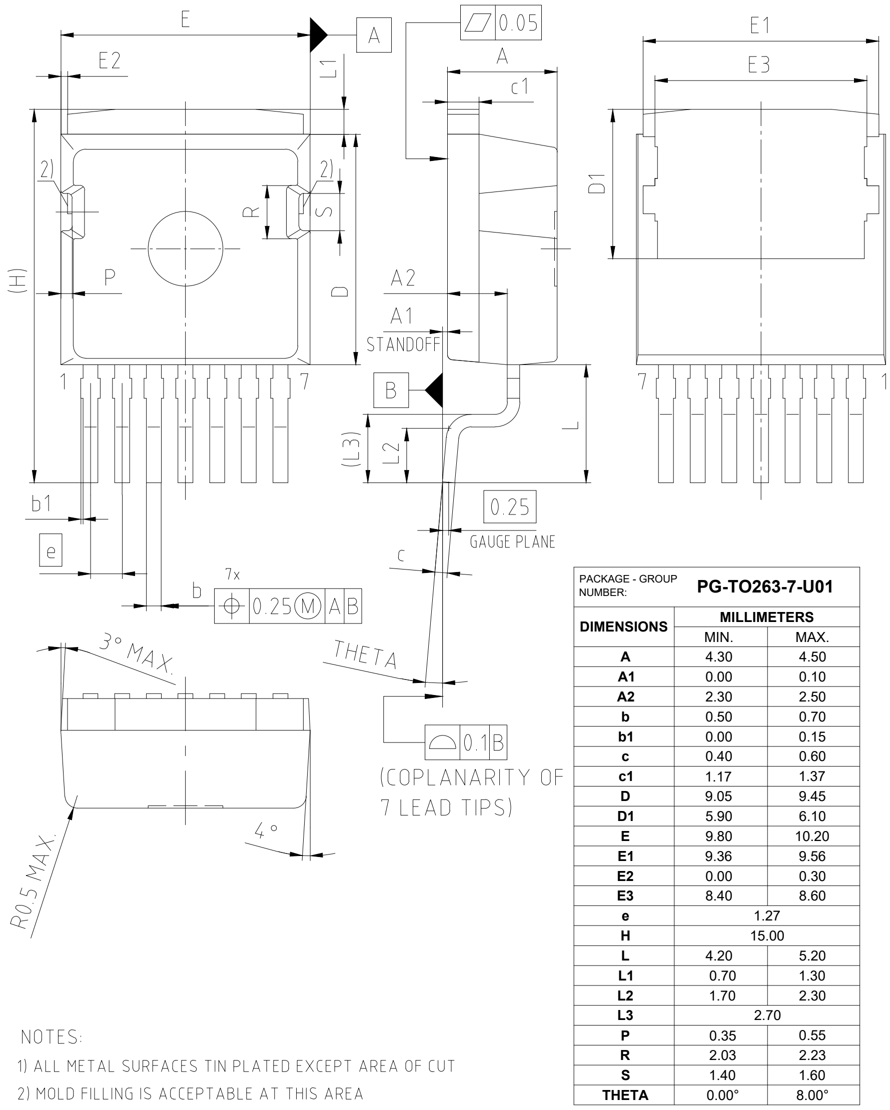
Switching times test circuit for inductive load	Switching times waveform
	

Table 11 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



PACKAGE - GROUP NUMBER:	PG-TO263-7-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.10
A2	2.30	2.50
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	5.90	6.10
E	9.80	10.20
E1	9.36	9.56
E2	0.00	0.30
E3	8.40	8.60
e	1.27	
H	15.00	
L	4.20	5.20
L1	0.70	1.30
L2	1.70	2.30
L3	2.70	
P	0.35	0.55
R	2.03	2.23
S	1.40	1.60
THETA	0.00°	8.00°

Figure 1 Outline PG-TO263-7, dimensions in mm

8 Appendix A

Table 12 Related Links

- IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Webpage
- IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Application Note
- IFX CoolSiC CoolSiC™ MOSFET 650 V G1 Simulation Model
- IFX Design tools

Revision History

IMBG65R057M1H

Revision 2024-08-26, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-12-10	Release of final version
2.1	2024-08-26	IDSS update, nomenclature update, datasheet layout update

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Published by
Infineon Technologies AG
81726 München, Germany

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