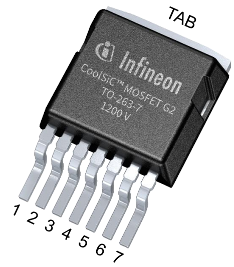
Final datasheet

CoolSiC™ 1200 V SiC MOSFET G2 : Silicon Carbide MOSFET

Features

- V_{DSS} = 1200 V at T_{vj} = 25°C
- I_{DDC} = 6.2 A at T_C = 100°C
- $R_{DS(on)}$ = 233.9 mΩ at V_{GS} = 18 V, T_{vj} = 25°C
- Very low switching losses
- Overload operation up to T_{vj} = 200°C
- Short circuit withstand time 2 µs
- Benchmark gate threshold voltage, $V_{GS(th)}$ = 4.2 V
- Robust against parasitic turn on, 0 V turn-off gate voltage can be applied
- Robust body diode for hard commutation
- .XT interconnection technology for best-in-class thermal performance
- Suitable Infineon gate drivers can be found under https://www.infineon.com/gdfinder



Halogen-free
Green
Lead-free
RoHS

Potential applications

- EV Charging
- Online UPS / Industrial UPS
- String inverter
- General purpose drives (GPD)

Product validation

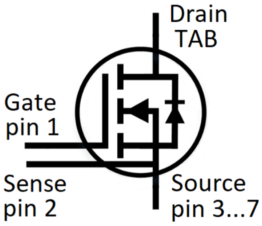
- Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Description

Pin definition:

- Pin 1 - Gate
- Pin 2 - Kelvin sense contact
- Pin 3…7 - Source
- Tab - Drain

Note: the source and sense pins are not exchangeable, their exchange might lead to malfunction (only for 4pin, TO263-7L)



Type	Package	Marking
IMBG120R234M2H	PG-TO263-7-U01	12M2H234

Table of contents

1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}	Reflow soldering (MSL1 according to JEDEC J-STD-020)			260	°C
Thermal resistance, junction-ambient	$R_{th(j-a)}$				62	K/W
MOSFET/body diode thermal resistance, junction-case	$R_{th(j-c)}$			1.44	1.87	K/W

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	$T_{vj} \geq 25$ °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{DDC}	$V_{GS} = 18$ V	$T_c = 25$ °C	8.1	A
			$T_c = 100$ °C	6.2	
Peak drain current, t_p limited by $T_{vj(max)}$ 1)	I_{DM}	$V_{GS} = 18$ V		31	A
Gate-source voltage, max. transient voltage	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10...25	V
Gate-source voltage, max. static voltage 2)	V_{GS}			-7...23	V
Avalanche energy, single pulse	E_{AS}	$I_D = 3$ A, $V_{DD} = 50$ V, $L = 8.2$ mH, $T_{vj(start)} = 25$ °C		37	mJ
Avalanche energy, repetitive	E_{AR}	$I_D = 3$ A, $V_{DD} = 50$ V, $L = 42.2$ µH, $T_{vj(start)} = 25$ °C		0.19	mJ
Short-circuit withstand time	t_{SC}	$V_{DD} \leq 800$ V, $V_{DS,peak} < 1200$ V, $V_{GS(on)} = 15$ V, $T_{vj(start)} = 25$ °C		2	µs
Power dissipation, limited by $T_{vj(max)}$	P_{tot}		$T_c = 25$ °C	80	W
			$T_c = 100$ °C	40	

1) verified by design.
2) The maximum gate-source voltage in the application design should be in accordance to IPC-9592B.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		15...18	V
Recommended turn-off gate voltage	$V_{GS(off)}$		-5...0	V

Table 4 Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	$I_D = 3$ A	$T_{vj} = 25$ °C, $V_{GS(on)} = 18$ V		233.9		mΩ
			$T_{vj} = 150$ °C, $V_{GS(on)} = 18$ V		477	622	
			$T_{vj} = 175$ °C, $V_{GS(on)} = 18$ V		554		
			$T_{vj} = 25$ °C, $V_{GS(on)} = 15$ V		292		
Gate-source threshold voltage	$V_{GS(th)}$	$I_D = 0.9$ mA, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at $V_{GS} = 20$ V)	$T_{vj} = 25$ °C	3.5	4.2	5.1	V
			$T_{vj} = 175$ °C		3.2		
Zero gate-voltage drain current	I_{DSS}	$V_{DS} = 1200$ V, $V_{GS} = 0$ V	$T_{vj} = 25$ °C			30	µA
			$T_{vj} = 175$ °C		0.4		
Gate leakage current	I_{GSS}	$V_{DS} = 0$ V	$V_{GS} = 23$ V			120	nA
			$V_{GS} = -10$ V			-120	
Forward transconductance	g_{fs}	$I_D = 3$ A, $V_{DS} = 20$ V			2		S
Internal gate resistance	$R_{G,int}$	$f = 1$ MHz, $V_{AC} = 25$ mV			25		Ω
Input capacitance	C_{iss}	$V_{DS} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			290		pF
Output capacitance	C_{oss}	$V_{DS} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			9.6		pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			0.8		pF
C_{oss} stored energy	E_{oss}	Calculated based on $C_{oss} = f(V_{DD})$			3.9		µJ
Output charge	Q_{oss}	Calculated based on $C_{oss} = f(V_{DD})$			14.7		nC
Effective output capacitance, energy related	$C_{o(er)}$	$V_{DS} = 0...800$ V, $V_{GS} = 0$ V, Calculated based on E_{oss}			12.2		pF
Effective output capacitance, time related	$C_{o(tr)}$	I_D = constant, $V_{DS} = 0...800$ V, $V_{GS} = 0$ V, Calculated based on Q_{oss}			18.4		pF
Total gate charge	Q_G	$V_{DD} = 800$ V, $I_D = 3$ A, $V_{GS} = 0/18$ V, turn-on pulse			7.9		nC

(table continues...)

Table 4 (continued) Characteristic values

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Plateau gate charge	$Q_{GS(pl)}$	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, turn-on pulse			1.9		nC
Gate-drain charge	Q_{GD}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, turn-on pulse			1.8		nC
Turn-on delay time	$t_{d(on)}$	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		1		ns
			T_{vj} = 175 °C		0.7		
Rise time	t_r	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		12.5		ns
			T_{vj} = 175 °C		12.4		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		1.4		ns
			T_{vj} = 175 °C		2.5		
Fall time	t_f	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		0.6		ns
			T_{vj} = 175 °C		0.7		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		16		µJ
			T_{vj} = 175 °C		28.5		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		4.1		µJ
			T_{vj} = 175 °C		4.1		
Total switching energy[1)]	E_{tot}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = 0/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		30.1		µJ
			T_{vj} = 175 °C		62.1		

(table continues...)

Table 4 **(continued) Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Turn-on energy at -5 V	E_{on}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		18		µJ
			T_{vj} = 175 °C		41		
Turn-off energy at -5 V	E_{off}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		4		µJ
			T_{vj} = 175 °C		4		
Total switching energy at -5 V[1)]	E_{tot}	V_{DD} = 800 V, I_D = 3 A, V_{GS} = -5/18 V, $R_{G,ext}$ = 2.3 Ω, L_σ = 15 nH, diode: body diode at V_{GS} = -5 V	T_{vj} = 25 °C		34		µJ
			T_{vj} = 175 °C		86		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[2)]				200	°C

1) including E_{fr}
2) up to 5000 cycles. Maximum ΔT limited to 100 K.

***Note**:* *The chip technology was characterized up to 200 kV/µs. The measured dV/dt was limited by measurement test setup and package.*

Characteristics at T_{vj} = 25°C, unless otherwise specified.

3 Body diode (MOSFET)

Table 5 **Maximum rated values**

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage	V_{DSS}	T_{vj} ≥ 25 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	3	A
			T_c = 100 °C	3.2	
Peak reverse drain current, t_p limited by $T_{vj(max)}$	I_{SM}	V_{GS} = 0 V		12	A

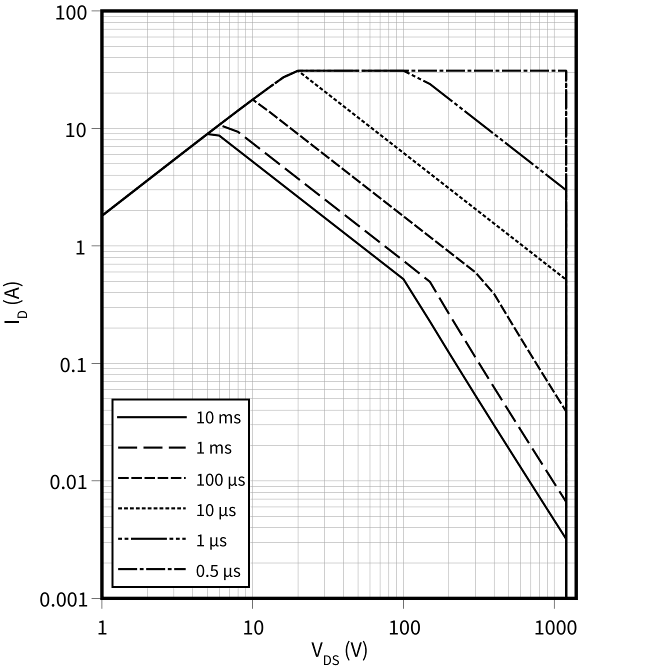
Table 6 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 3 A, V_{GS} = 0 V	T_{vj} = 25 °C		4.2	5.5	V
			T_{vj} = 100 °C		4.11		
			T_{vj} = 175 °C		4.05		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 3 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		0.48		nC
			T_{vj} = 175 °C		0.44		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 3 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		23		A
			T_{vj} = 175 °C		21		
MOSFET forward recovery energy	E_{fr}	V_{DD} = 800 V, I_{SD} = 3 A, V_{GS} = 0 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		10		µJ
			T_{vj} = 175 °C		29.2		
MOSFET forward recovery energy at -5 V	E_{fr}	V_{DD} = 800 V, I_{SD} = 3 A, V_{GS} = -5 V, $R_{G,ext}$ = 2.3 Ω, Q_{fr} includes also Q_C	T_{vj} = 25 °C		12		µJ
			T_{vj} = 175 °C		41		
Virtual junction temperature	T_{vj}			-55		175	°C
Virtual junction temperature	$T_{vj(over)}$	overload, cumulative max. 100 h[1]				200	°C

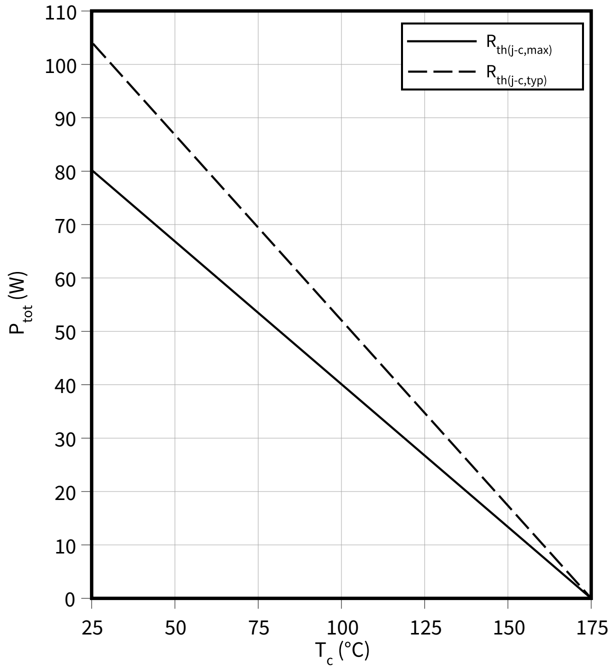
1) up to 5000 cycles. Maximum ΔT limited to 100 K.

4 Characteristics diagrams

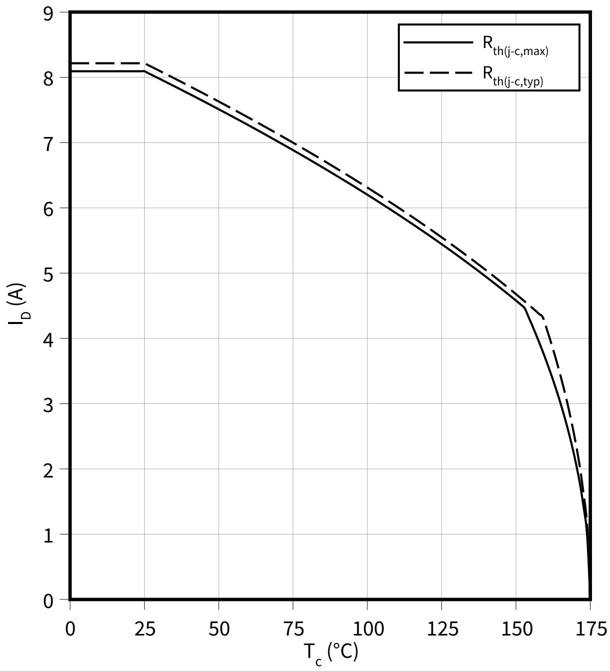
Safe operating area (SOA)
$I_D = f(V_{DS})$
$T_{vj} \leq 175$ °C, $T_c = 25$ °C



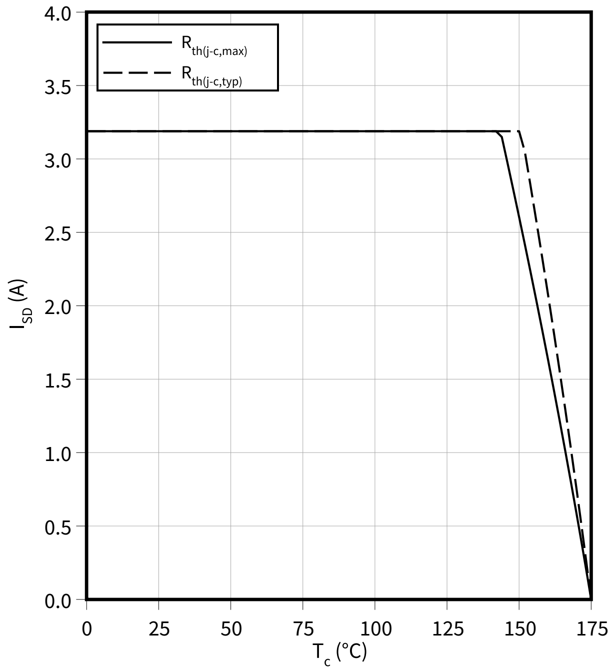
Power dissipation as a function of case temperature
$P_{tot} = f(T_c)$



Maximum DC drain to source current as a function of case temperature limited by bond wire
$I_D = f(T_c)$



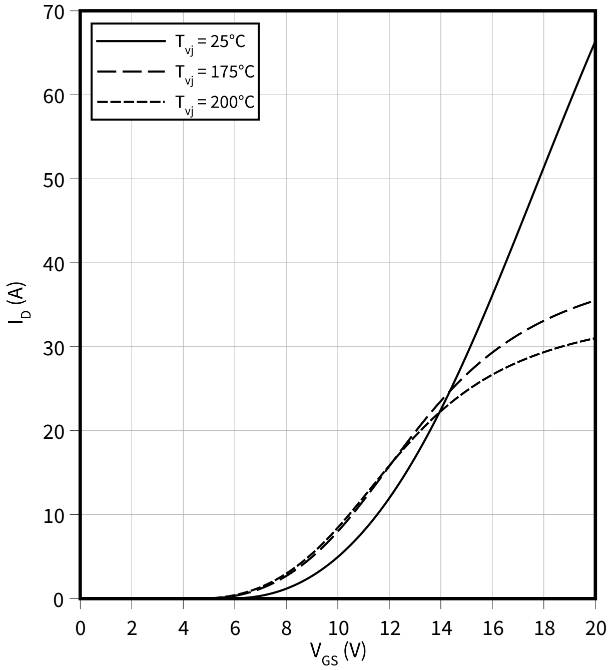
Maximum source to drain current as a function of case temperature limited by bond wire
$I_{SD} = f(T_c)$
$V_{GS} = 0$ V



Typical transfer characteristic

$I_D = f(V_{GS})$

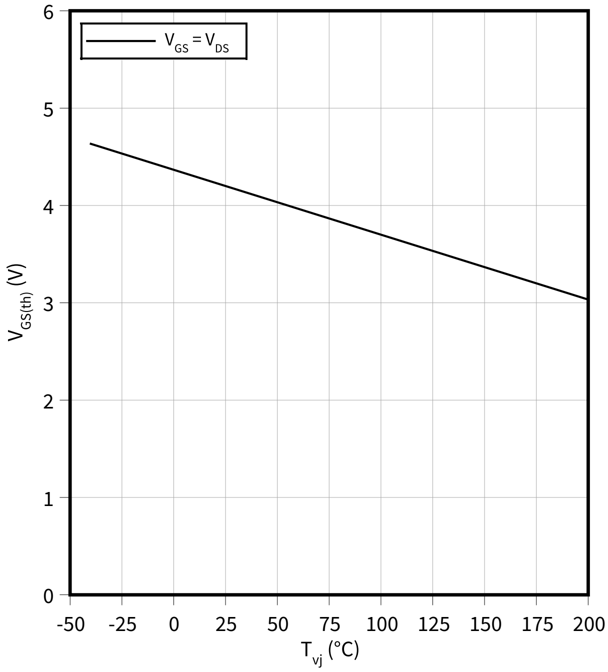
$V_{DS} = 20$ V, $t_p = 20$ µs



Typical gate-source threshold voltage as a function of junction temperature

$V_{GS(th)} = f(T_{vj})$

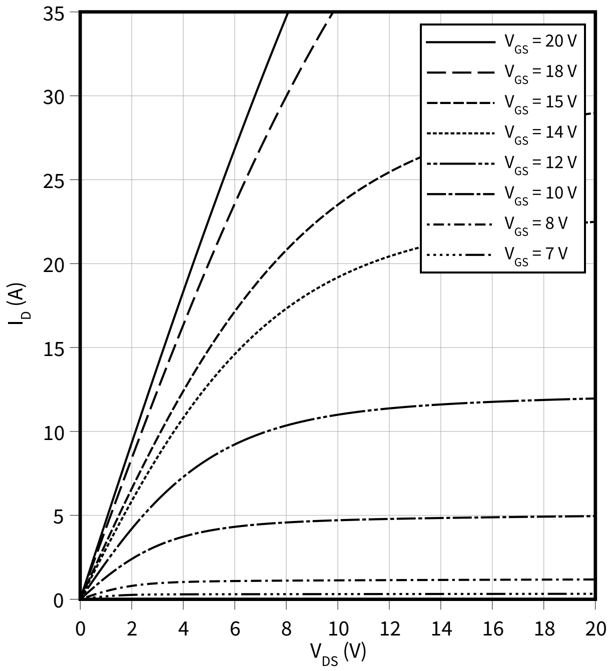
$I_D = 0.9$ mA



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

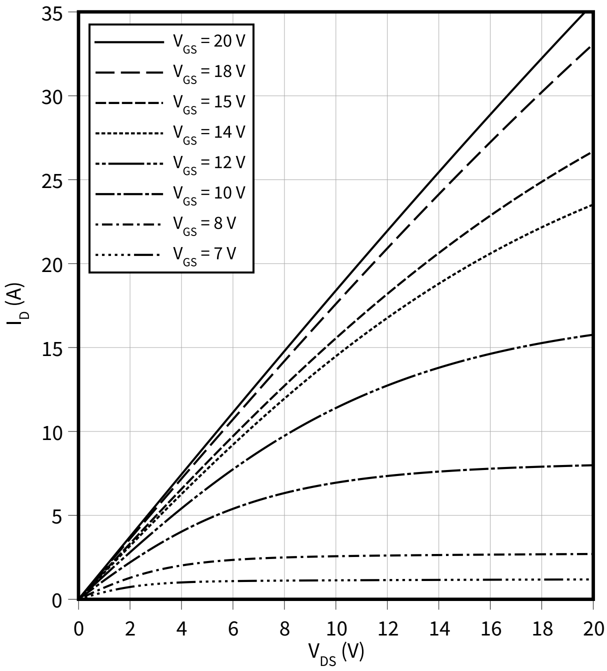
$T_{vj} = 25$ °C, $t_p = 20$ µs



Typical output characteristic, V_{GS} as a parameter

$I_D = f(V_{DS})$

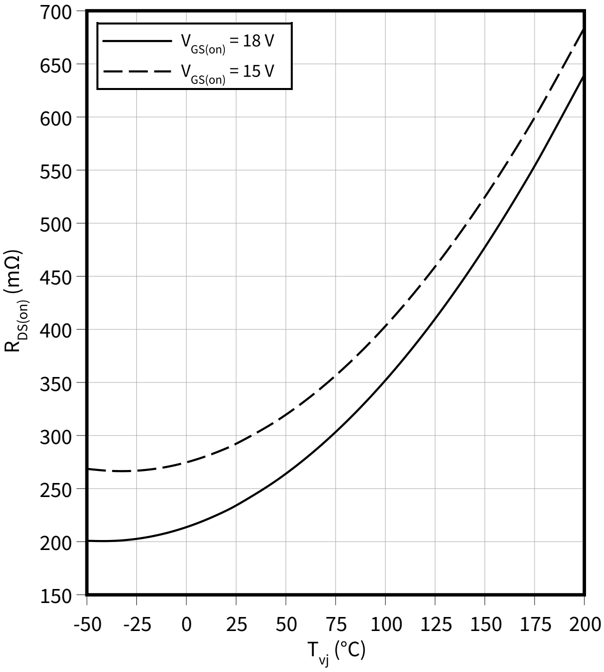
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

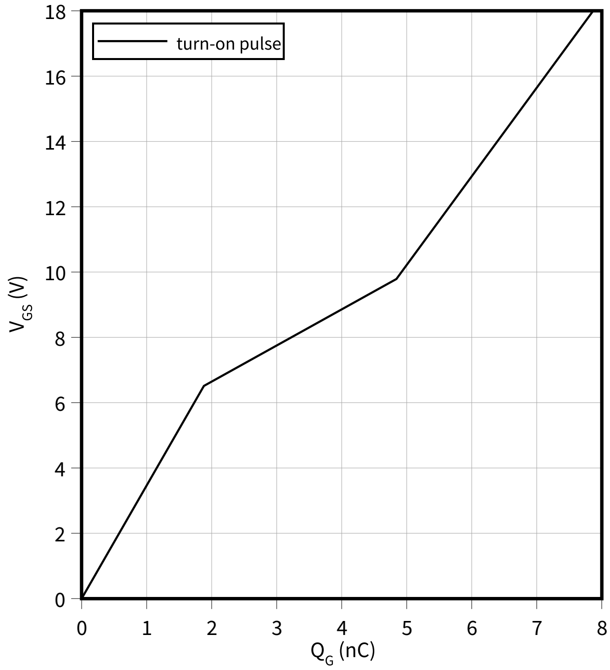
$I_D = 3$ A



Typical gate charge

$V_{GS} = f(Q_G)$

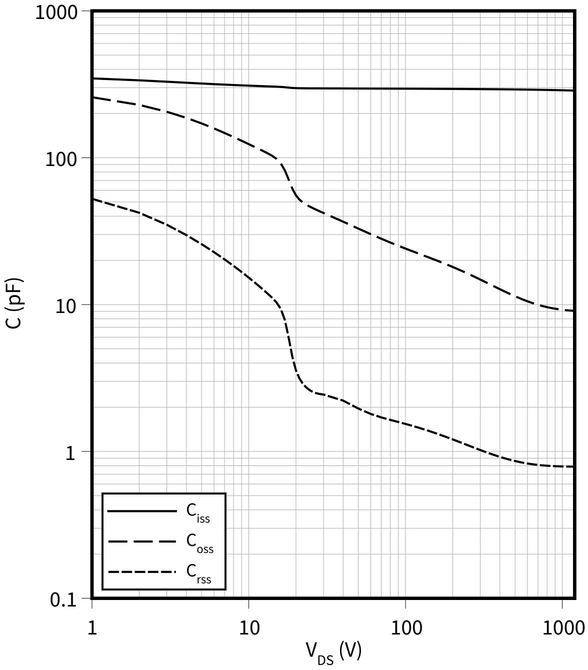
$V_{DS} = 800$ V, $I_D = 3$ A



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

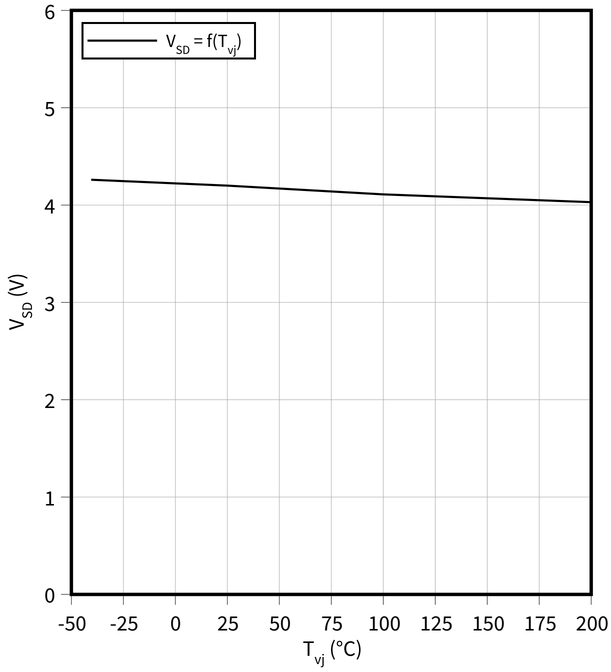
$f = 100$ kHz, $V_{GS} = 0$ V



Typical reverse drain voltage as a function of junction temperature

$V_{SD} = f(T_{vj})$

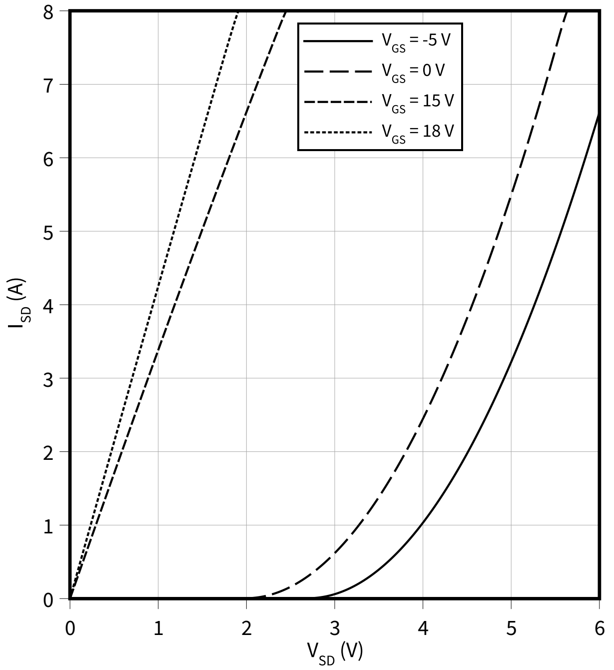
$I_{SD} = 3$ A, $V_{GS} = 0$ V



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

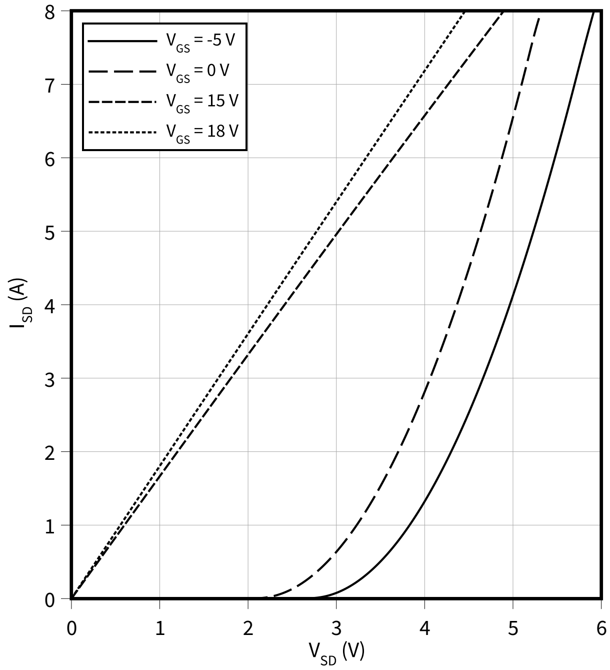
$T_{vj} = 25\ °C$, $t_p = 20\ µs$



Typical reverse drain current as a function of reverse drain voltage, V_{GS} as a parameter

$I_{SD} = f(V_{SD})$

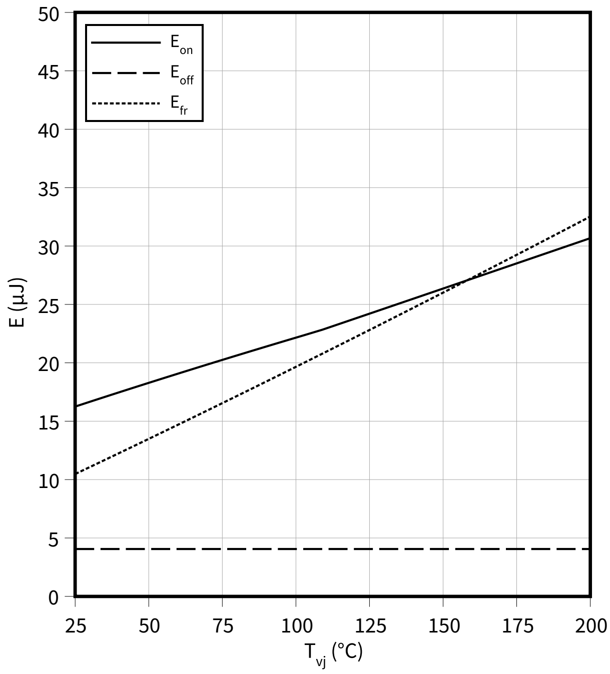
$T_{vj} = 175\ °C$, $t_p = 20\ µs$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(T_{vj})$

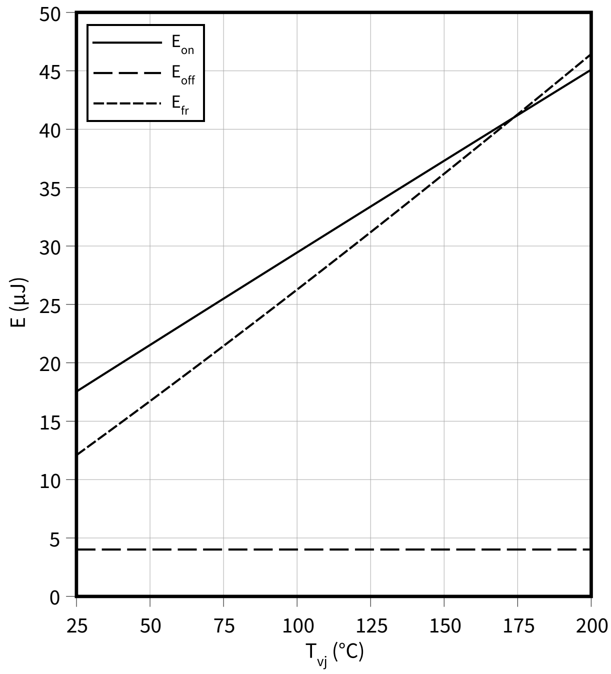
$V_{GS} = 0/18\ V$, $I_D = 3\ A$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(T_{vj})$

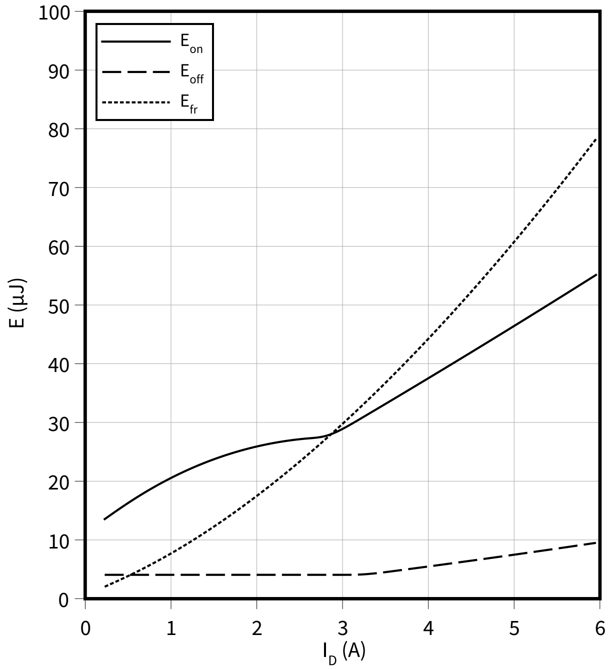
$V_{GS} = -5/18\ V$, $I_D = 3\ A$, $R_{G,ext} = 2.3\ Ω$, $V_{DD} = 800\ V$



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(I_D)$

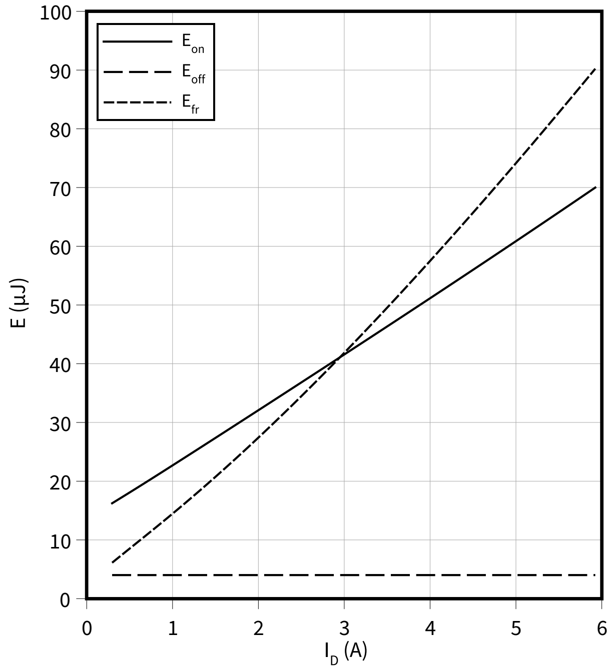
V_{GS} = 0/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(I_D)$

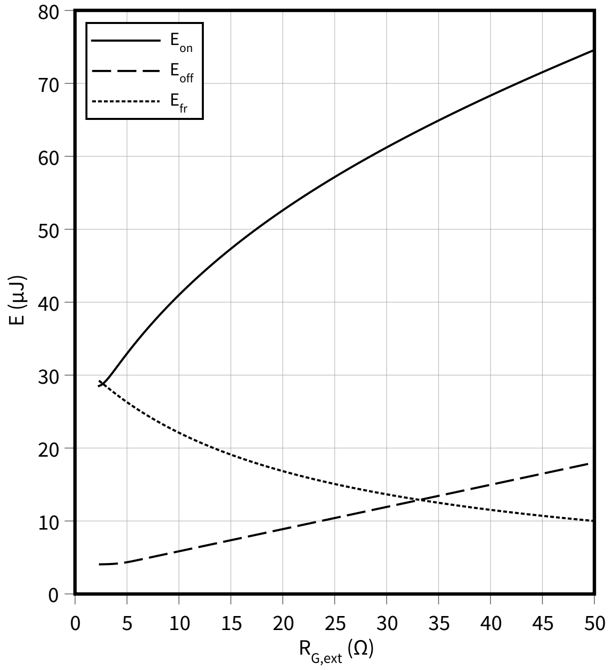
V_{GS} = -5/18 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

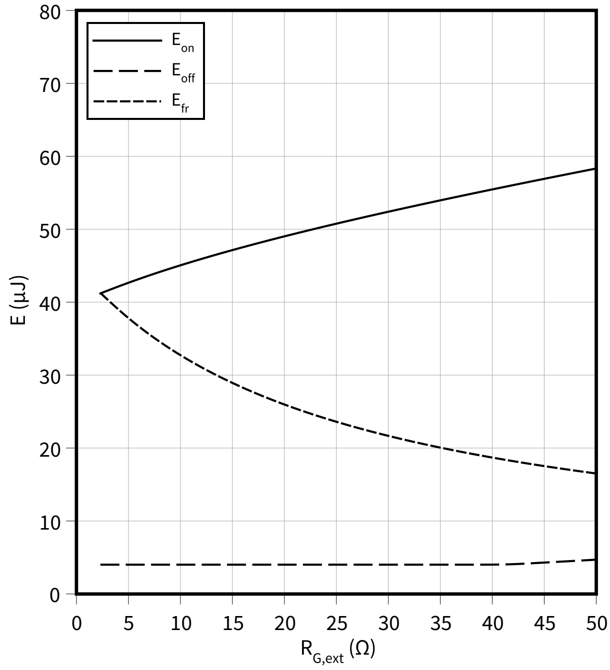
V_{GS} = 0/18 V, I_D = 3 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(R_{G,ext})$

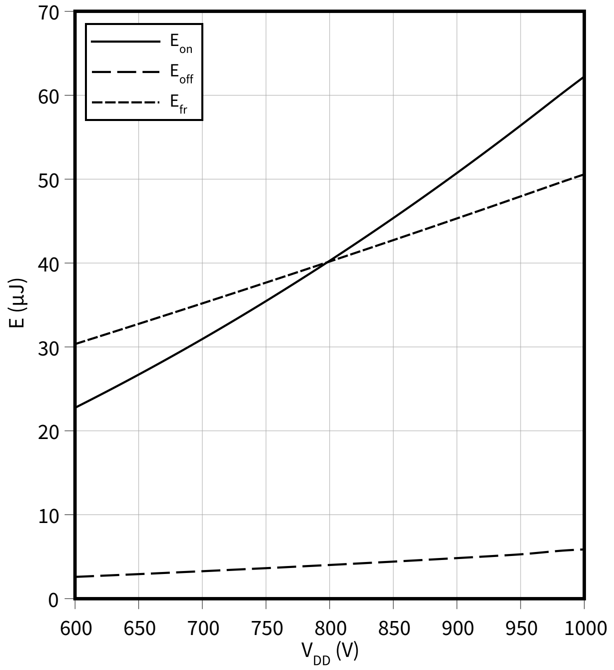
V_{GS} = -5/18 V, I_D = 3 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(V_{DD})$

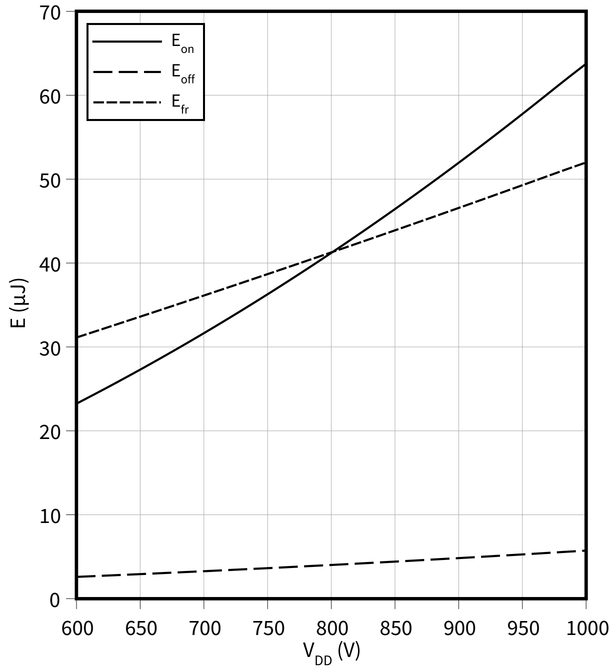
V_{GS} = 0/18 V, I_D = 3 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching energy as a function of DC link voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(V_{DD})$

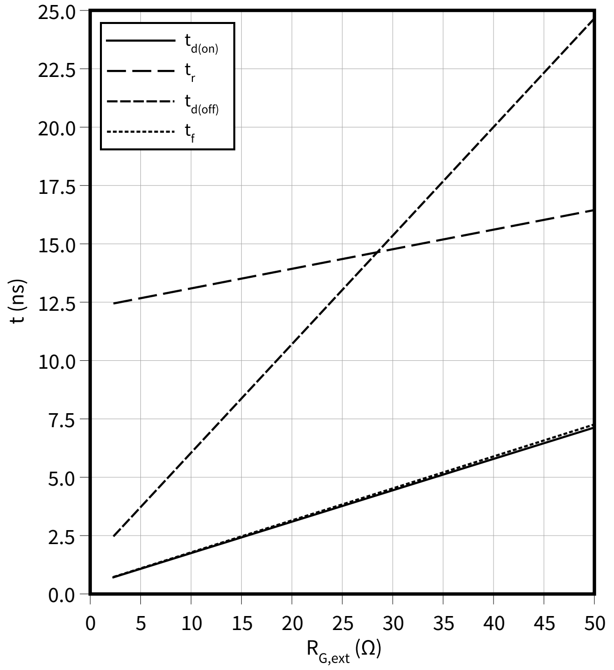
V_{GS} = -5/18 V, I_D = 3 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω



Typical switching times as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$t = f(R_{G,ext})$

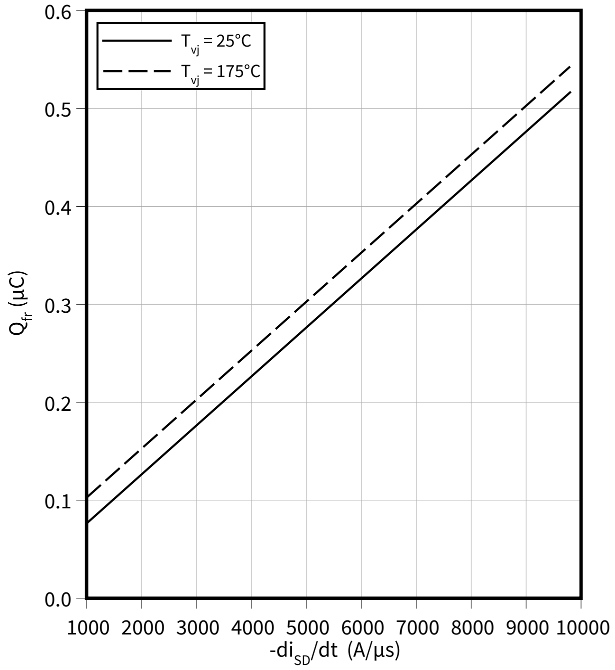
V_{GS} = 0/18 V, I_D = 3 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical reverse recovery charge as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$Q_{fr} = f(-di_{SD}/dt)$

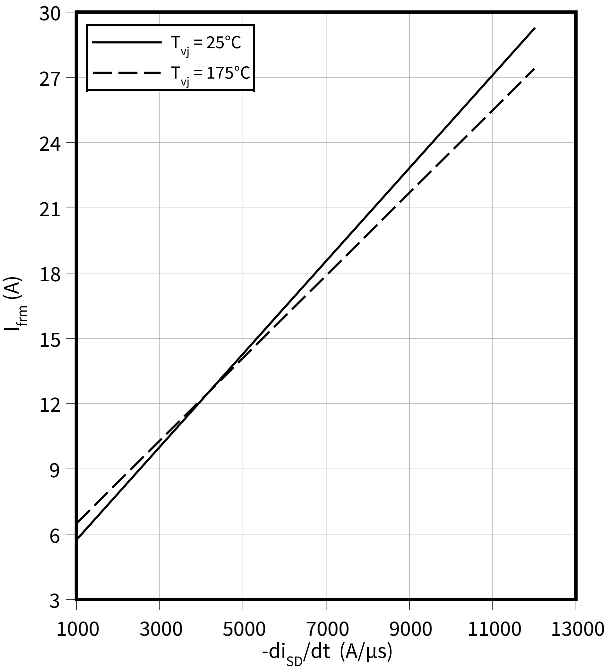
V_{GS} = 0/18 V, I_{SD} = 3 A, V_{DD} = 800 V



Typical reverse recovery current as a function of reverse drain current slope, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$I_{frm} = f(-di_{SD}/dt)$

V_{GS} = 0/18 V, I_{SD} = 3 A, V_{DD} = 800 V

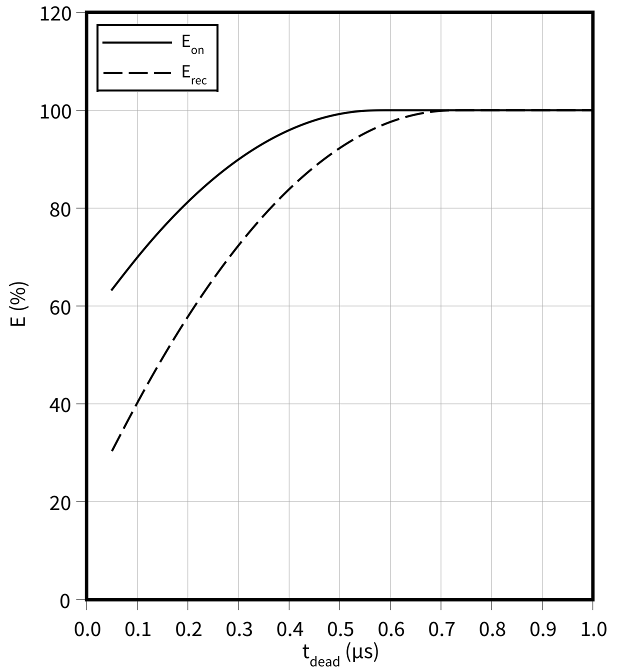


Typical switching energy as a function of dead time / blanking time, test circuit in Fig. F, 2nd device own body diode: V_{GS} = -5 V

$E = f(t_{dead})$

V_{GS} = 0/18 V, I_D = 3 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2.3 Ω

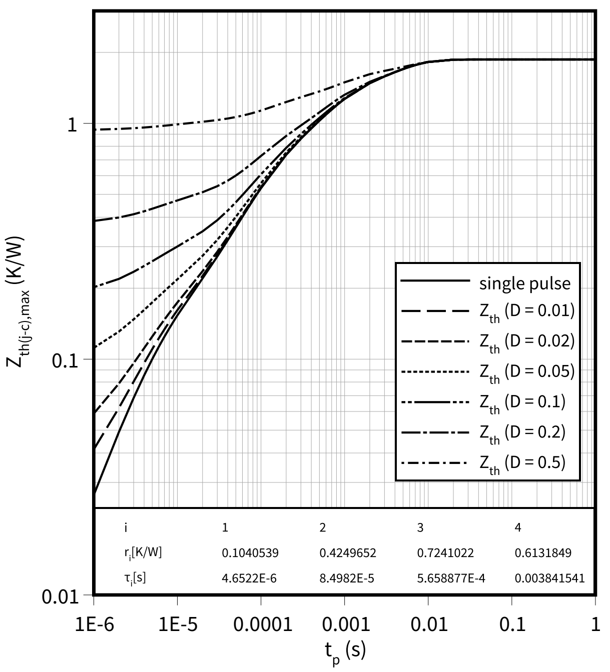
V_{DD} = 800 V



Max. transient thermal impedance (MOSFET/diode)

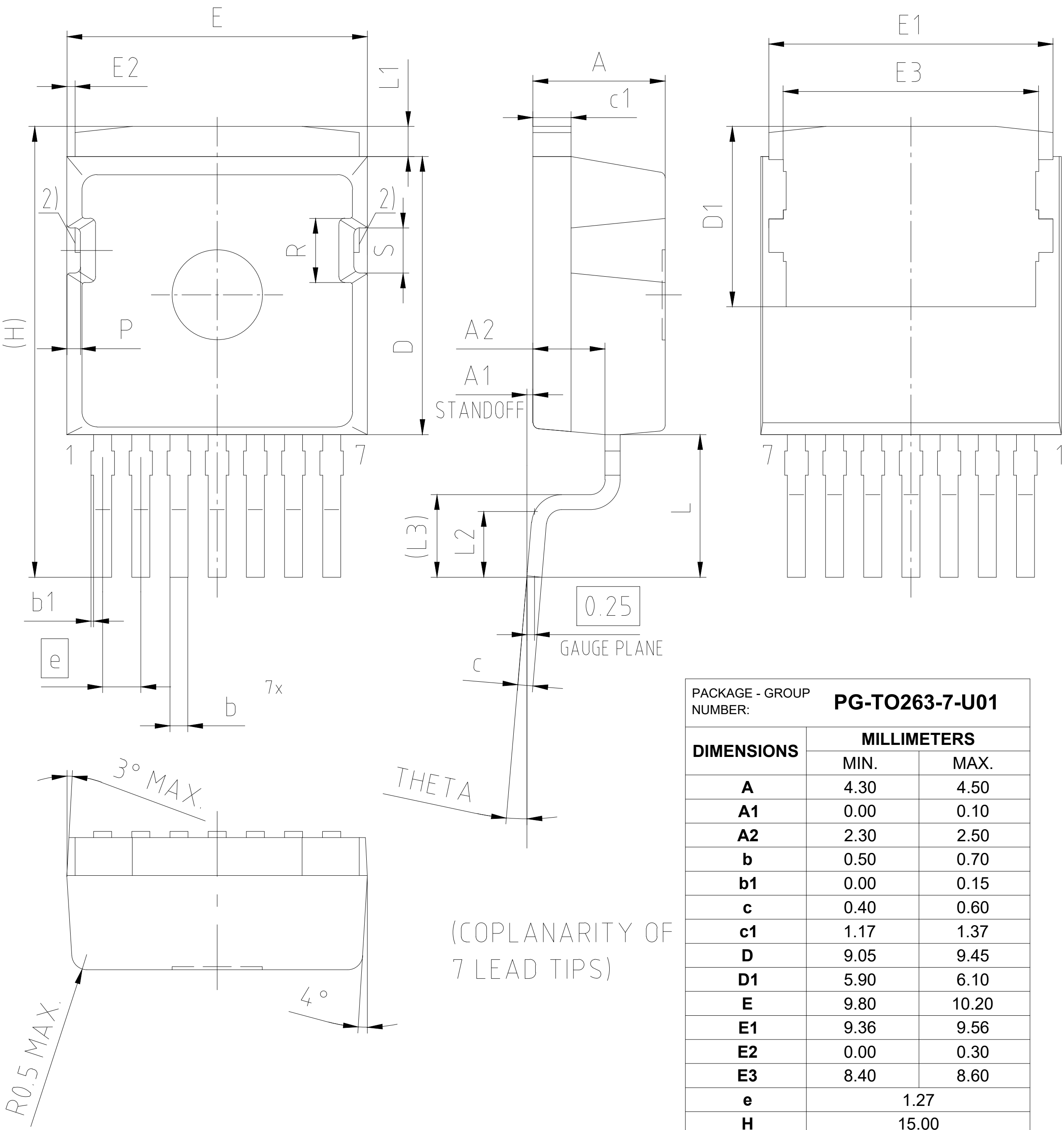
$Z_{th(j-c),max} = f(t_p)$

$D = t_p/T$



i	1	2	3	4
r_i[K/W]	0.1040539	0.4249652	0.7241022	0.6131849
τ_i[s]	4.6522E-6	8.4982E-5	5.658877E-4	0.003841541

5 Package outlines



PACKAGE - GROUP NUMBER:	PG-TO263-7-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.10
A2	2.30	2.50
b	0.50	0.70
b1	0.00	0.15
c	0.40	0.60
c1	1.17	1.37
D	9.05	9.45
D1	5.90	6.10
E	9.80	10.20
E1	9.36	9.56
E2	0.00	0.30
E3	8.40	8.60
e	1.27	
H	15.00	
L	4.20	5.20
L1	0.70	1.30
L2	1.70	2.30
L3	2.70	
P	0.35	0.55
R	2.03	2.23
S	1.40	1.60
THETA	0.00°	8.00°

NOTES:
1) ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT
2) MOLD FILLING IS ACCEPTABLE AT THIS AREA

Figure 1

6 Testing conditions

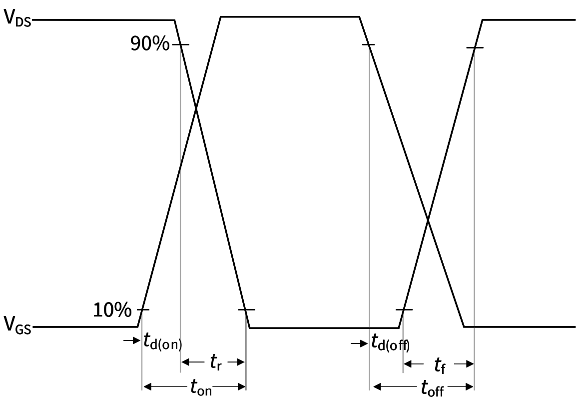


Figure A. **Definition of switching times**

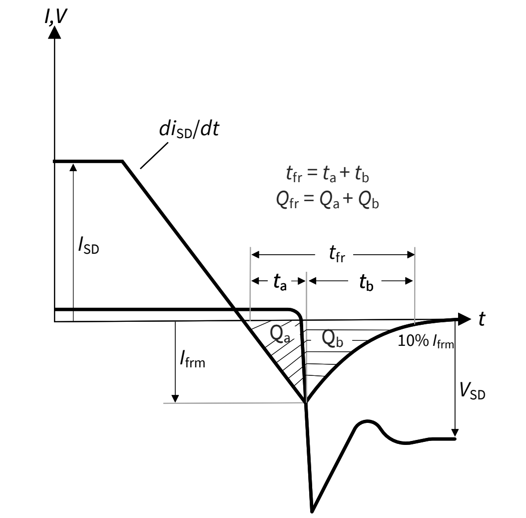


Figure B. **Definition of body diode switching characteristics**

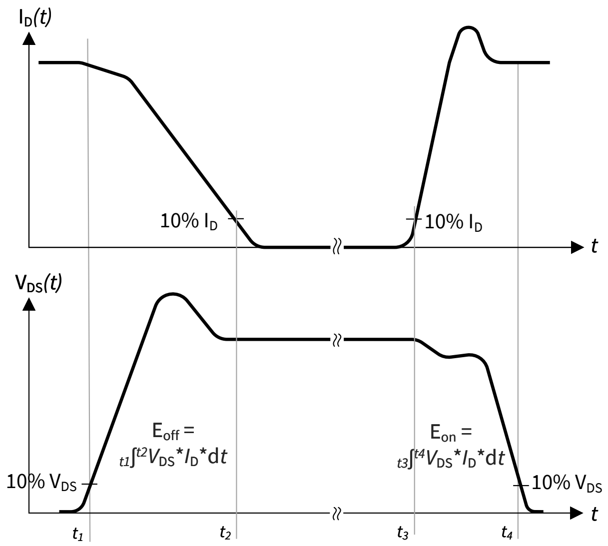


Figure C. **Definition of switching losses**

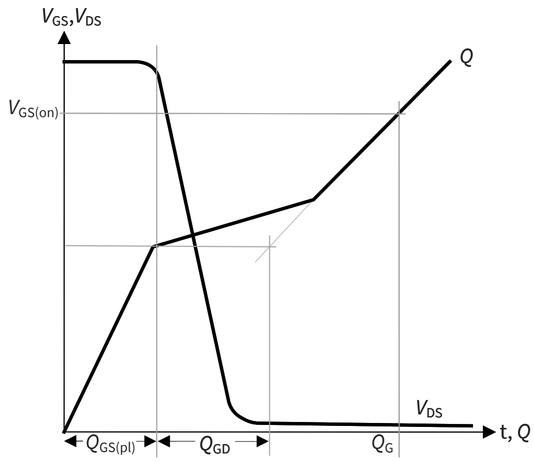


Figure D. **Definition of QGD**

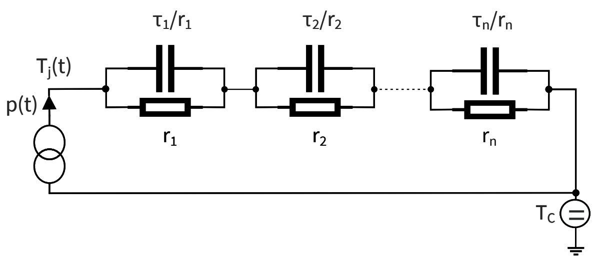


Figure E. **Thermal equivalent circuit**

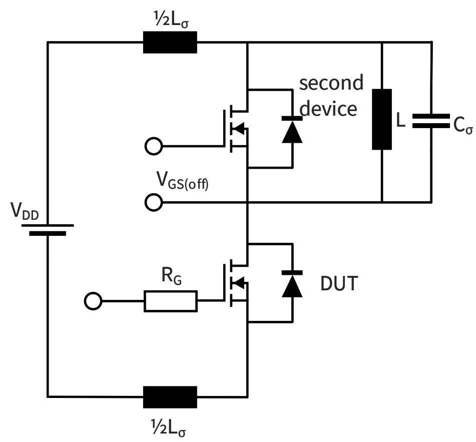


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2023-08-09	Preliminary datasheet
1.00	2023-10-05	Final datasheet
1.10	2024-01-12	Negative gate voltage values updated Additional capacitance & charge values added $E = f(t_{dead})$ graph y-axis correction to percentage values Editorial changes
1.20	2024-07-02	Updated „Potential applications“ Corrected package name Corrected static and dynamic gate-source voltage Corrected unit of L to µH for “Avalanche energy, repetitive” Corrected value of g_{fs} in the Table 4 Corrected diagrams "Typical transfer characteristic" and "Max. transient thermal impedance (MOSFET/diode)" Updated Figure D. Definition of QGD
1.30	2024-11-08	Corrected diagram $I_{frm} = f(-di_{SD}/dt)$ Editorial changes
1.40	2026-01-27	Increased I_{DM} in Table 2 Corrected conditions for Q_G, $Q_{GS(pl)}$ and Q_{GD} in Table 4 Added switching information for V_{GS} = -5/18 V in Table 4 and 6 and corresponding diagrams Added I_{SDC} in Table 5 Corrected test conditions and adapt values of the body diode in Table 6 Added SOA diagram on page 8 Added diagram $E = f(V_{DD})$ @ V_{GS} = 0/18 V Added diagram $E = f(V_{DD})$ @ V_{GS} = -5/18 V Editorial changes

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