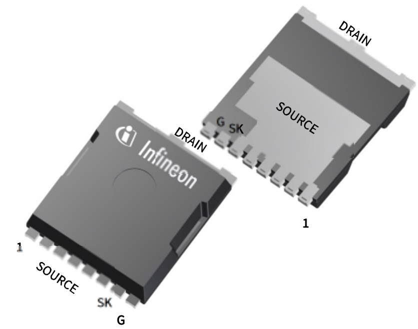
IGT40R070D1 E8220

400V CoolGaN™ enhancement-mode Power Transistor

The 400V CoolGaN™ family is the derivative of industry benchmark 600V CoolGaN™ technology, optimized for Class-D Audio amplifier applications.

Features

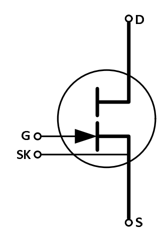
- Enhancement mode transistor – Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- Qualified according to JEDEC Standards (JESD47 and JESD22)



Gate	8
Drain	drain contact
Kelvin Source	7
Source	1,2,3,4,5,6

Benefits

- Improves efficiency due to best Figure Of Merit (FOM) in 400V class
- Exhibits very low noise level
- Lower THD compared to best-in-class Silicon switch
- Compatible with existing control ICs



Applications

- Class-D Audio Amplifier

Table 1 Key Performance Parameters at $T_j = 25$ °C

Parameter	Value	Unit
$V_{DS,max}$	400	V
$R_{DS(on),max}$	70	mΩ
$Q_{G,typ}$	4.5	nC
$I_{D,pulse}$	60	A
Q_{oss} @ 320 V	35	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Type / Ordering Code	Package	Marking	Related links
IGT40R070D1 E8220	PG-HSOF-8	40L070D1	NA

Table of Contents

1 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain Source Voltage [1]	$V_{DS,max}$	-	-	400	V	V_{GS} = 0 V
Continuous current, drain source	I_D	- - -	- - -	31 20 14	A	T_C = 25 °C; $T_j = T_{j,max}$ T_C = 100 °C; $T_j = T_{j,max}$ T_C = 125 °C; $T_j = T_{j,max}$
Pulsed current, drain source [2,3]	$I_{D,pulse}$	-	-	60	A	T_C = 25 °C; I_G = 26.1 mA; See Figure 3;Figure 21;
Pulsed current, drain source [3,4]	$I_{D,pulse}$	-	-	35	A	T_C = 125 °C; I_G = 26.1 mA; See Figure 4;Figure 22;
Gate current, continuous [4,5]	I_G	-	-	20	mA	T_j = 0 °C to 150 °C; Refer to gate drive app note
Gate current, pulsed [5]	$I_{G,pulse}$	-	-	2000	mA	T_j = 0 °C to 150 °C; t_{PULSE} = 50 ns, f=100 kHz Refer to gate drive app note
Gate source voltage, continuous [5]	V_{GS}	-10	-	-	V	T_j = 0 °C to 150 °C; Refer to gate drive app note
Gate source voltage, pulsed [5]	$V_{GS,pulse}$	-25	-	-	V	T_j = 0 °C to 150 °C; t_{PULSE} = 50 ns, f = 100 kHz; open drain Refer to gate drive app note
Power dissipation	P_{tot}	-	-	125	W	T_C = 25 °C
Operating temperature	T_j	0	-	150	°C	
Storage temperature	T_{stg}	0	-	150	°C	Max shelf life depends on storage conditions.
Drain-source voltage slew-rate	dV/dt			200	V/ns	

[1] All devices are 100% tested at I_{DS} = 12.2 mA to assure $V_{DS} \geq$ 800 V

[2] Limits derived from product characterization, parameter not measured during production

[3] Ensure that average gate drive current, I_G is ≤ 20 mA

[4] Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

[5] We recommend using an advanced driving technique to optimize the device performance. Please see application information for details.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1	°C/W	
Thermal resistance, junction-ambient	R_{thJA}	-	-	62	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction-ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm* 1.5mm epoxy PCB FR4 with 6cm^2 (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	245	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	I_{DS} = 2.6 mA; V_{DS} = 10 V; T_j =25 °C I_{DS} = 2.6 mA; V_{DS} = 10 V; T_j =125 °C
Drain-Source leakage current	I_{DSS}	- -	1 20	100 -	µA	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C V_{DS} = 400 V; V_{GS} = 0 V; T_j = 150 °C
Drain-Source leakage current at application conditions[1]	I_{DSSapp}	-	60	-	µA	V_{DS} = 320 V; V_{GS} = 0 V; T_j = 125 °C
Gate-Source leakage current	I_{GSS}	-1 -1	- -	- -	mA	V_{DS} = 0 V; V_{GS} = -10 V; T_j = 25 °C V_{DS} = 0 V; V_{GS} = -10 V; T_j = 125 °C
Drain-Source on-state resistance	$R_{DS(on)}$	- -	0.055 0.100	0.070 -	Ω	I_G = 26.1 mA; I_D = 8 A; T_j = 25 °C I_G = 26.1 mA; I_D = 8 A; T_j = 150 °C
Gate resistance	$R_{G,int}$	-	0.68	-	Ω	LCR impedance measurement; f = f_{res} ; open drain;

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	382	-	pF	V_{GS} = 0 V; V_{DS} = 320 V; f = 1 MHz
Output capacitance	C_{oss}	-	72	-	pF	V_{GS} = 0 V; V_{DS} = 320 V; f = 1 MHz
Reverse Transfer capacitance	C_{rss}	-	0.3	-	pF	V_{GS} = 0 V; V_{DS} = 320 V; f = 1 MHz
Effective output capacitance, energy related [2]	$C_{o(er)}$	-	84	-	pF	V_{DS} = 0 to 320 V
Effective output capacitance, time related [3]	$C_{o(tr)}$	-	109.4	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 320 V; Id = const
Output charge	Q_{oss}	-	35	-	nC	V_{DS} = 0 to 320 V
Turn- on delay time	$t_{d(on)}$	-	11	-	ns	see Figure 23
Turn- off delay time	$t_{d(off)}$	-	11	-	ns	see Figure 23
Rise time	t_r	-	7.5	-	ns	see Figure 23
Fall time	t_f	-	9	-	ns	see Figure 23

[1] Parameter represents end of use leakage in applications

[2] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as Coss while VDS is rising from 0 to 320 V

[3] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as Coss while VDS is rising from 0 to 320 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	4.5	-	nC	I_{GS} = 0 to 10 mA; V_{DS} = 320 V; I_D = 8 A

Table 8 Reverse conduction characteristics

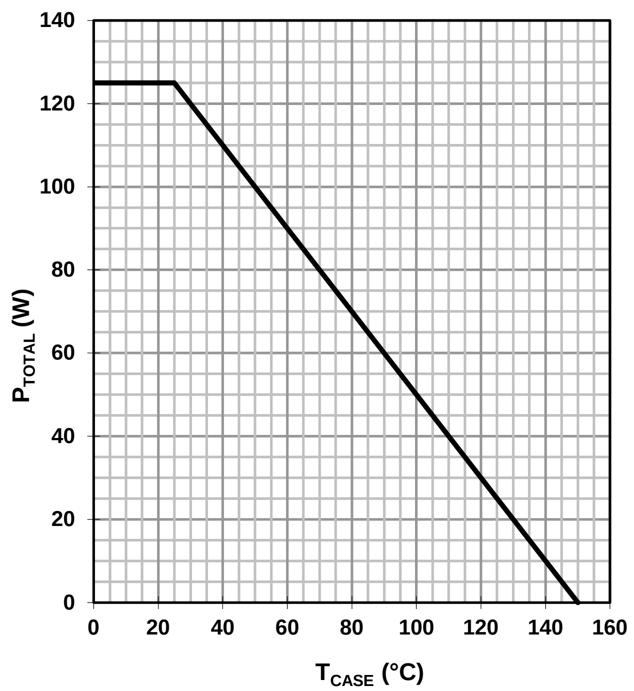
Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.0	2.5	V	V_{GS} = 0 V; I_{SD} = 8 A
Pulsed current, reverse	$I_{S,pulse}$	- -	- -	60	A	I_G = 26.1 mA
Reverse recovery charge	Q_{rr} [1]	-	0	-	nC	I_S = 8 A, V_{DS} = 320 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

[1] Excluding Qoss

4 Electrical characteristics diagrams

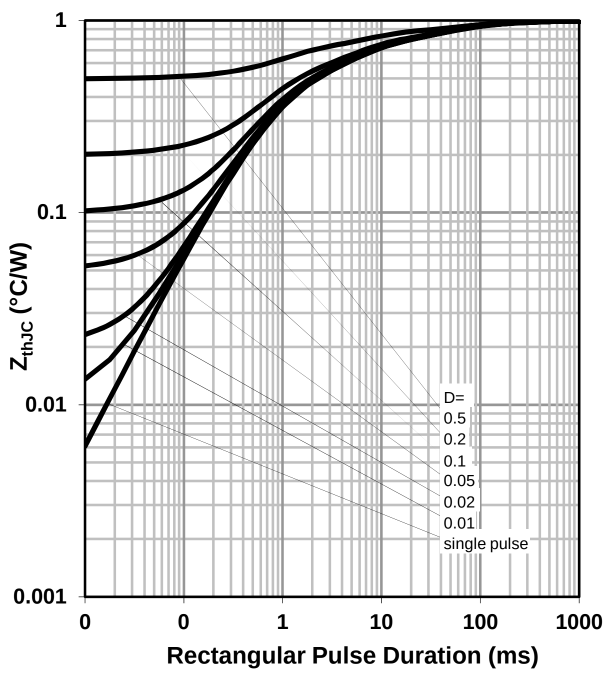
at T_j = 25 °C, unless specified otherwise

Figure 1 Power dissipation



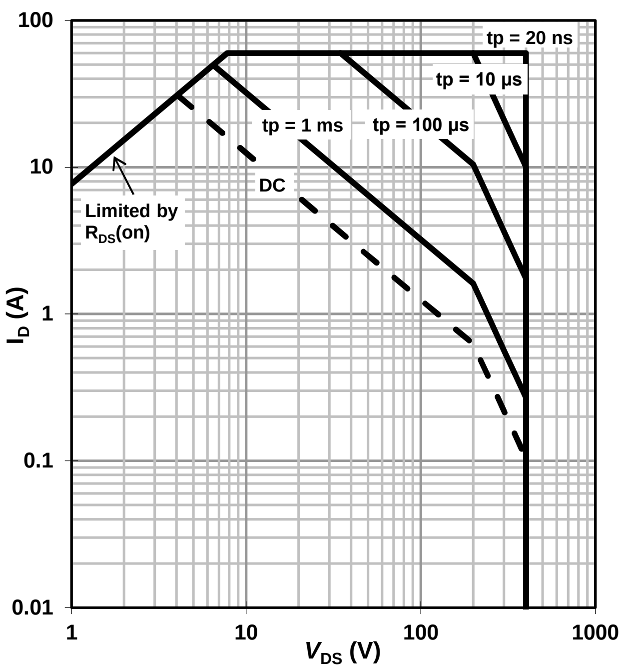
$P_{tot}=f(T_c)$

Figure 2 Max. transient thermal impedance



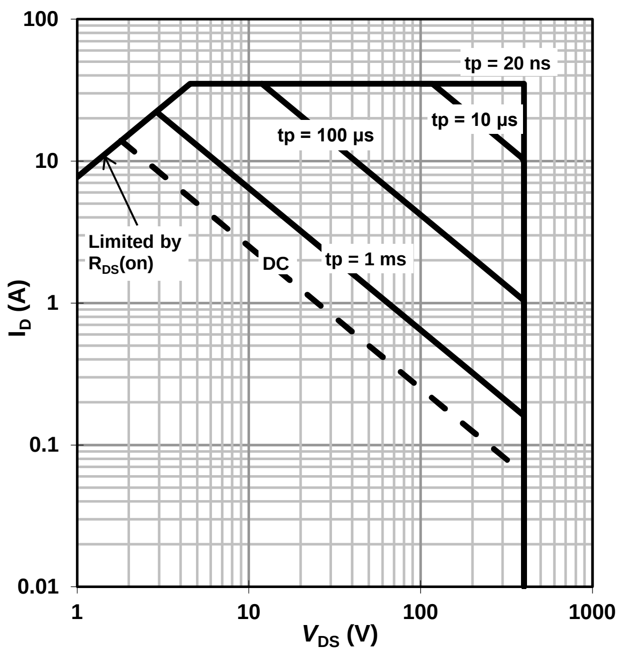
$Z_{thJC}=f(t_p, D)$

Figure 3 Safe operating area



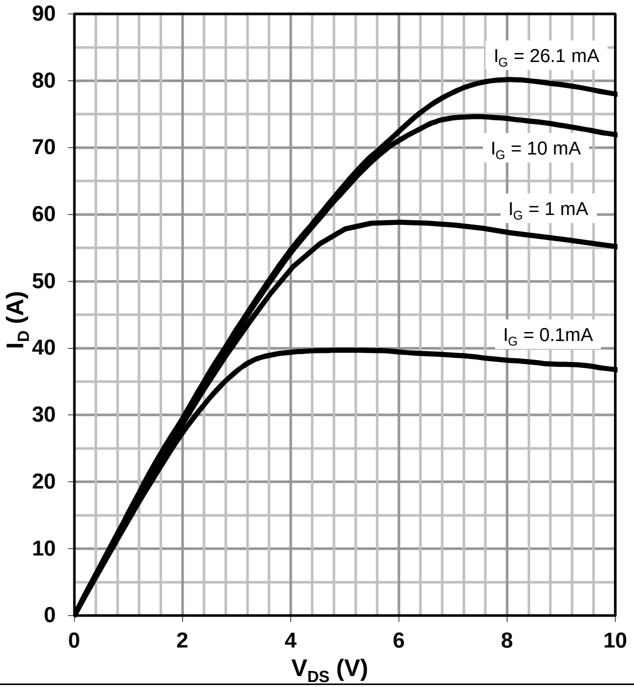
$I_D=f(V_{DS})$; T_C = 25 °C

Figure 4 Safe operating area



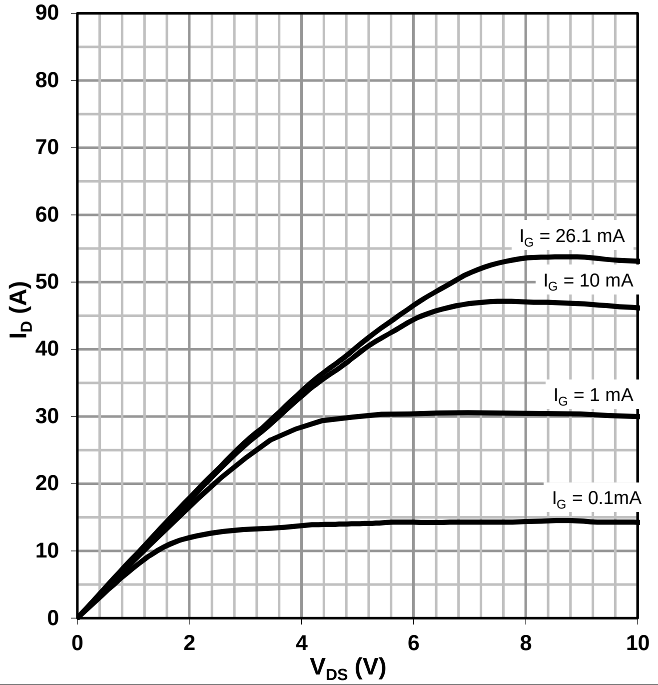
$I_D=f(V_{DS})$; T_C = 125 °C

Figure 5 Typ. output characteristics



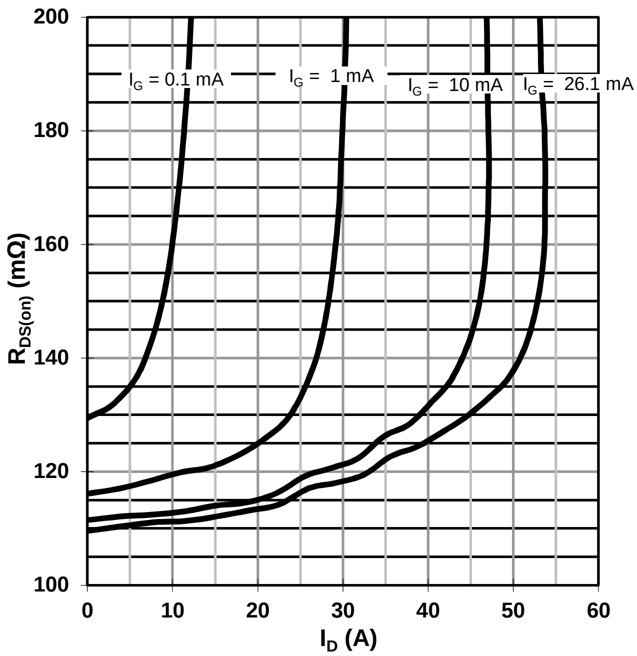
$I_D=f(V_{DS},I_G)$; $T_j = 25$ °C

Figure 6 Typ. output characteristics



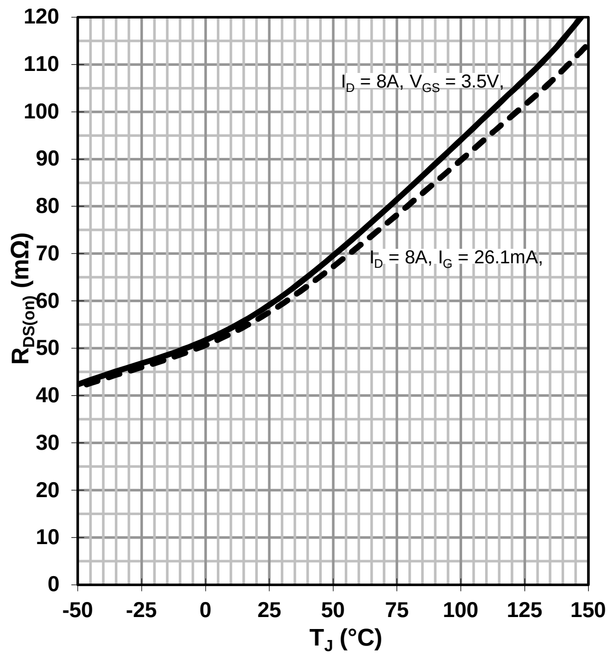
$I_D=f(V_{DS},I_G)$; $T_j = 125$ °C

Figure 7 Typ. Drain-source on-state resistance



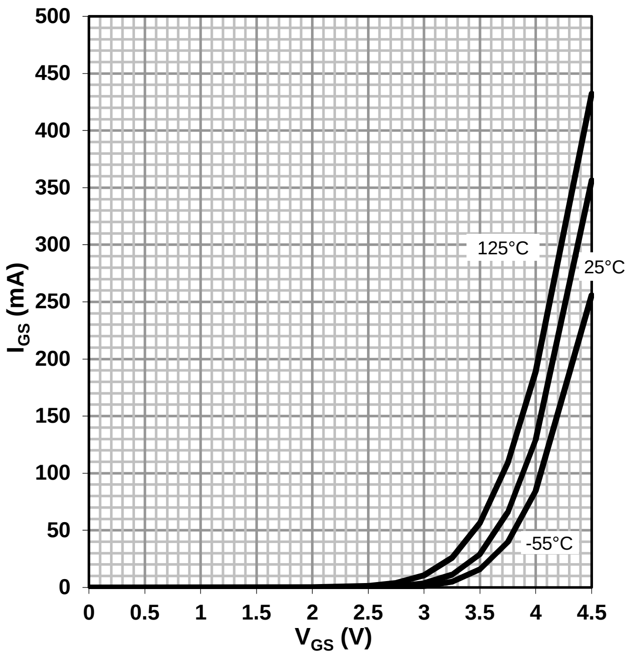
$R_{dson}=f(I_D,I_{GS})$; $T_j = 125$ °C

Figure 8 Drain-source on-state resistance



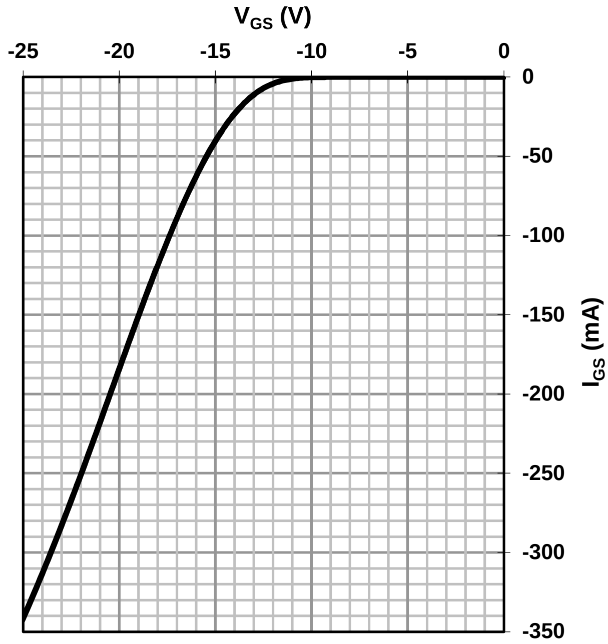
$R_{dson}=f(T_j)$; $I_D = 8$ A

Figure 9 Typ. gate characteristics forward



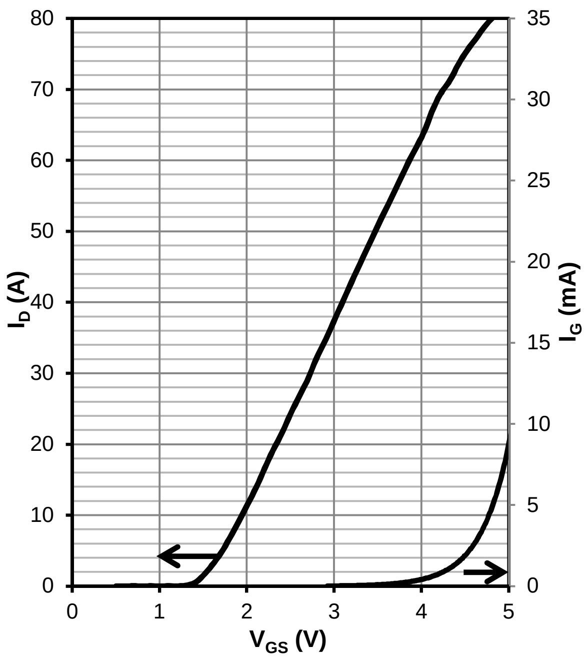
$I_{GS}=f(V_{GS}, T_j)$; open drain

Figure 10 Typ. gate characteristics reverse



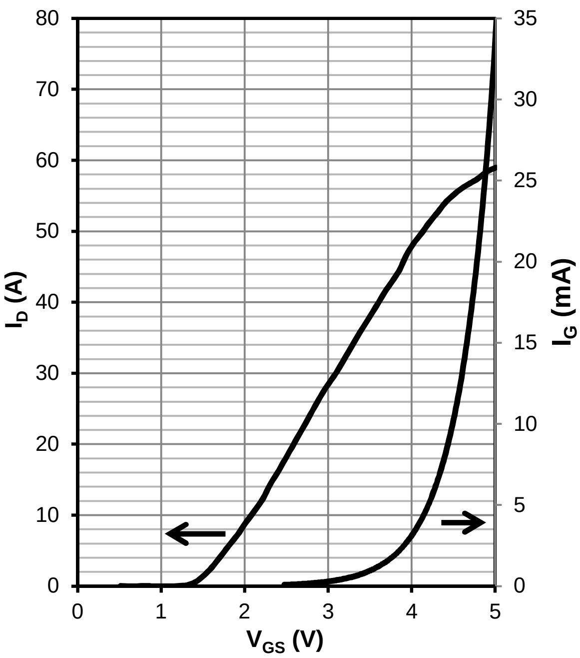
$I_{GS}=f(V_{GS})$; $T_j = 25$ °C

Figure 11 Typ. transfer characteristics



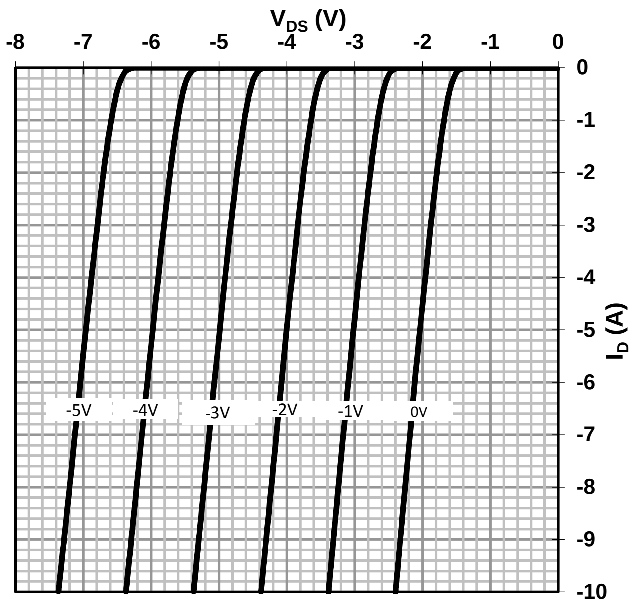
I_D, $I_G=f(V_{GS})$; $V_{DS} = 8$ V; $T_j = 25$ °C

Figure 12 Typ. transfer characteristics



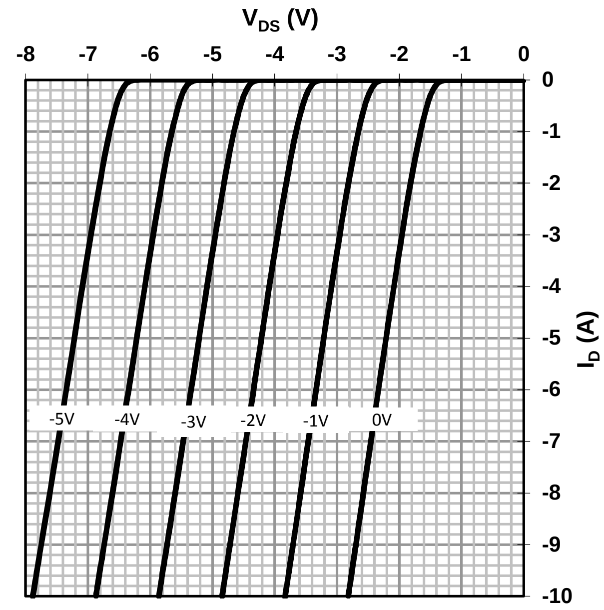
I_D, $I_G=f(V_{GS})$; $V_{DS} = 8$ V ; $T_j = 125$ °C

Figure 13 Typ. channel reverse characteristics



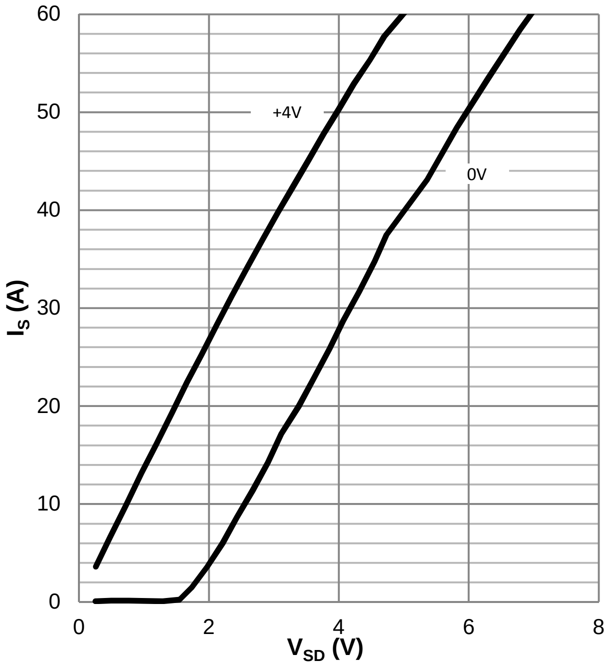
$V_{DS}=f(I_D, V_{GS})$; $T_j = 25$ °C

Figure 14 Typ. channel reverse characteristics



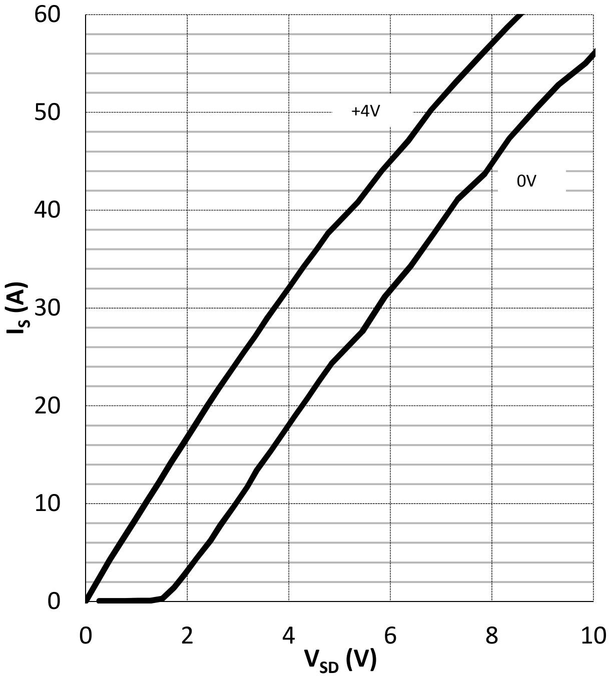
$V_{DS}=f(I_D, V_{GS})$; $T_j = 125$ °C

Figure 15 Typ. channel reverse characteristics



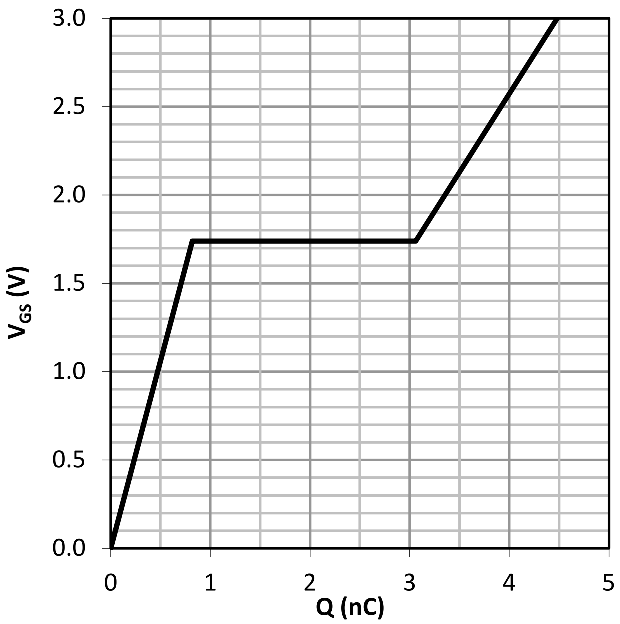
$I_D=f(V_{DS}, V_{GS})$; $T_j = 25$ °C

Figure 16 Typ. channel reverse characteristics



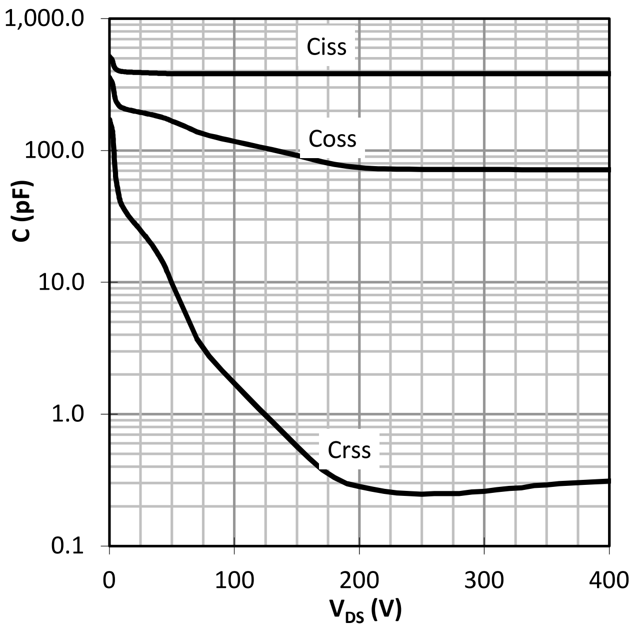
$I_D=f(V_{DS}, V_{GS})$; $T_j = 125$ °C

Figure 17 Typ. gate charge



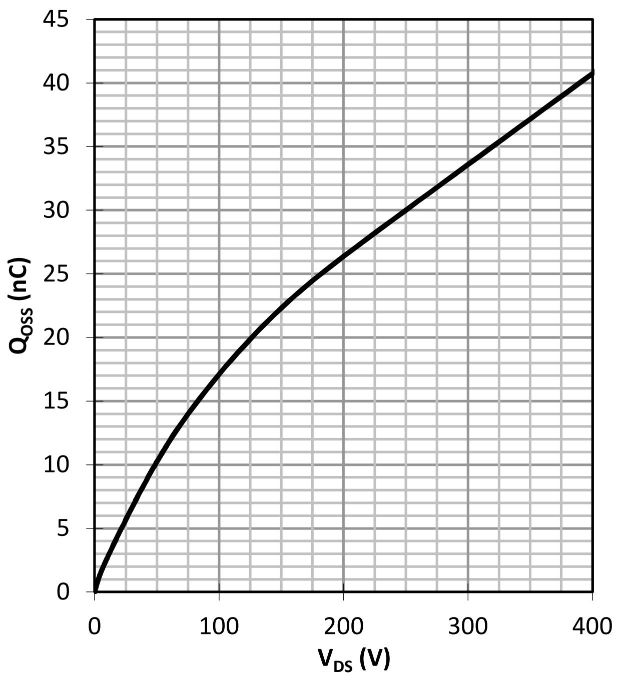
$V_{GS} = f(Q_G)$; V_{DCLINK} = 320 V; I_D = 8 A

Figure 18 Typ. capacitances



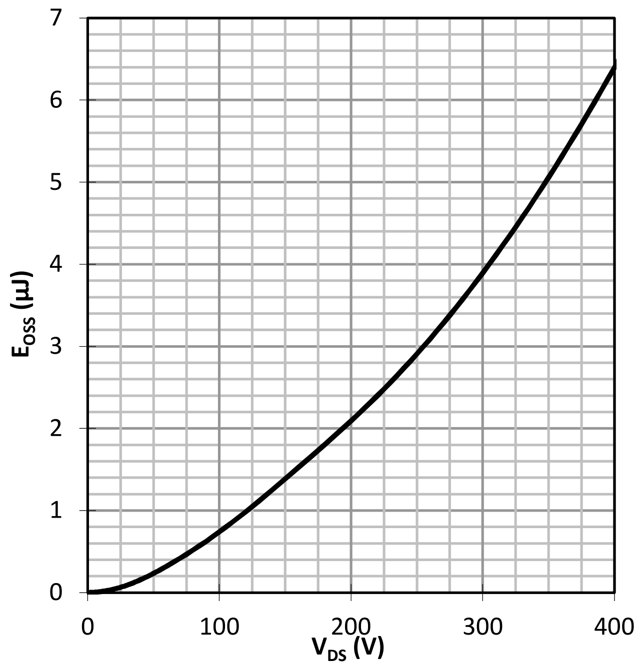
$C_{xss} = f(V_{DS})$

Figure 19 Typ. output charge

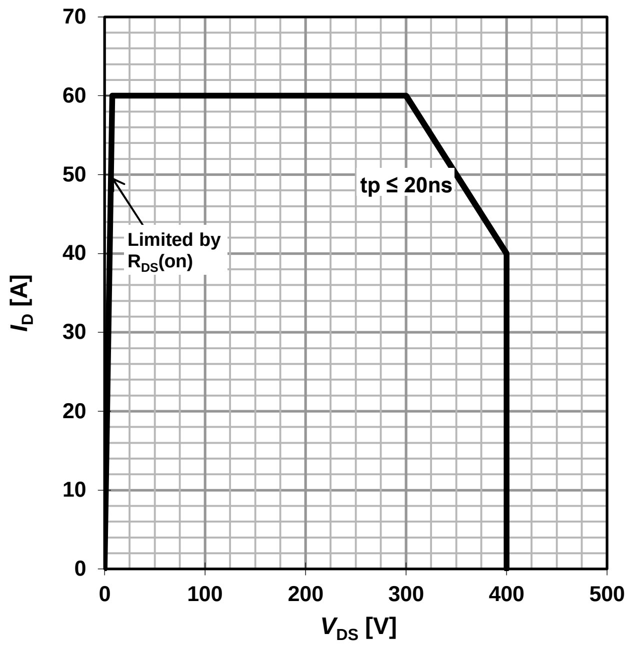
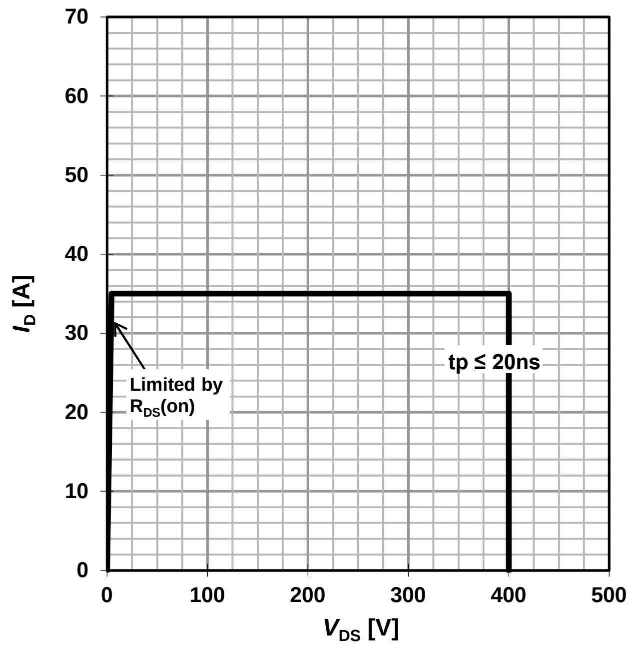


$Q_{OSS} = f(V_{DS})$

Figure 20 Typ. Coss stored Energy



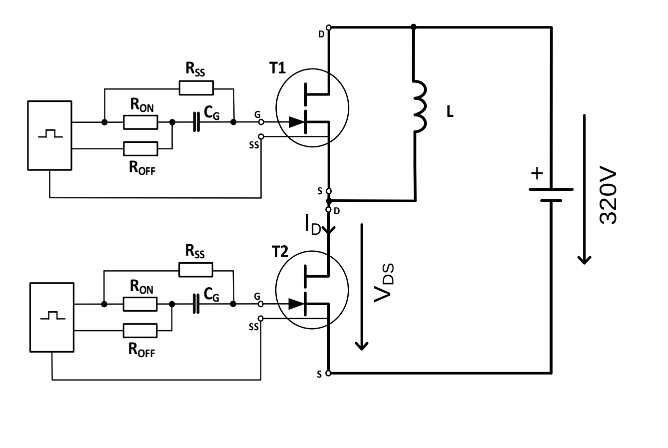
$E_{OSS} = f(V_{DS})$

Figure 21 Repetitive safe operating area[1]	Figure 22 Repetitive safe operating area[1]
	
Tc = 25 °C; T_j ≤ 150 °C	Tc = 125 °C; T_j ≤ 150 °C

[1] Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

5 Test Circuits

Figure 23 Switching times with inductive load



$I_D = 8A$, $R_{ON} = 10\ \Omega$; $R_{OFF} = 10\ \Omega$; $R_{SS} = 820\ \Omega$; $C_G = 2\ nF$; $V_{DRV} = 12V$

Figure 24 Switching times waveform

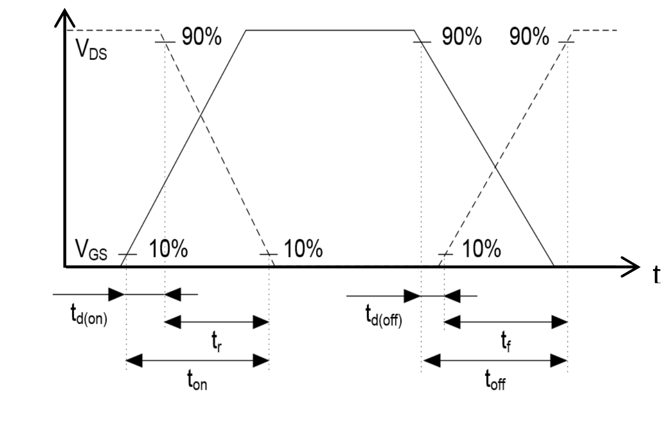
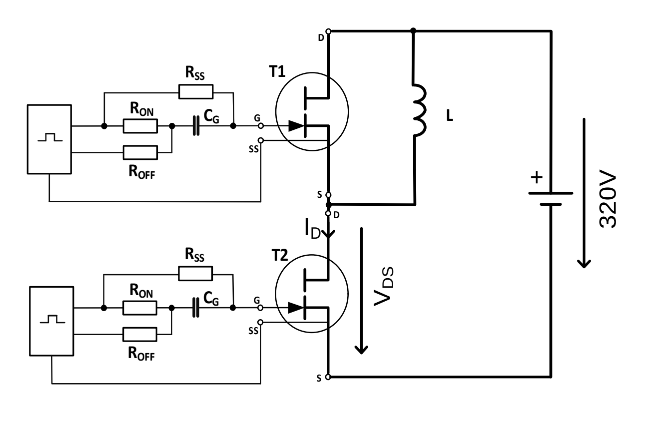
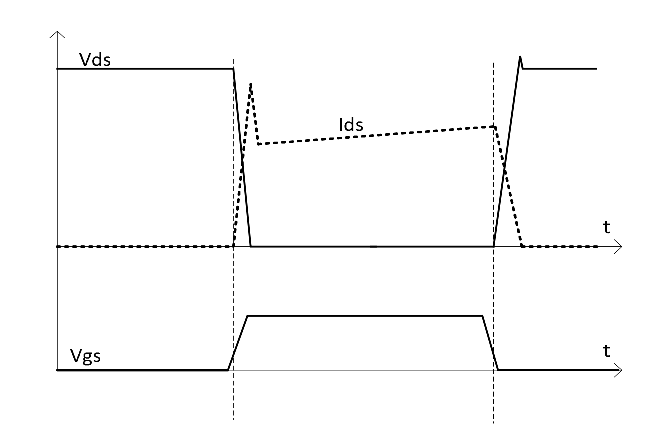


Figure 25 Reverse Channel Characteristics



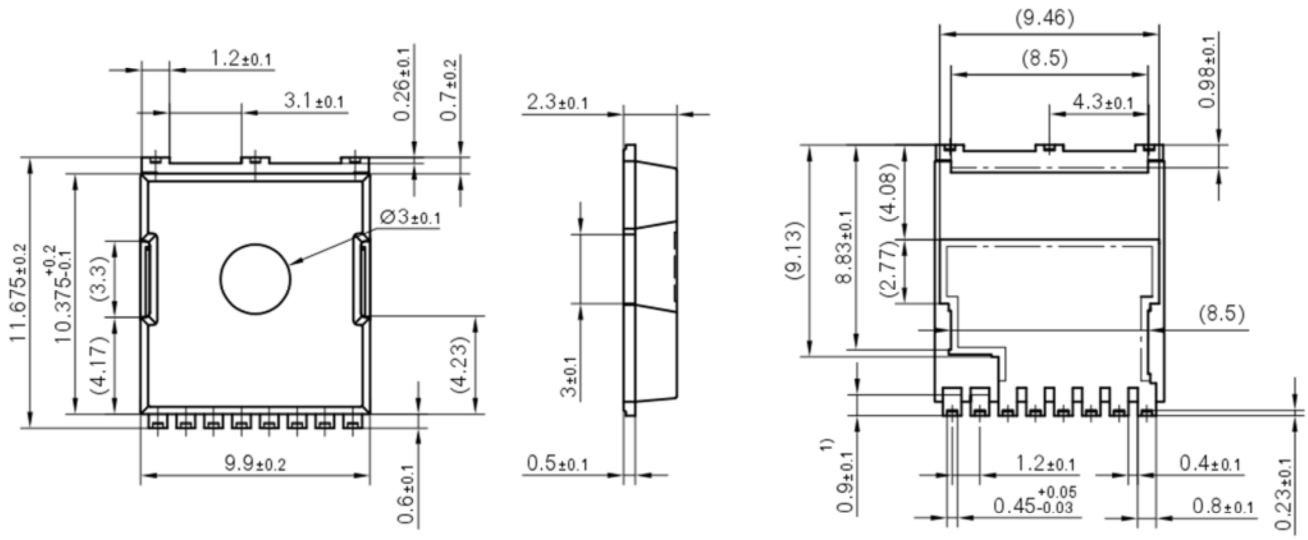
$I_D = 8\ A$, $R_{ON} = 10\ \Omega$; $R_{OFF} = 10\ \Omega$; $R_{SS} = 820\ \Omega$; $C_G = 2\ nF$; $V_{DRV} = 12V$

Figure 26 Typ. Rev. Channel Recovery



The recovery charge is Q_{OSS} only, no additional Q_{rr}

6 Package Outlines



1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED.
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Figure 27 PG-HSOF-8 Package Outline, dimensions (mm)

7 Revision History

Major changes since the last revision

Revision	Date	Description of change
2.0	2018-04-25	Release of final version

Edition 2018-04-25

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

ifx1