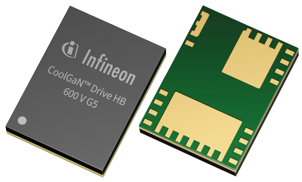
CoolGaN™ Drive HB 600 V G5

110 mΩ / 600 V GaN half-bridge with level-shift gate drivers



Features

- Two 110 mΩ GaN switches in half-bridge configuration with integrated high- and low-side gate drivers
  - Source / sink driving current +0.29 A / -0.7 A
  - Application-configurable turn-on and turn-off speed
  - Integrated ultra-fast low-resistance bootstrap diode
- Fast input-to-output propagation (typ. 98 ns) with extremely small channel-to-channel mismatch
- PWM input signal
- Standard logic input levels compatible with digital controllers
- Single gate driver supply voltage (typ. 12 V) with fast UVLO recovery
- Low-side open source for current sensing with external shunt resistor
- Thermally enhanced 6 x 8 mm TFLGA-27 package
- Product is fully qualified acc. JEDEC for Industrial Applications

Description

IGI60L1111B1M combines a half-bridge power stage consisting of two 110 mΩ (typ. R_{dson}) / 600 V enhancement-mode CoolGaN™ switches with integrated gate drivers in a small 6 x 8 mm TFLGA-27 package. In the low-to-medium power area (example configuration in **Figure 1**), it is thus ideally suited to support the design of high-density motor drives and SMPS utilizing the superior switching behavior of CoolGaN™ power switches.
Infineon's CoolGaN™ and related power switches provide a very robust gate structure. When driven by a continuous gate current of a few mA in the "on" state, a minimum on-resistance R_{dson} is always guaranteed.

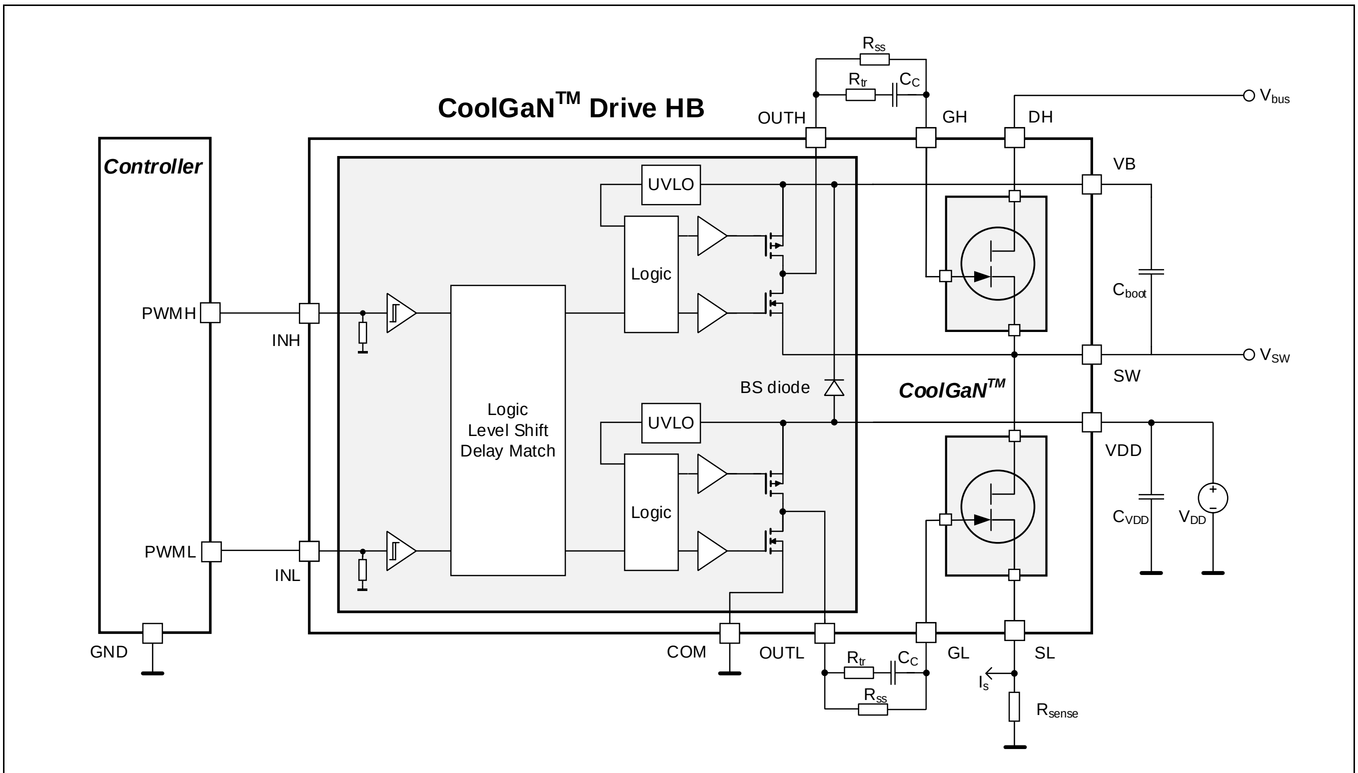


Figure 1 Typical configuration circuit

Due to the GaN-specific low threshold voltage and the fast-switching transients, a negative gate drive voltage is required in certain applications to both enable fast turn-off and avoid cross-conduction effects. This can be achieved by the well-known RC interface between driver and switch. A few external SMD resistors and caps enable easy adaptation to different power topologies.
The driver utilizes Infineon's SOI-technology to achieve an excellent ruggedness and noise immunity with capability to maintain operational logic at negative gate voltages. The floating channel can be used to drive the high side GaN die with integrated bootstrap configuration.

Applications

- Low power motor drives
- Low power SMPS

Power Topologies

- Single-phase or multiphase two-level inverters

Product Versions

Table 1 CoolGaN™ Drive HB 600 V G5 product overview

Part Number / Ordering code	OPN	Package	Typ. R_{dson} high- / low-side	Marking
IGI60L1111B1M	IGI60L1111B1MXUM A1	PG-TFLGA-27-2 6 x 8 mm	110 mΩ / 110 mΩ	60L1111B
IGI60L1414B1M	IGI60L1414B1MXUM A1	PG-TFLGA-27-2 6 x 8 mm	140 mΩ / 140 mΩ	60L1414B
IGI60L2727B1M	IGI60L2727B1MXUM A1	PG-TFLGA-27-2 6 x 8 mm	270 mΩ / 270 mΩ	60L2727B
IGI60L5050B1M	IGI60L5050B1MXUM A1	PG-TFLGA-27-2 6 x 8 mm	500 mΩ / 500 mΩ	60L5050B

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1 Pin configuration and description

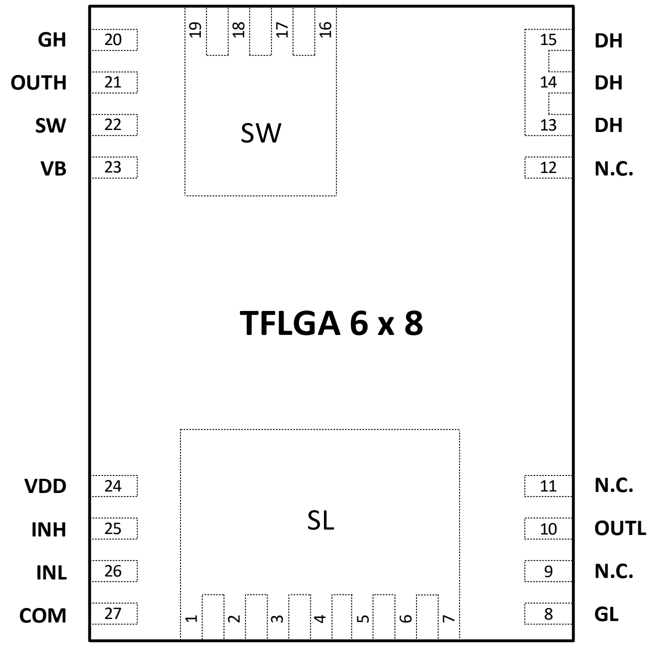


Figure 2 Pin configuration and exposed pads for TFLGA-27 6 x 8 mm package, top view (not to scale)

Table 2 Pin description

Pin No.	Symbol	Description
1 - 7	SL	Source connection low-side switch
8	GL	Gate connection low-side switch
10	OUTL	Driver output low-side
13 - 15	DH	Drain connection high-side switch
16 - 19	SW	Half-bridge output (switching node)
22	SW	Must be connected to switch node at PCB level[1]
20	GH	Gate connection high-side switch
21	OUTH	Driver output high-side
23	VB	High-side gate drive floating supply
24	VDD	Low-side and logic supply voltage
25	INH	Input signal (default state “Low”); controls high-side switch
26	INL	Input signal (default state “Low”); controls low-side switch
27	COM	Low-side gate drive return
9,11,12	N.C.	Not connected pin

[1] Straight trace from Pin 22 to SW exposed pad.

2 Functional description

2.1 Block Diagram

A simplified functional block diagram of the CoolGaN™ Power Stage is given in Figure 3.

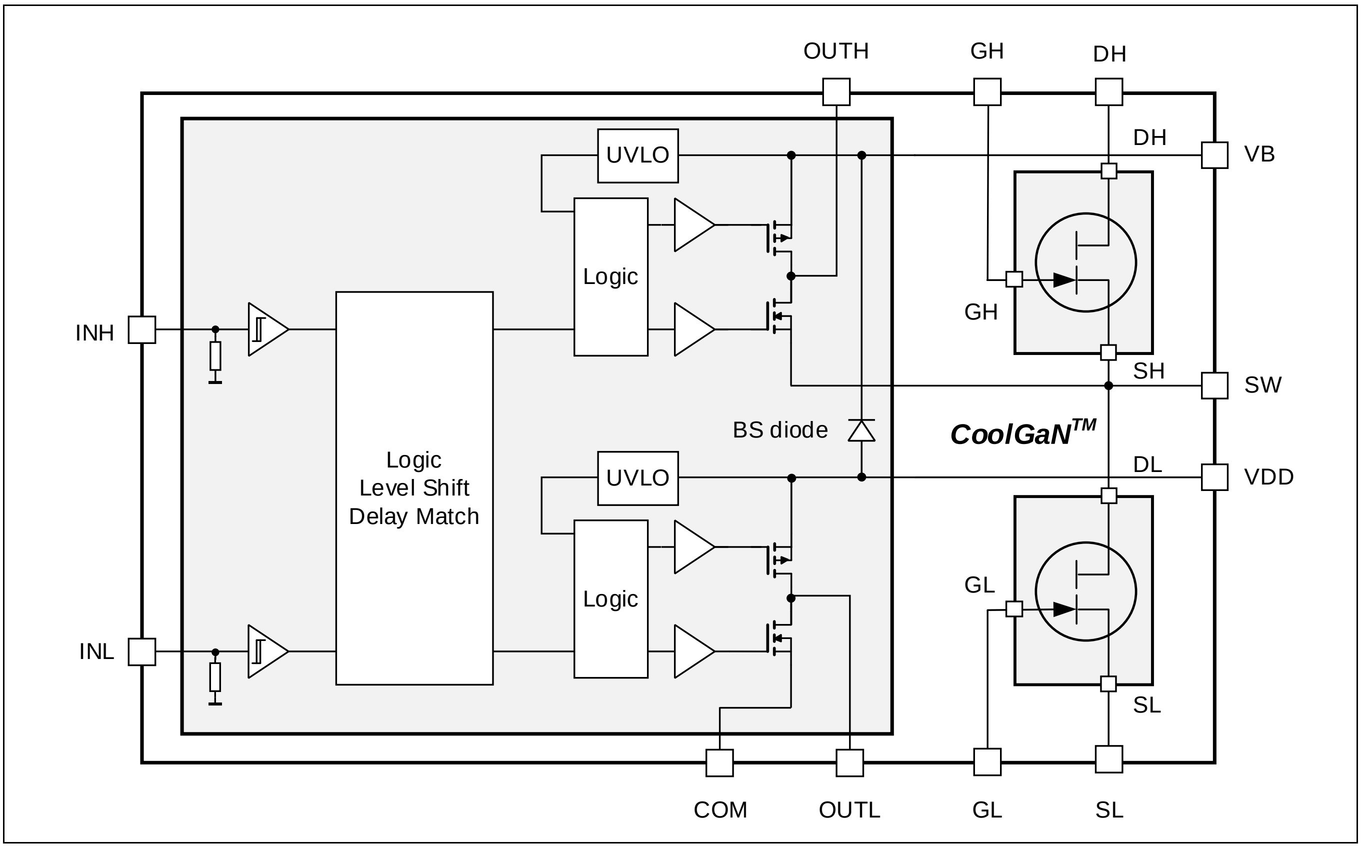


Figure 3 Block Diagram IGI60L1111B1M

2.2 Power supply

The power stage requires a ground-related V_{DD} supply for the low-side driver. The high-side driver is supplied by V_B in bootstrap configuration with integrated bootstrap diode. Independent Undervoltage Lockout (UVLO) functions for both VDD and VB voltages ensure a defined start-up and robust functionality under all operating conditions. VDD has to be supplied by typical 12 V related to the source of the low-side GaN switch.

2.3 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the gate drive outputs can be switched to their high level only, if both VDD and VB supply voltages exceed the corresponding UVLO threshold voltages. Thus it can be guaranteed, that the GaN switches are in “off” state, if the driving voltage is too low for complete and fast switching on, thereby avoiding excessive power dissipation and keeping the switch transistors within their safe operating area (SOA). The UVLO levels for the low-side supply voltage V_{DD} and high-side bootstrap voltage V_B are set to a typical “on”-value of 8.9 V (with 0.9 V hysteresis).

2.4 CoolGaN^{TM} output stage

The output stage consists of two CoolGaN^{TM} 600 V switches in half-bridge configuration. The switches are characterized by a typical R_{dson} of 110 mΩ @ 25 °C. And thanks to the current driving concept, this value increases by a comparably moderate 85 % @ 150 °C. As typical for GaN, gate and output charges are very small and there is no reverse recovery charge due to the lack of a physical body diode.

3 Characteristics

3.1 Absolute maximum ratings

The absolute maximum ratings are listed in **Table 3**. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Conditions
		Min.	Max.		
Voltage between output pins DH, SW and SL	V_{DHSW} V_{SWSL}	— —	600 600	V V	 V_{GHSW} = 0 V, V_{GLSL} = 0 V
Drain-to-source voltage pulsed	$V_{DS,pulse}$	— —	750[1] 750	V V	T_J = 25°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 10h T_J = 125°C, V_{GS} ≤ 0 V, cumulated stress time ≤ 1h
Continuous drain current	I_D	— —	7.4 5.8	A A	T_{Case} = 25°C T_{Case} = 125°C
Pulsed drain current[2]	$I_{D,pulse}$	— —	30 18[3]	A A	T_{Case} = 25°C, I_G = 13mA T_{Case} = 125°C, I_G = 13mA
Voltage at pin VDD	V_{DD}	-1	24	V	with respect to SL
Voltage at pin VB	V_B	-1	24	V	with respect to SW
Voltage at pins INL, INH	V_{IN}	-5	V_{DD} + 0.5	V	
Junction temperature	T_J	- 40	150	°C	
Storage temperature	T_S	- 55	150	°C	
Soldering temperature	T_{sold}	—	260	°C	reflow/wave soldering[4]
ESD capability	V_{ESD_HBM}	—	1.5	kV	Human Body Model[5]
	V_{ESD_CDM}	—	1.0	kV	Charged Device Model[6]

[1] Acc to JEDEC-JEP180
[2] Limits derived from product characterization, parameter not measured during production
[3] Parameter is influenced by reliability requirements. Please contact the local Infineon Sales Office to get an assessment of your application
[4] Acc. to JESD22A111
[5] Acc. to EIA/JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)
[6] Acc. to JESD22-002

3.2 Thermal characteristics

Table 4 **Thermal characteristics**

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction-case	R_{thJC}	—	4.0	—	°C/W	
Thermal resistance junction-ambient 4-layer each GaN device	R_{thJA}	—	52	—	°C/W	Device mounted on 2s2p 4-layer PCB with 600 mm^2 total cooling area

3.3 Recommended operating range

Table 5 **Recommended operating range**

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Low-side output voltage	V_{DD}	10	12	20	V	min. defined by UVLO
High-side floating well supply voltage	V_{BS}	10	12	20	V	min. defined by UVLO
Bootstrap voltage	V_B	V_{SW} + 10	—	V_{SW} + 20	V	
Logic input voltage at pins INL and INH	V_{IN}	-4	—	V_{DD}	V	
Gate current, continuous[1] [2]	$I_{G, avg}$	—	—	10	mA	
Junction temperature	T_J	-40	—	125 [3]	°C	

[1] Parameter is influenced by rel-requirements. Contact the local Infineon Sales Office to get an assessment of your application.
[2] We recommend to use RC interface gate drive to optimize the device performance. Please see gate drive application note for details.
[3] Continuous operation above 125°C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted, min/max values of characteristics are the lower and upper limits, resp. They are valid within the full operating range. All values are given at T_J = 25 °C with (V_{DD} - V_{SL}) = (V_B - V_{SW}) = 15 V.

Table 6 Static gate driver electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
V_{BS} supply undervoltage lockout turn-on threshold	V_{BSUV+}	8.2	8.9	9.6	V	
V_{BS} supply undervoltage lockout turn-off threshold	V_{BSUV-}	7.3	8.0	8.7	V	
V_{BS} supply undervoltage hysteresis	V_{BSUVHY}	—	0.9	—	V	
V_{DD} supply undervoltage lockout turn-on threshold	V_{DDUV+}	8.2	8.9	9.6	V	
V_{DD} supply undervoltage lockout turn-off threshold	V_{DDUV-}	7.3	8.0	8.7	V	
V_{DD} supply undervoltage hysteresis	V_{DDUVHY}	—	0.9	—	V	
High-side gate driver leakage current	I_{LK}	—	1	—	µA	V_B = V_{SW} = 600 V
Quiescent V_{BS} supply current	I_{QBS}	—	160	245	µA	V_{IN} = 0V or 5V
Quiescent V_{DD} supply current	I_{QDD}	—	400	650	µA	
High level output voltage drop, V_{DD} – V_{OUTL} , V_B – V_{OUTH}	V_{OH}	—	0.05	0.2	V	I_O = 2 mA
Low level output voltage drop, V_{OUTL} – V_{SL} , V_{OUTH} – V_{SW}	V_{OL}	—	0.02	0.1	V	
Peak output current turn-on	I_{o+}	—	290	—	mA	V_O = 0 V, PW ≤ 10 µs
Peak output current turn-off	I_{o-}	—	700	—	mA	V_O = 15 V, PW ≤ 10 µs
Logic "1" input voltage (rising edge)	V_{IH}	1.7	2.1	2.4	V	V_{DD} = 10 V to 20 V
Logic "0" input voltage (falling edge)	V_{IL}	0.7	0.9	1.1	V	
Gate driver input pin current output high	I_{IN+}	—	25	70	µA	V_{IN} = 5 V

Gate driver input pin current output low	I_{IN-}	—	—	5	µA	V_{IN} low
Bootstrap diode forward voltage between VDD and VB	V_{FBSD}	—	1	1.2	V	$I_F = 0.3$ mA
Bootstrap diode forward current between VDD and VB	I_{FBSD}	25	80	130	mA	$V_{DD} - V_B = 4$ V
Bootstrap diode resistance	R_{BSD}	15	36	54	Ω	

Table 7 Dynamic gate driver electrical characteristics (see Figure 4)

All values are given at $T_J = 25$ °C with ($V_{DD} - V_{SL}$) = ($V_B - V_{SW}$) = 15 V and $C_L = 1000$ pF unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Turn-on propagation delay	t_{ON}	—	90	110	ns	Vin = 5V, $V_{SL} = 0$ V
Turn-off propagation delay	t_{OFF}	—	90	110	ns	Vin = 5V, $V_{SL} = 0$ V
Turn-on rise time	t_R	—	70	170	ns	Vin = 5V, $V_{SL} = 0$ V
Turn-off fall time	t_F	—	35	90	ns	Vin = 5V, $V_{SL} = 0$ V
Delay matching time (HS & LS turn-on/off)[1]	MT	—	—	10	ns	

[1] Parameter not subject to production test. Parameter guaranteed by design and characterization.

Table 8 Output characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
R_{dson} high-side	R_{dshs}	—	110	140	mΩ	I_G = 13 mA, I_D = 4 A, T_J = 25°C
		—	240	—	mΩ	I_G = 13 mA, I_D = 4 A, T_J = 150°C
R_{dson} low-side	R_{dsls}	—	110	140	mΩ	I_G = 13 mA, I_D = 4 A, T_J = 25°C
		—	240	—	mΩ	I_G = 13 mA, I_D = 4 A, T_J = 150°C
Drain-source leakage current	I_{leakhs}, I_{leakls}	—	0.5	51	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 25°C
		—	10	—	µA	V_{DS} = 600 V, V_{GS} = 0 V, T_J = 150°C
Total gate charge (per switch)[1]	Q_G	—	2.4	—	nC	V_{GS} = 0 to 3 V, V_{DS} = 400 V, I_D = 4 A

Table 9 Static characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9	1.2	1.6	V	I_{DS} = 1.3 mA, V_{DS} = 10 V, T_J = 25 °C
		—	1.0	—	V	I_{DS} = 1.3 mA, V_{DS} = 10 V, T_J = 150°C
Gate-source reverse clamping voltage	$V_{GS,\ clamp}$	—	—	-8	V	I_{GSS}[2] = -1 mA, T_J =25 °C
Gate resistance	$R_{G,int}$	—	0.96	—	Ω	LCR impedance measurement

[1] Verified by design / characterization, not tested in production

[2] Gate-Source leakage current

Table 10 Dynamic characteristics GaN switches

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	—	170	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Output capacitance	C_{oss}	—	29	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Reverse transfer capacitance	C_{rss}	—	0.39	—	pF	V_{GS} = 0 V, V_{DS} = 400 V; f = 1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	—	33	—	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective output capacitance, time related[2]	$C_{o(tr)}$	—	45	—	pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Output charge	Q_{oss}	—	18	—	nC	V_{DS} = 0 to 400 V

Table 11 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	—	2.2	3	V	V_{GS} = 0 V, I_{SD} = 4 A
Pulsed current, reverse	$I_{S,pulse}$	—	—	30	A	I_G = 13 mA
Reverse recovery charge	Q_{rr}[3]	—	0	—	nC	I_{SD} = 4 A, V_{DS} = 400 V
Reverse recovery time	t_{rr}	—	0	—	ns	
Peak reverse recovery current	I_{rrm}	—	0	—	A	

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

[3] Excluding Q_{oss}

3.5 Timing diagrams and undervoltage lockout

The relationships between the input digital signal INL, INH and the gate signals OUTH, OUTL are illustrated below in **Figure 4.** From this figure, we can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

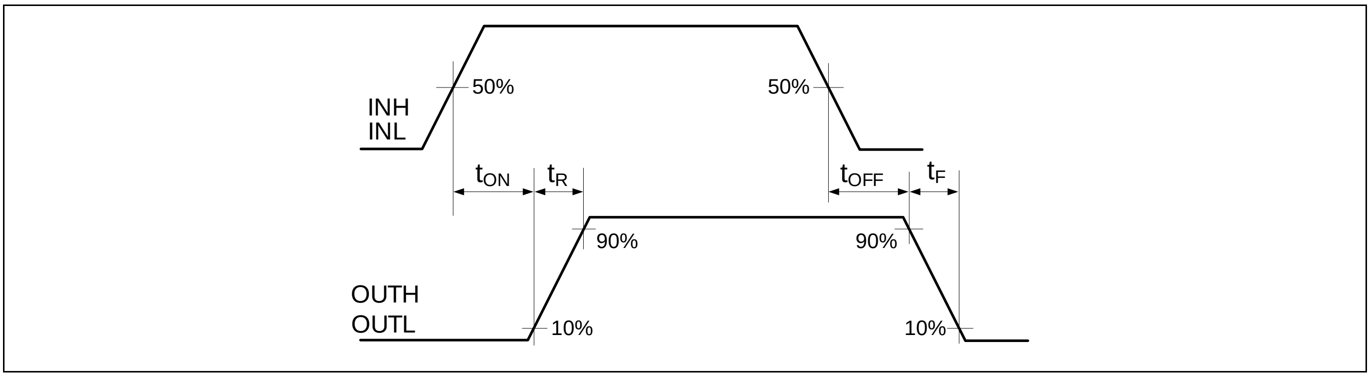


Figure 4 Propagation delay, rise and fall time

IGI60L1111B1M is designed with propagation delay matching circuitry. With this feature, the integrated gate driver IC's response at the output to a signal at the input requires approximately the same time duration (i.e., tON, tOFF) for both the low-side channels and the high-side channels as shown in **Figure 5**. The maximum difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the integrated gate driver is matched to the propagation turn-off delay (t_{OFF}).

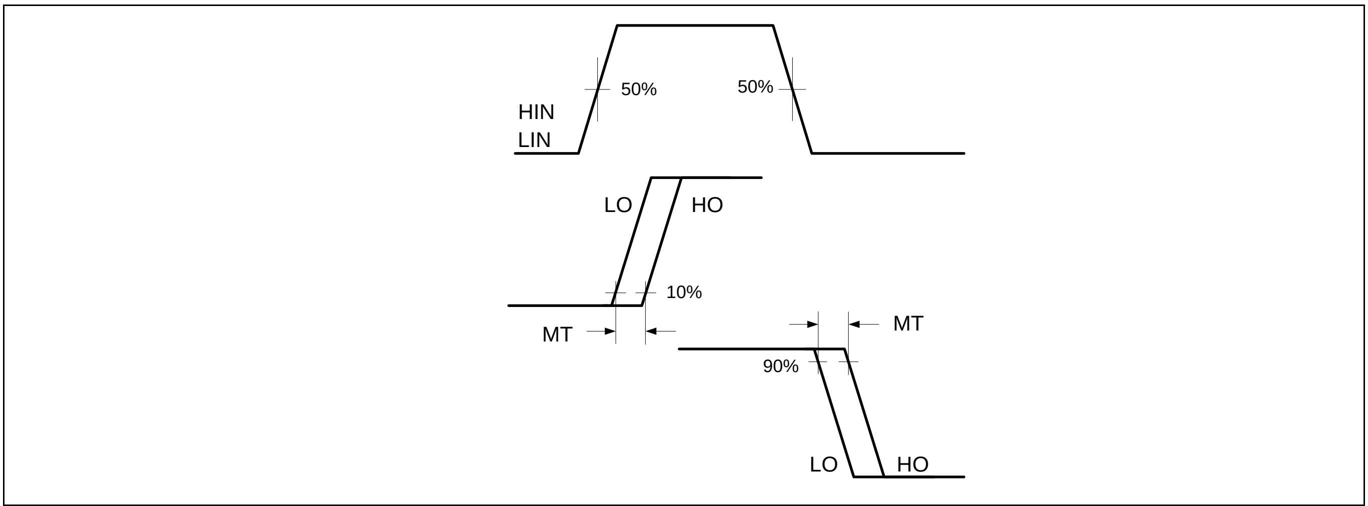


Figure 5 Delay matching waveform definition

IGI60L1111B1M provides undervoltage lockout protection on both the V_{DD} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. **Figure 6** is used to illustrate this concept; V_{DD} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{DDUV+/-}$ or $V_{BSUV+/-}$) the undervoltage protection is enabled or disabled.

Upon power-up, should the V_{DD} voltage fail to reach the V_{DDUV+} threshold, the IC won't turn-on. Additionally, if the V_{DD} voltage decreases below the V_{DDUV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs. The same behavior is valid for V_{BS}.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

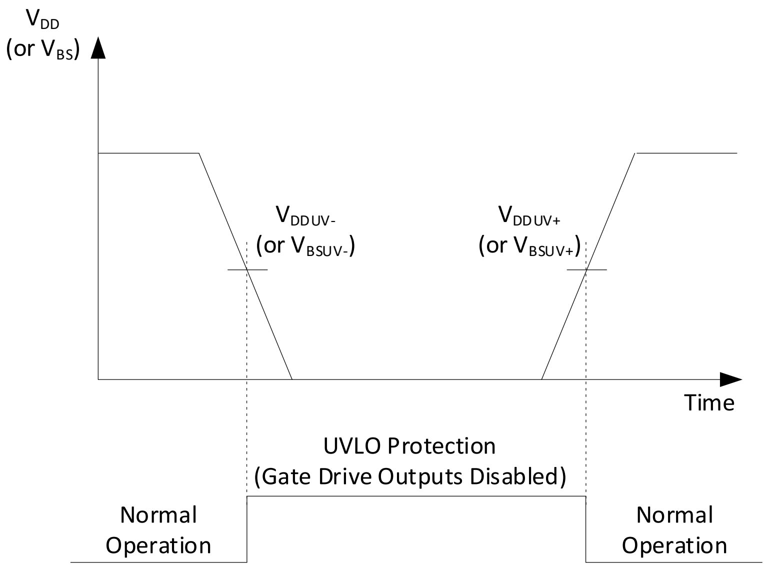


Figure 6 UVLO behavior, start-up and deactivation time (unloaded output)

4 Driving CoolGaN™ HEMTs

Although Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) with ohmic connection to a pGaN gate are robust enhancement-mode ("normally-off") devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in **Figure 7**. In the steady "on" state a continuous gate current is required to achieve stable operating conditions. The switch is "normally-off", but the threshold voltage V_{th} is rather low (~ +1 V). This is why in many applications a negative gate voltage $-V_N$, typically in the range of several Volts, is required to safely keep the switch "off" (**Figure 7b**).

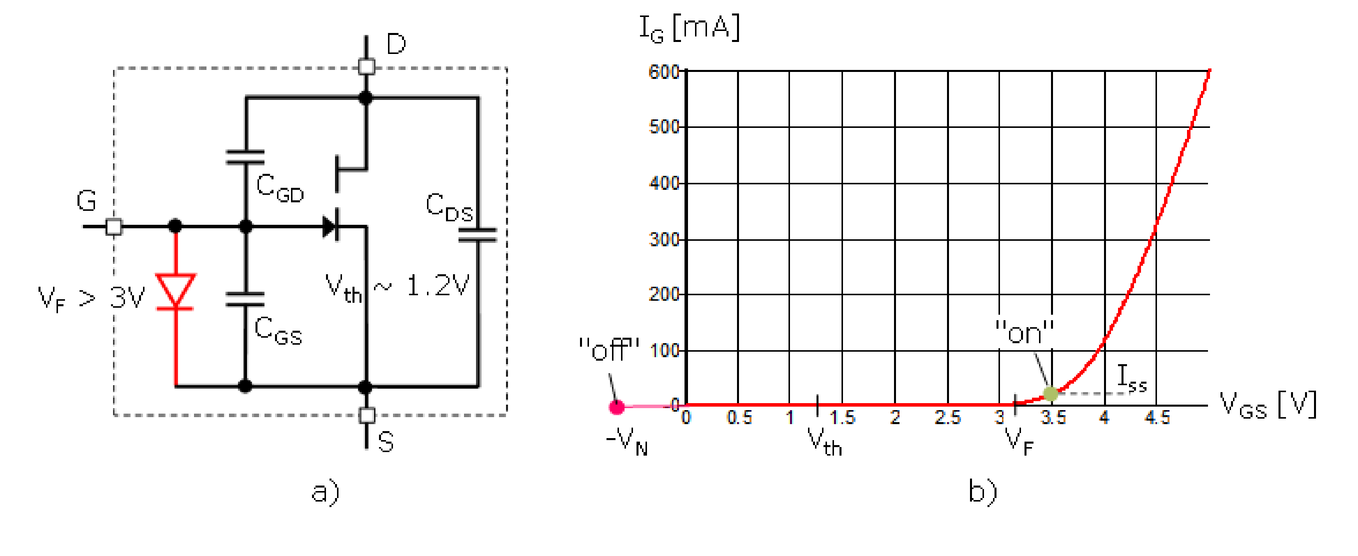


Figure 7 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

Obviously the transistor in **Figure 7** cannot be driven like a conventional MOSFET due to the need for a steady-state "on" current I_{ss} and a negative "off" voltage $-V_N$. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. To avoid a dedicated driver with 2 separate "on" paths and bipolar supply voltage, the solution depicted in **Figure 8** is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{on} and R_{off}, respectively, are connected to the gate via a coupling capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the "on"-state C_C is charged to the difference of driver supply V_{DD} and diode voltage V_F. When switching off, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value:

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}} \quad (2)$$

(with Q_G denoting the total gate charge $Q_{GS} + Q_{GD}$) V_N can thus be controlled by proper choice of V_{DD} and C_C. During the „off" state the negative V_{GS} decreases, as C_C is discharged via R_{SS}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 µs range. The negative gate voltage at the end of the "off" phase (V_{Nf} in **Figure 8b**) thus depends on the "off" duration. It lowers the effective driver voltage for the following switching-on event, resulting in a slight dependence of switching dynamics on frequency and duty cycle. However, in most applications the impact of this effect is negligible.
Another situation requires attention, too. If there is by any reason a longer period with both switches of a half-bridge in "off"-state (e.g. during system start-up, burst mode operation etc.), both capacitors C_C will be discharged. That

means, for the first switching pulse after such an extended non-switching period no negative voltage is available. To avoid instabilities due to spurious turn-on effects in such a situation, C_C should be chosen to guarantee sufficient negative gate voltage during device turn-off.

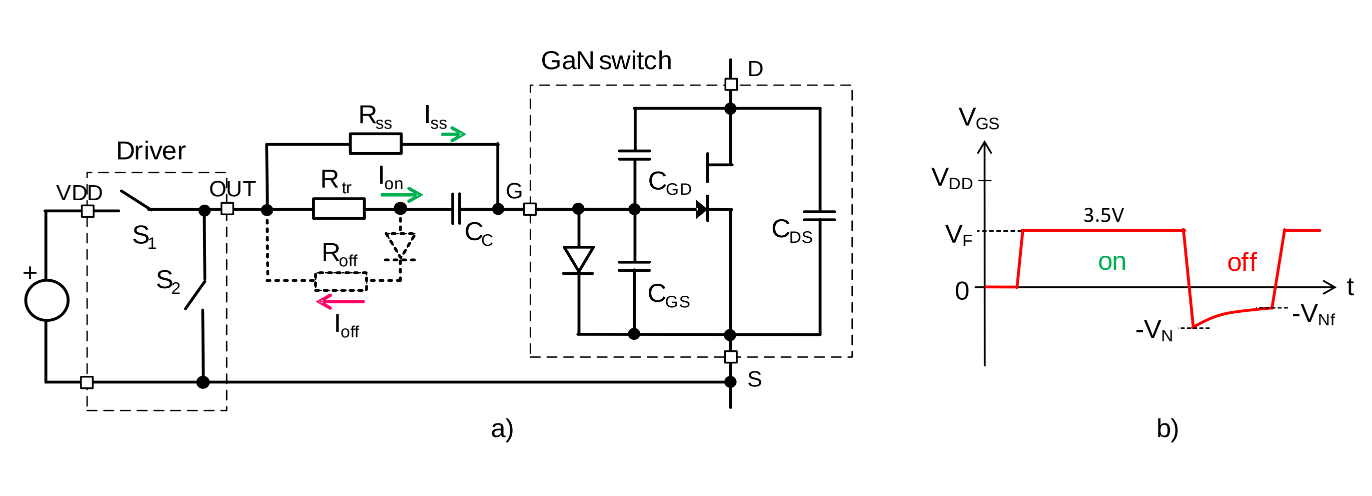


Figure 8 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

In the topology of **Figure 8** often a single resistor R_{tr} can be used for setting the maximum transient charging and discharging current. If this is not acceptable by any reason, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize independent gate impedances for the "on" and "off" transient, respectively.
All relevant driving parameters are easily programmable by choosing V_{DD}, R_{ss}, R_{tr}, R_{off} and C_C according to the relations

$$V_N = \frac{C_C \cdot (V_{DD} - V_F) - Q_G}{C_C + C_{GS}}$$

$$I_{ss} = \frac{V_{DD} - V_F}{R_{ss}}, \qquad I_{on,max} \sim \frac{V_{DD} - V_{Nf}}{R_{tr}}, \qquad I_{off,max} \sim \frac{(V_{th} + V_N) \cdot (R_{off} + R_{tr})}{R_{off} \cdot R_{tr}} \tag{3}$$

The main guidelines for dimensioning gate drive parameters are as follows:

- V_N must always be positive; a target value of 2 V in soft-switching and 4 V to 5 V in hard-switching systems is recommended.
- A target value of I_{ss} is around few mA, a higher I_{ss} current normally comes with a higher drain-source saturation current. R_{ss} has to be chosen according to the desired output characteristics.
- R_{tr} sets the transient speed for a hard switching "on" event. For soft switching systems R_{tr} is anyway uncritical.
- If a separate R_{off} is used, it should guarantee sufficient damping of oscillations in the gate loop.

For more information regarding how to drive GaN HEMT refer to white paper: Gate drive configurations for GaN power transistors.

CoolGaN™ Drive HB integrates a half-bridge level shift gate driver with bootstrap diode. If there is not enough voltage for the level shifter to transmit a valid signal to the high side, high-side driver doesn't turn on. The level shifter circuit is with respect to COM (refer to Block Diagram in **Figure 3**), and the voltage from VB to COM is the supply voltage of level shifter. Under the condition of SL is negative voltage with respect to COM as shown in **Figure 9**, VB – COM is decreased.

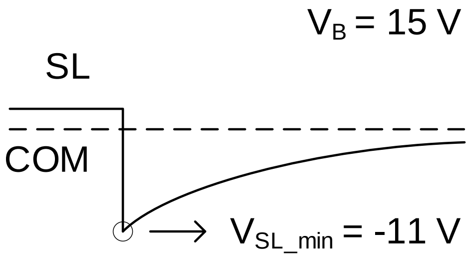
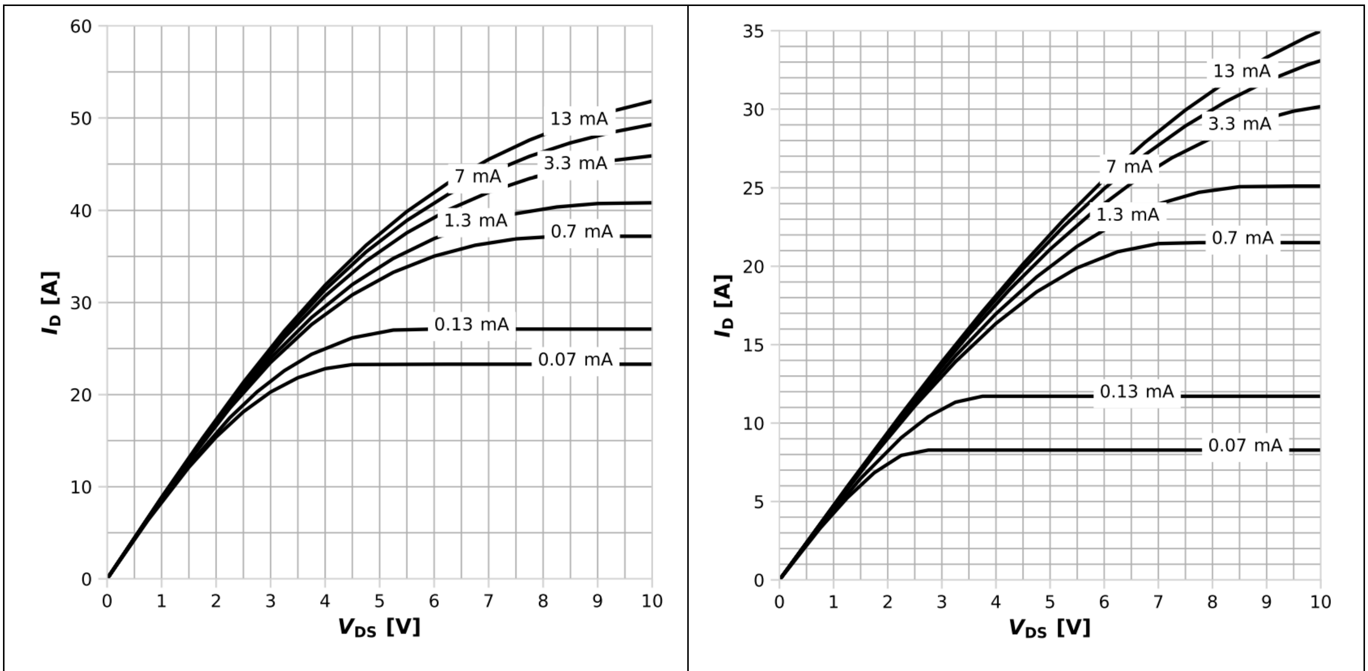


Figure 9 Headroom for HV level shifter data transmission

There is a minimum operational supply voltage of level shifter, as the voltage from VB to COM should be at least 4 V. Assuming voltage at the bootstrap capacitor V_B = 15V, voltage between SL and COM should not be lower than -11 V to guarantee INH signal pass through level shifter to OUTH. For integrated Bootstrap detailed design and Bootstrap capacitor sizing guide, please refer to 2ED2101S06F standalone gate driver datasheet.

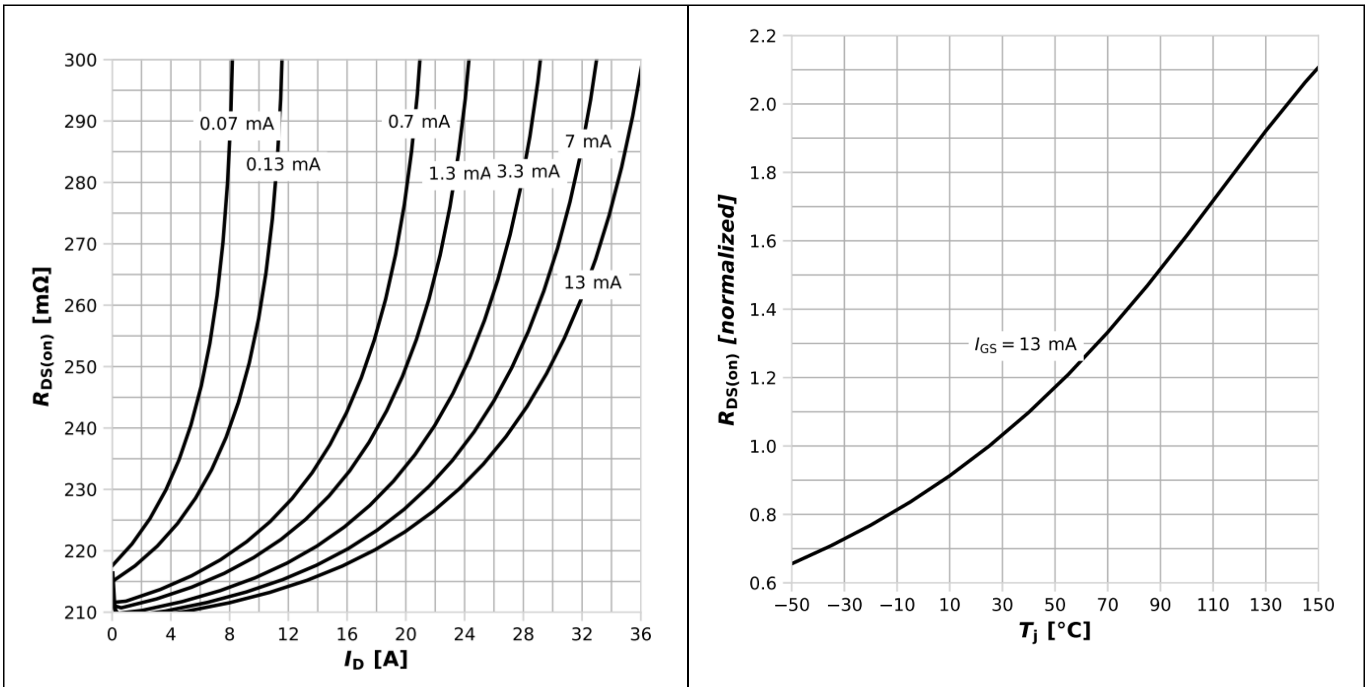
5 Typical GaN switch characteristics

The following graphs refer to a single GaN switch.



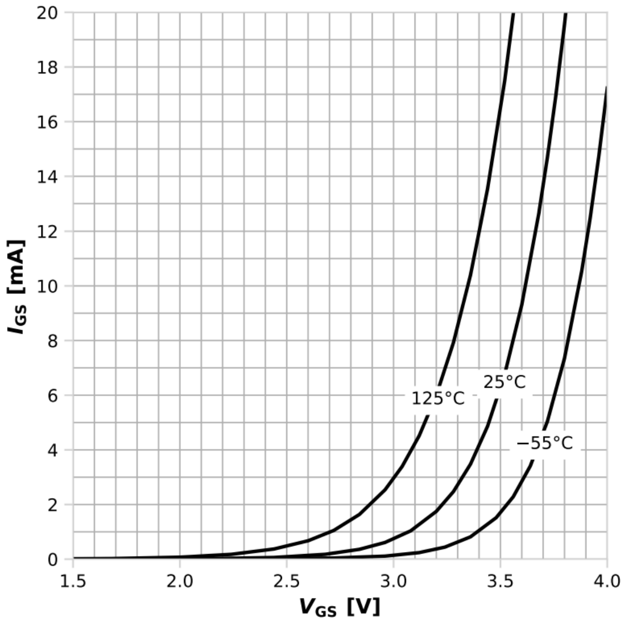
I_D=f(V_{DS},I_{GS}); T_j=25°C	I_D=f(V_{DS},I_{GS}); T_j=125°C

Figure 10 Typical output characteristics

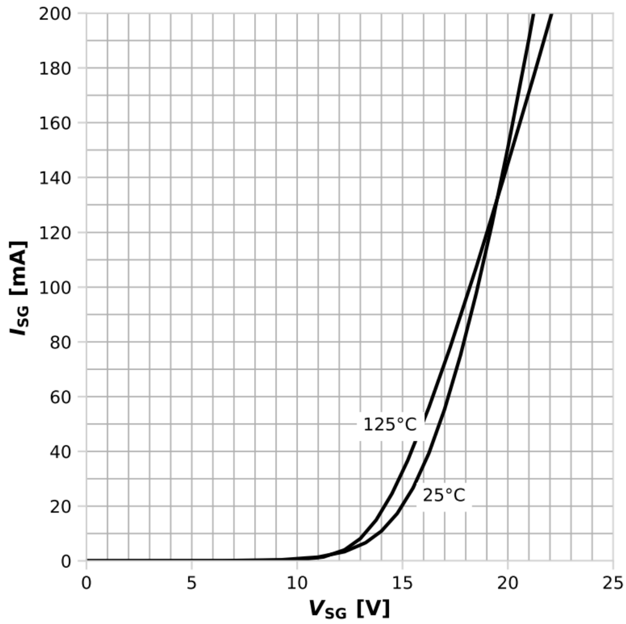


$R_{DS(on)}$=f(I_D,I_G); T_j=125°C	$R_{DS(on)}$=f(T_j); I_D=4.0 A

Figure 11 Typical drain-source on-resistance

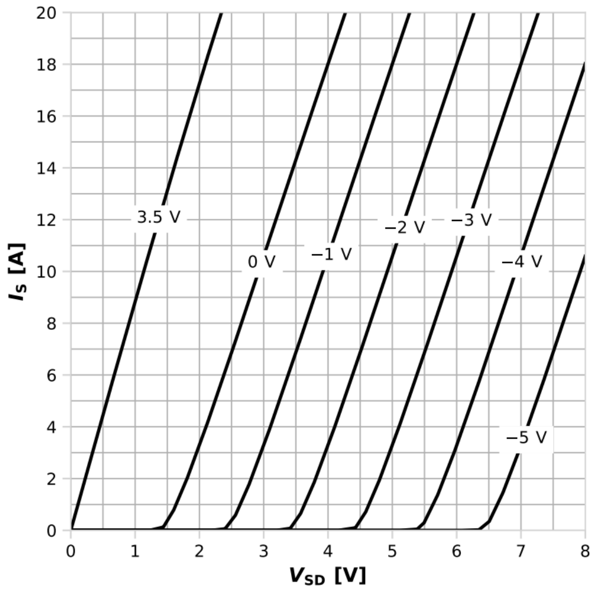


I_{GS}=f(V_{GS},T_j); open drain

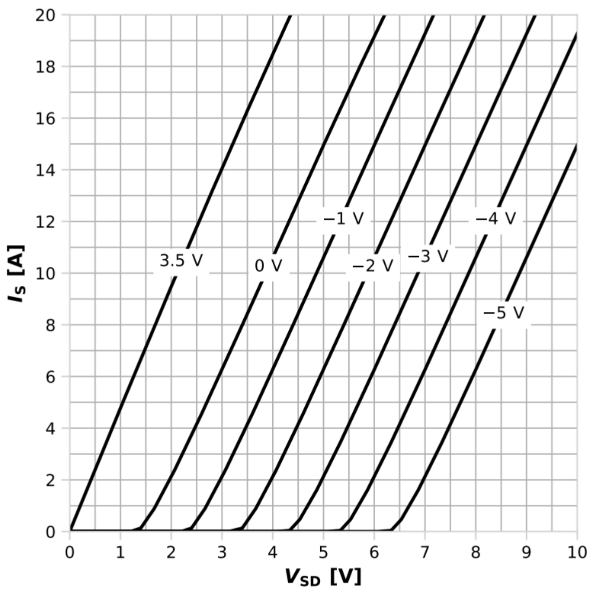


I_{SG}=f(V_{SG},T_j); open drain

Figure 12 Typical gate characteristics forward and reverse

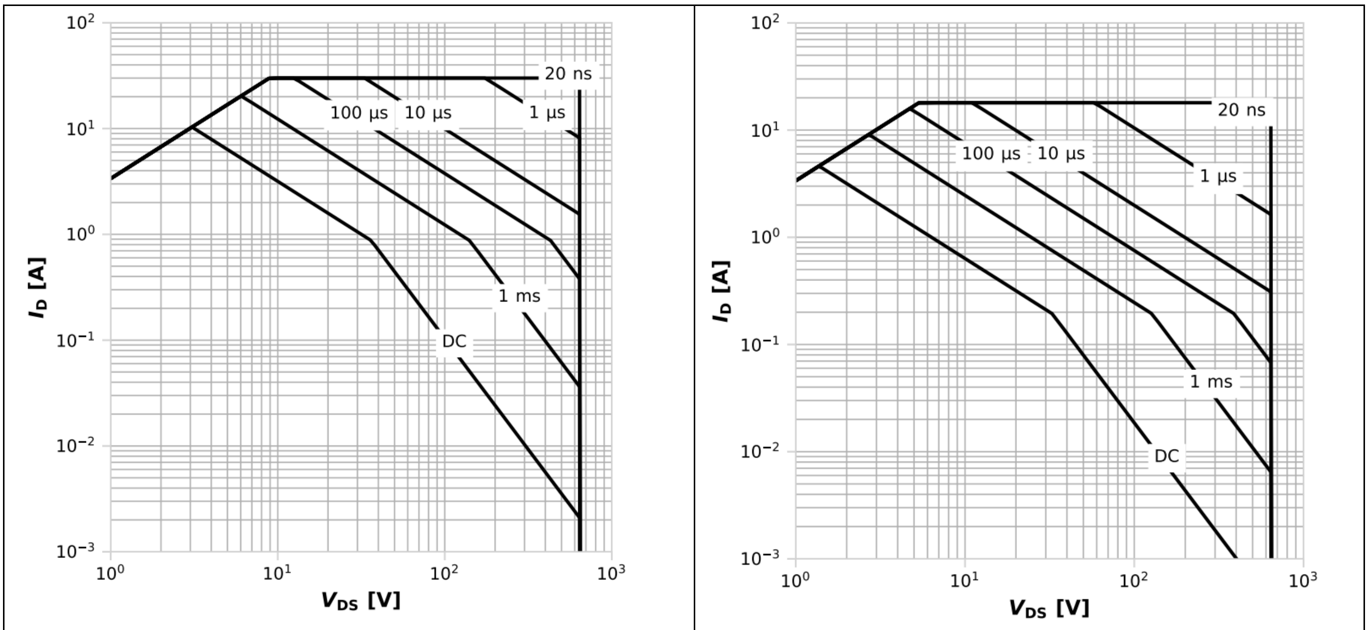


I_S=f(V_{SD},V_{GS}); T_j=25°



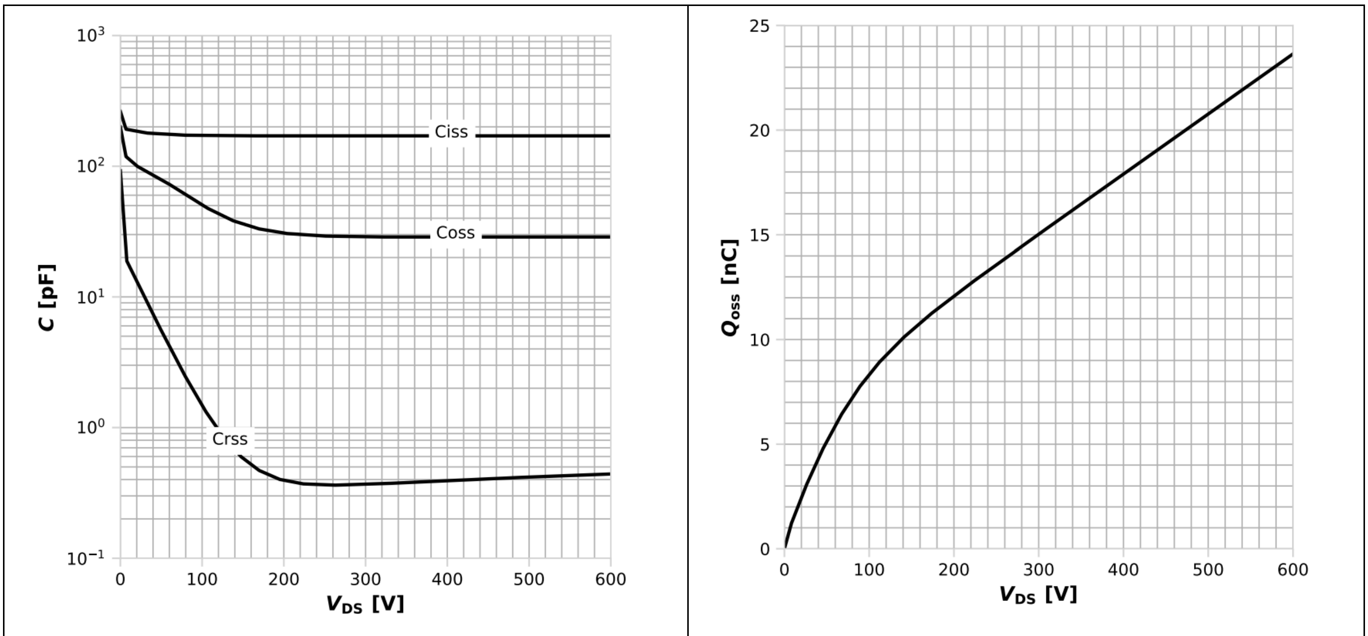
I_S=f(V_{SD},V_{GS}); T_j=125°

Figure 13 Output characteristic I_{ds} (V_{ds}) in reverse operation (parameter V_{gs})



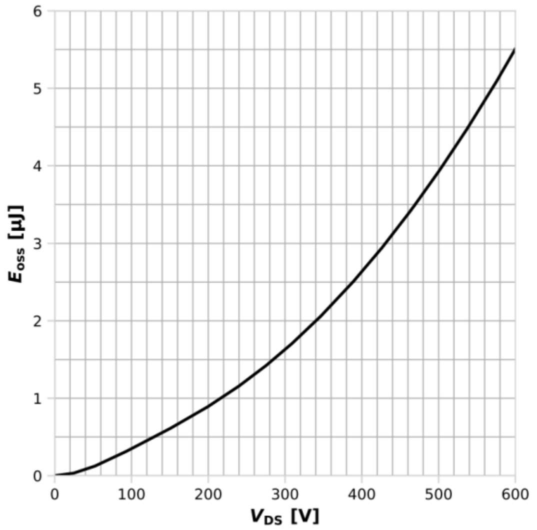
I_D=f(V_{DS}); T_{Case}=25°C	I_D=f(V_{DS}); T_{Case}=125°C

Figure 14 Safe Operating Area (SOA)



C=f(V_{DS}); V_{GS}=0 V	Q_{OSS}=f(V_{DS})

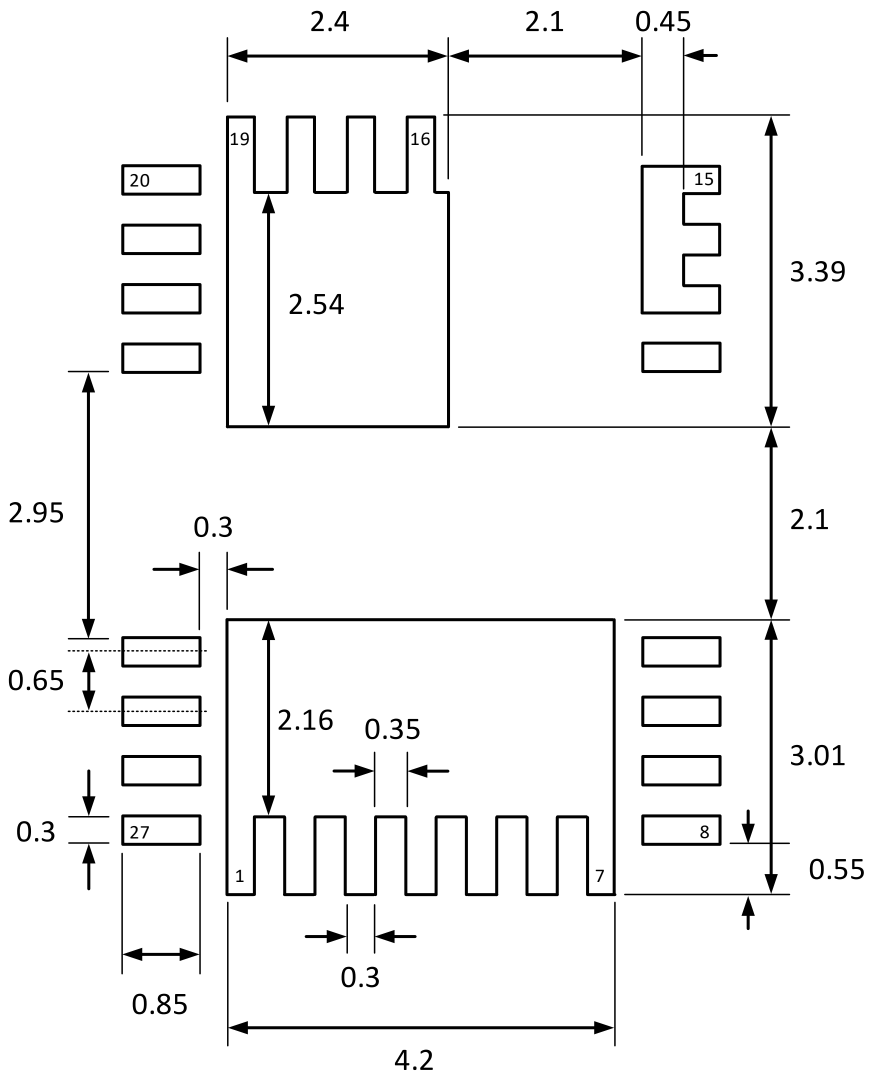
Figure 15 Terminal capacitances and output charge (single switch)



$E_{OSS}=f(V_{DS})$

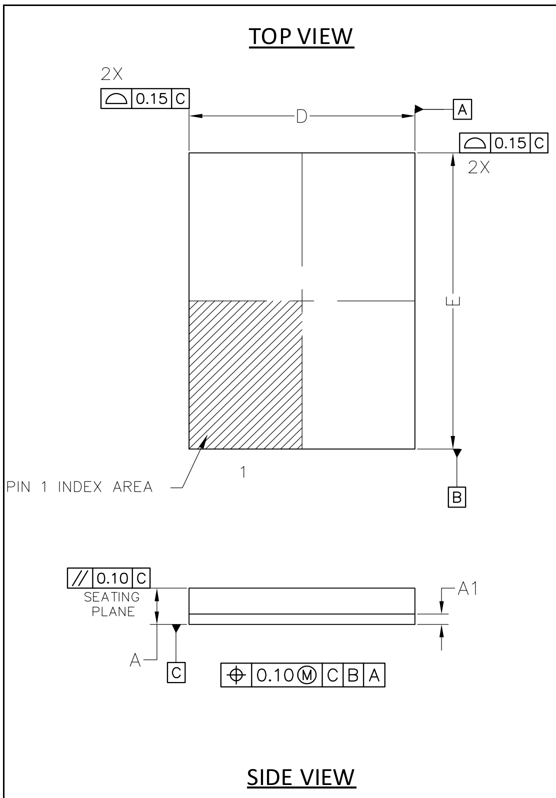
Figure 16 Typical output energy (single switch)

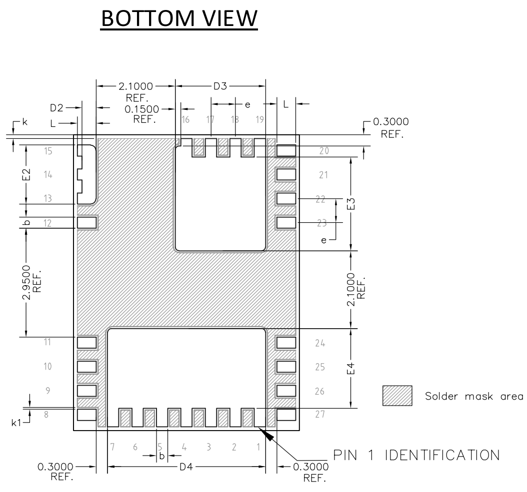
6 Package information



All dimensions are in units mm

Figure 17 TFLGA-27-2 6x8 PCB footprint





SYMBOL	DIMENSIONS MILLIMETER		
	MIN.	NOM.	MAX.
A	0.84	0.96	1.08
A1	0.26	0.28	0.32
b	0.25	0.30	0.35
D	5.90	6.00	6.10
E	7.90	8.00	8.10
D2	0.325	0.375	0.425
E2	1.55	1.60	1.65
D3	2.35	2.40	2.45
E3	2.49	2.54	2.59
D4	4.15	4.20	4.25
E4	2.11	2.16	2.21
e	0.65 BSC		
k	0.1 TYP		
L	0.45	0.50	0.55
k1	0.00	0.05	0.10

Figure 18 TFLGA-27-2 6x8 package outline

7 Appendix

- PCB footprint and Altium file for the reference PCB design can be found in the CoolGaN™ product page
- Related Links
    - IFX CoolGaN^{TM} webpage: www.infineon.com/why-coolgan
    - IFX CoolGaN^{TM} reliability white paper: www.infineon.com/gan-reliability
- IFX CoolGaN^{TM} applications information:

  www.infineon.com/gan-in-server-telecom

  www.infineon.com/gan-in-wirelesscharging

  www.infineon.com/gan-in-adapter-charger

Revision history

Document version	Date of release	Description of changes
V1.0	2025-04-25	First final datasheet release

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