

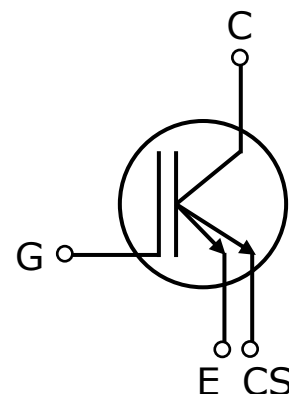
EDT2 IGBT Chip for Automotive Applications

IGBT

Quality Requirement Category: Automotive

Features

- 750V trench + field stop technology
- LOW $V_{CE(sat)}$
- Low switching losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling
- Integrated current sensor
- Double side cooling



Applications

- Drives

Description

Recommended for power modules.

Product Validation

Technology qualified for automotive applications. Ready for Validation for automotive applications according to AEC Q100/101 or LV324

Key Performance Parameters

Chip Type	V_{CE}	I_{cn}	Die Size	Package
IGC125T75E12RD2CA	750V	285A	125mm ²	Sawn on foil

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1 Parameters and Characteristics

Table 1 Mechanical Parameters

Raster size	14.530 x 8.600	mm ²
Area total	125	
Emitter pad size	See chip drawing	
Gate pad size	1.100 x 1.100	
Silicon thickness	70	μm
Wafer size	300	mm
Maximum possible chips per wafer	481	
Passivation frontside	Photoimide	
Pad metal	NiP/Pd/Au	
Backside metal	NiP/Pd/Au	
Die bond	Electrically conductive epoxy glue and soft solder	
Wire bond	Al, ≤500μm	
Reject ink dot size	Inkless	
Storage environment (<6 months)	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C

Table 2 Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	V_{CE}	750	V
DC collector current, limited by $T_{vj\text{ max}}$	I_C	- ¹	A
Pulsed collector current, t_p limited by $T_{vj\text{ max}}$ ²	$I_{C,puls}$	855	A
Gate-emitter voltage	V_{GE}	± 20	V
Junction temperature	T_{vj}	$-40 \dots +175$	$^{\circ}\text{C}$
Operating junction temperature	$T_{vj,op}$	$-40 \dots +150$ ³	$^{\circ}\text{C}$
Short circuit data ^{1/2/4} $V_{GE} \leq 15\text{V}$, $V_{CE} = 450\text{V}$, $V_{CE,max} \leq 750\text{V}$, $T_{vj} = 150^{\circ}\text{C}$	t_{sc}	4	μs
Reverse bias safe operating area (RBSOA) ²	$I_{C,max} = 570\text{A}$, $V_{CE,max} = 750\text{V}$, $25^{\circ}\text{C} \leq T_{vj,op} \leq T_{vj,op,max}$ $I_{C,max} = 570\text{A}$, $V_{CE,max} = 700\text{V}$, $-40^{\circ}\text{C} \leq T_{vj,op} < 25^{\circ}\text{C}$		

Table 3 Static Characteristics (Tested on Wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$	750	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	$V_{GE}=15\text{V}$, $I_C=85\text{A}$	-	1.0	-	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=4.0\text{mA}$, $V_{GE}=V_{CE}$	5.0	5.8	6.5	
Zero gate voltage collector current	I_{CES}	$V_{CE}=450\text{V}$, $V_{GE}=0\text{V}$	-	-	10	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0\text{V}$, $V_{GE}=20\text{V}$	-	-	600	nA
Integrated gate resistor	r_G		-	2.4	-	Ω

Table 4 Electrical Characteristics²

Parameter		Symbol	Conditions	Value			Unit
				min.	typ.	max.	
Collector-emitter saturation voltage	$T_{vj}=25^{\circ}\text{C}$	V_{CEsat}	$V_{GE}=15\text{V}$, $I_C=285\text{A}$	-	1.25	1.45	V
	$T_{vj}=125^{\circ}\text{C}$			-	1.35	-	
Input capacitance		C_{ies}	$V_{CE}=25\text{V}$, $V_{GE}=0\text{V}$, $f=100\text{kHz}$ $T_{vj}=25^{\circ}\text{C}$	-	32000	-	pF
Reverse transfer capacitance		C_{res}		-	151	-	
Current sense layout ratio (A_L/A_{CS}) of integrated current mirror		k	Defined by design	-	1000	-	

¹ Depending on thermal properties of assembly.

² Not subject to production test - verified by design/characterization.

³ $T_{vj,op}=175^{\circ}\text{C}$ for 100 hours.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.

2 Further Electrical Characteristics

Note: Switching characteristics and thermal properties are dependent on module design and mounting technology and can therefore not be specified for a bare die.

4 Bare Die Product Specifics

Note: Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Description

- AQL 0.1 for visual inspection according to “Failure Catalogue For Bare Die Delivery”
- Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision history

Revision	Description of change
V1.0	Initial Datasheet.
V1.01	Condition of chip capacitances is changed from $f = 1\text{MHz}$ to 100kHz . The C_{res} value is modified with measurement result at $f = 100\text{kHz}$.

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