

How Long is Your System Going to Last?

A Discrete IGBT Reliability Study Based on Power-Cycling Tests

High quality and reliability are among the key aspects in the design of a power semiconductor. The influence of these parameters is evident, since they not only affect the lifetime and location of the application, but also the reliable operation under maximum-power and high-load current levels.

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To evaluate the performance of advanced chip, bonding and packaging technologies, the power-cycling test is a good practice. Models for power semiconductors were introduced in the late 1990s, which could predict the lifetime of the product, however, the focus of such tests was on power modules. In the last few years, applications for discrete packaged IGBTs have increased. Such applications as UPS (Uninterruptible Power Supplies), solar inverters, low-power industrial drives, induction cooking and EV chargers have emerged, where designers require more information on the reliability and lifetime of their power system.

In this article, we would like to present our method for power-cycling tests and the results thereof for transfer-molded discrete IGBTs from Infineon Technologies. The evaluation was done in close collaboration with the Chemnitz University of Technology. Details of the power-cycling test setup and procedure at the Chemnitz University can be found in Ref. [1].

For the test runs, a set of eleven devices from Infineon's broad spectrum of 1200 V, 650 V and 600 V IGBTs in TO247 packages were chosen to cover all identified aspects that could influence the power-cycling capability. The main aspects included the IGBT voltage class and the nominal device current (Figure 1). These parameters have a direct relation to the device area via static power losses, and to the bonding scheme via specified device current. In all runs, the bill of material for the TO247 package remained unchanged. All devices under test were assembled with the same mold compound and the same bond-wire diameter.

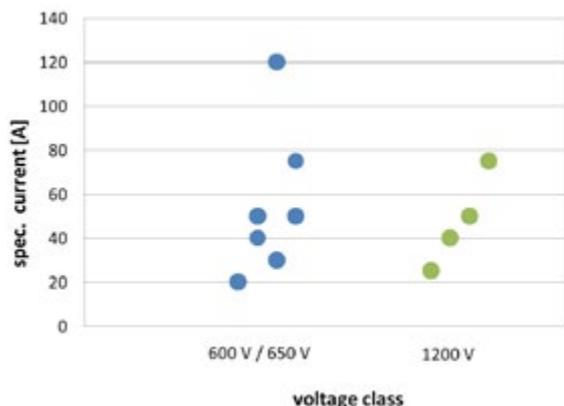


Figure 1: Nominal device current for the chosen devices grouped by voltage class

The aim of this first run was to identify the main contributors to the power-cycling capability besides the Coffin-Manson law, and temperature dependence as described in Ref. [2]. Therefore, the tests were performed under similar conditions, a temperature swing of $\Delta T_j \sim 90^\circ\text{C}$, a mean junction temperature $T_{j,m} \sim 105^\circ\text{C}$, and load pulse on duration $t_{on} = 2$ s and load pulse off duration $t_{off} = 4$ s. This parameter set covers the standard applications for these IGBT families, and has the advantage of performing the tests close to the specified device current.

The chip temperature was measured via the $V_{ce}(T)$ method. Based on the test concept, the maximal junction temperature cannot be measured directly at switch-off; for a reliable measurement, the delay was set at 500 μs . The finite element simulation (FEM) shows that the devices used in this test runs cool down for about 1.1°C in 500 μs at a power loss of 1 W/mm^2 per active area as shown in Figure 2.

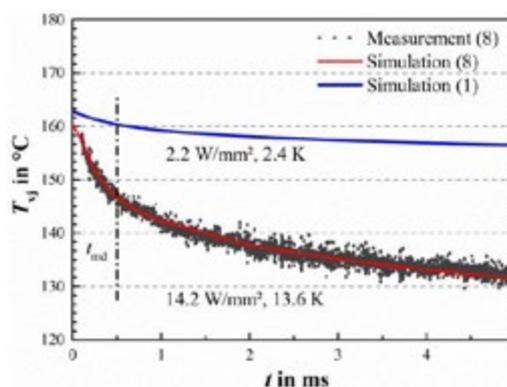


Figure 2: FEM simulation of temperature progression after pulse switch-off; simulation matches very well with measurements as shown for DUT8

For data evaluation, the measured junction temperatures were corrected accordingly, and then in a second step, normalized to the same test conditions $\Delta T_j = 90^\circ\text{C}$ and $T_{j,mean} = 105^\circ\text{C}$. This was done using a Coffin-Manson exponent of $\alpha = -3.56$ and an activation energy $E_a = 0.168 \text{ eV}$. The Coffin-Manson exponent and the activation energy were determined in a second run of experiments using a device with single-bond wire and single-bond foot. Details of the parameter extraction are described in Ref. [3]. To analyze the end-of-life failure mode, all parts were examined via a scanning acoustic microscope (SAM).

No degradation of the solder chip interface was found, however, a strong degradation of the interface between the bond foot and the IGBT chip surface was discovered, as shown in Figure 3. The non-

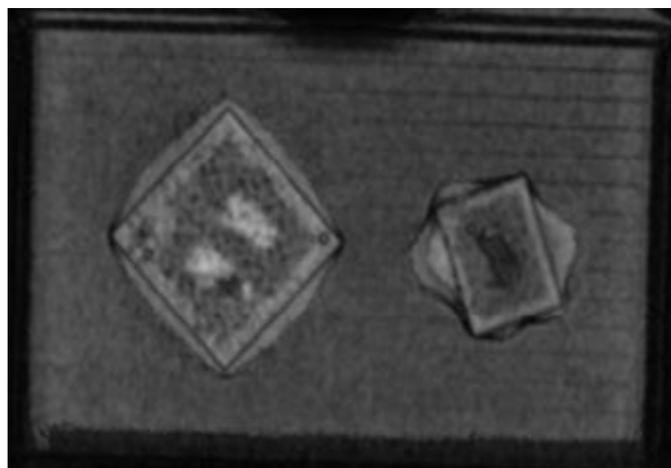


Figure 3: SAM picture of chip, front side: Non-disturbed bond wire foot remains black for the diode; the complete bright area for the upper IGBT bond wire foot indicates bond wire lift-off. This is in confirmed after removal of the mold compound (decap), Figure 4

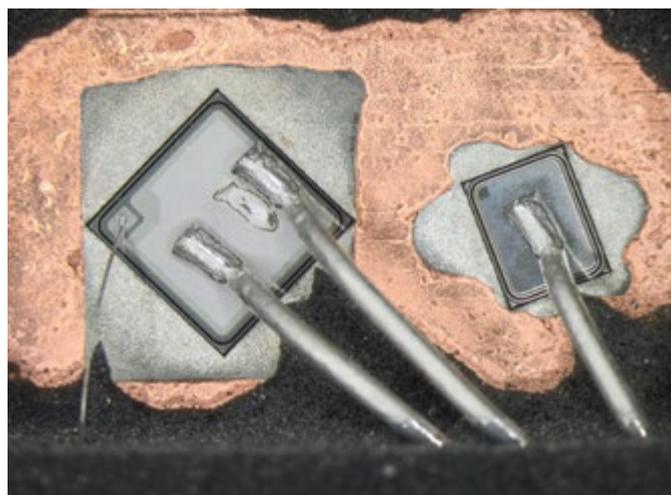


Figure 4: IGBT with upper lifted bond foot after decap, SAM showed complete bright area for this bond foot

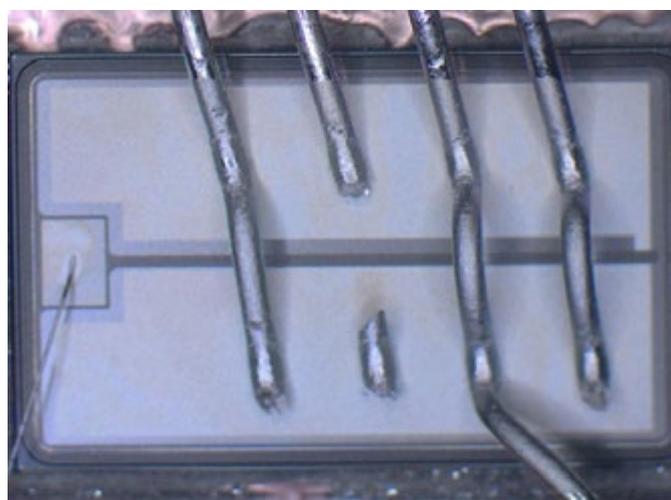


Figure 5: Heel crack of bond wires after power-cycling

stressed bond foot of the diode remains dark (chip on the right); the stressed bond foot of the IGBT becomes bright. Furthermore, some end-of-life (EOL) stressed devices were opened to inspect the bond wire. For complete bright contact areas seen in the SAM, bond lift-off as end-of-life failure mode could be confirmed (Figure 4); for SAM pictures with remaining dark areas, bond-wire heel cracks were observed (Figure 5).

For devices that failed mainly due to heel cracks, we observed an EOL dependency from the load current per bond. This is not yet conclusive for devices that failed mainly due to lifted bonds. Here additional data are required, see Figure 6. In addition, the heel-crack fail mode typically achieves higher EOL cycle numbers than the lifted-bond fail mode. The same results can be concluded for the EOL cycle dependency from the current density. There is no clear dependency of EOL cycles for devices that failed mainly with bond lift-off, but a dependency can be seen for devices showing mainly heel cracks.

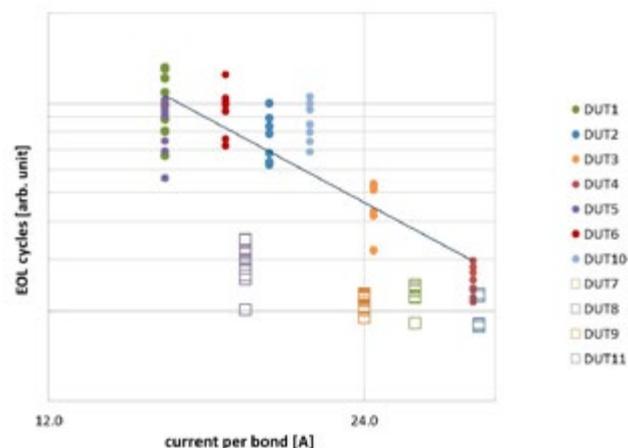


Figure 6: EOL cycles for the tested devices depending on current per bond. The measured cycles were normalized to $T_{jmean} = 105^{\circ}C$, $\Delta T = 90^{\circ}C$. Points indicate devices with heel crack as EOL fail mode, open squares indicate DUTs with bond lift-off as EOL fail mode

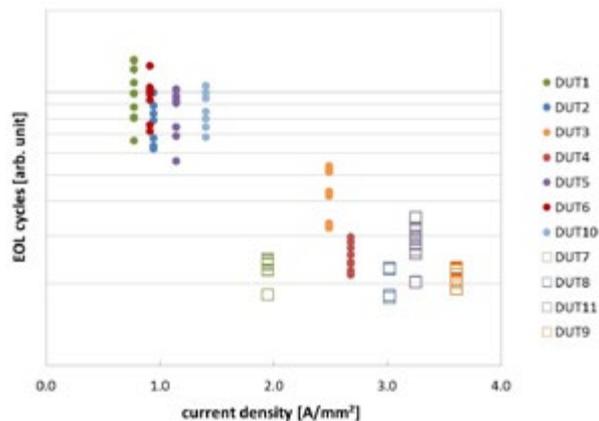


Figure 7: EOL cycles for the tested devices depending on current density

At comparable power densities, 600 V / 650 V IGBTs achieve higher current densities than 1200 V IGBTs (Figure 8) caused by the higher V_{ce} saturation voltage for these IGBTs. Our data show that testing in the higher current density regime tends to promote wire lift off as failure mechanism that limits cycle number before heel crack may set in. A model to understand this correlation has still to be developed.

To provide a power cycle curve for Infineon's 600 V / 650 V IGBTs, all groups with bond lift-off, marked in Figures 5 and 6 as squares, were taken into account, and no corrections for e.g. current density or current per bond wire were made. Figure 7 shows the corresponding accumulated Weibull distribution of the achieved cycles. The overall linear behavior indicates that no additional parameter influences the power cycle capability. Using the data from the linear fit, we can deduce the power cycle diagram for Infineon's 600 V / 650 V IGBT devices in TO247, as shown in Figure 10. Depending on the temperature swing, three different EOL percentage curves for a $T_{jmean} = 80^{\circ}\text{C}$ temperature are plotted. They are valid for pulse durations of < 10 s. For much longer pulse times, it is expected that the EOL cycle number will be limited to solder fatigue of the chip backside solder, but this was not proven in the study.

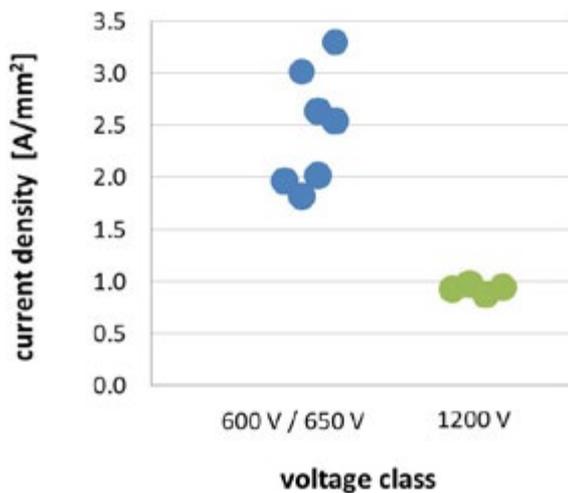


Figure 8: Current per device area, current density, grouped by voltage class

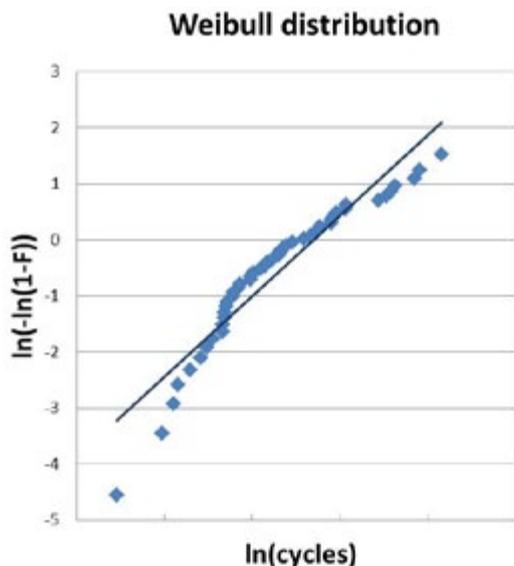


Figure 9: Achieved power cycles for DUT 7, 8, 9 and 11

In this work two series of power cycling tests were performed on eleven different device types in TO-247 package and more than 110 devices were tested until end of life. The devices have failed during the power cycling tests with bond wire failure. In the first test series the load current per bond or load current density was found to have a great impact on the power cycling capability of TO-247 package. In the second test series the dependency of lifetime on junction temperature swing ΔT_j and mean junction temperature T_{jm} was investigated and the deduced model for Infineon's 600 V / 650 V IGBT in TO247 is available on request to provide users with the power-cycling capability for different application conditions. A similar model for Infineon's 1200 V devices in TO247 will follow soon.

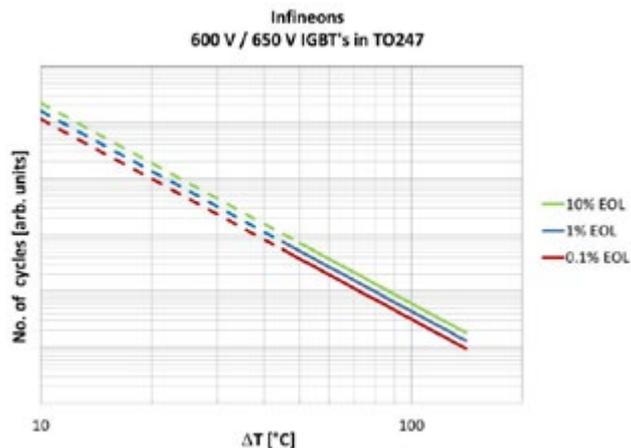


Figure 10: Achievable power cycles per ΔT for 10%, 1% and 0.1% EOL. Curves are valid for pulse durations < 10 s and $T_{jmean} = 80^{\circ}\text{C}$. Dashed lines indicate data extrapolation; solid lines are based on measured data.

Acknowledgement:

The authors gratefully thank Oliver Wenzel and Prof. Josef Lutz from Technical University of Chemnitz for their support and discussions during the experiments, and further Karina Rött and Herbert Hopfgartner from Infineon Technologies for their support in organizing and running the project.

Reference

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