The Physical Layer in the CAN FD World

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Abstract

In automotive and industrial applications the CAN protocol is very well established. But in this applications more and more data will be used and the limitation of the classical CAN network with 1 Mbit/s was not sufficient to cover the future needs. With bit rates up to 5 Mbit/s, the improvement of CAN called CAN FD is now available to increase the average data rate significant. An update of the physical layer requirements for this high bit rates was necessary and all new for CAN FD relevant parameters are described in this article.

Content

1 Motivation

For CAN physical layer the ISO specifications 11898-2/5/6 are relevant. These three specifications are now merged into one specification ISO11898-2 (ed. 2016), which will be released mid to end of 2016. In these updated specification additional dynamic parameters for CAN FD and higher bit rates are added and a lot of existing parameters are modified and adjusted for future needs. The dynamic parameters, relevant for CAN FD, will be discussed in this article.

2 General

During arbitration phase, when two or more nodes are in competition to win the arbitration, the maximum bitrate is limited by

- Network propagation delays
- Transceiver propagation delays
- And reflection.

After the arbitration phase, the propagation delay between nodes is not important anymore, but the bit width variations, caused by the network behavior and the transceiver performance, are now relevant. What are the reasons for bit width variations? Which parts of the network determine the bit width variation? The most critical parts are:

- The interface between micro-controller and transceiver
- The transceiver
- The network (reflection, damping)
-

The transceiver has three different kinds of propagation delays

- Loop delay TxD to RxD
- Transceiver Tx (Transmitter) delay
- Transceiver Rx (Receiver) delay.

The symmetry requirements of these delays are now added in the ISO 11898-2 and will be described in the next chapters.

At the moment for CAN FD communication two bit rates in the data phase are in discussion. 2Mbit/s and 5Mbit/s. The ISO 11898-2 (ed2016) specifies for this two bit rates the dynamic symmetry requirements. Normally, the symmetry of the transceiver is independent from data bit rates. A 5 Mbit/s transceiver can also be used for lower bit rates like 2 Mbit/s or 500kBit/s. The min bit rate is limited by the permanent TxD dominant time out feature. This feature is implemented to block the bus communication in case the TxD pin of a transceiver is permanently clamped to ground. With the ISO parameter for this feature a minimum bit rate of 50kBit/s can be realized.

2.1 Loop delay symmetry

The loop delay is the delay between the TxD input signal and the RxD output signal of a transmitting transceiver. Figure 1 illustrates the Transceiver loop delay. In the existing ISO 11898-5 this propagation

delay is specified with max 255ns. In the new ISO 11898-2 the condition, how to test and to guarantee is now added and the maximum allowed delay is unchanged.

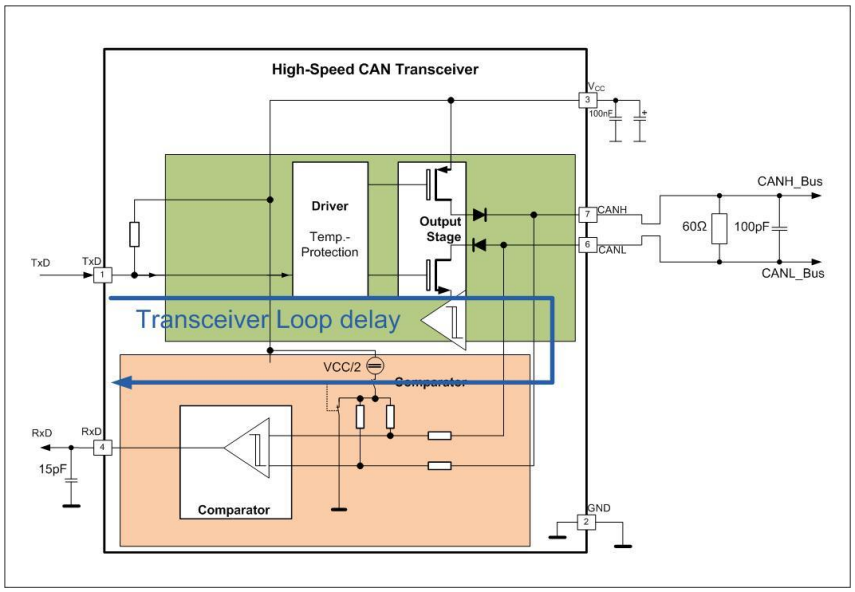

Figure 1: Transceiver Loop delay

Figure 2 illustrates, how the loop delay is specified. The delay of the recessive to dominant transition (falling edge in TxD) starts at 30% of the TxD voltage swing and stops at 30% of the RxD output level.

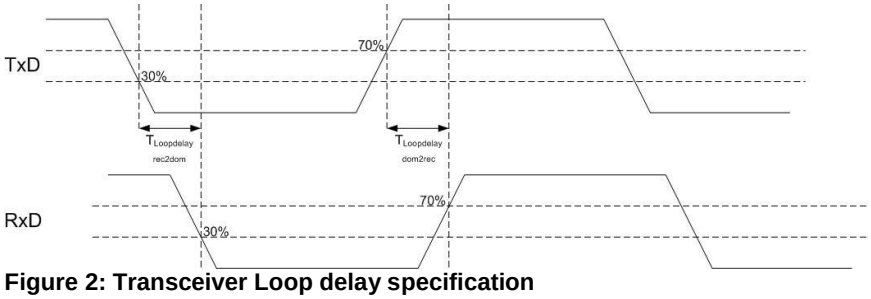

Figure 2: Transceiver Loop delay specification

The dominant to recessive transition (rising edge) starts at 70% of the TxD level and stops at 70% of its RxD level. The loop delay is an important parameter for a transmitting note. The transceiver loop delay is part of the transmitter delay which can be compensated in the transmitter delay compensation unit (TDC) in the CAN controller. In Figure 3 the difference between Transmitter and Transceiver loop delay is

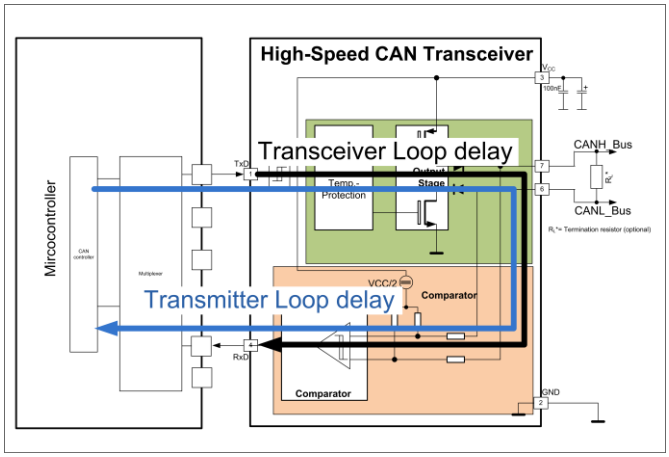

Figure 3: Difference between Transmitter and Transceiver Loop delay

demonstrated. The Transmitter loop delay starts at the output of the CAN controller as a part of the microcontroller and ends on the receiver input of the CAN controller. For high bit rates the nominal bit time may be shorter than the propagation delay. The Transmitter compensation delay unit (TDC) in the CAN FD controller compensates the transmitter delay. For high bit rates a high resolution of this unit is recommended. The symmetry of the recessive to dominant and dominant to recessive transition is very important for the transmitting node and may be different. To check this dynamic performance of the transceiver, the recessive bit width on the RXD pin ($t_{Bit(RXD)}$) after five consecutive dominant bits (see Figure 4) is defined in the ISO 11898-2 specification. In Table 1 the RxD recessive bit width specification

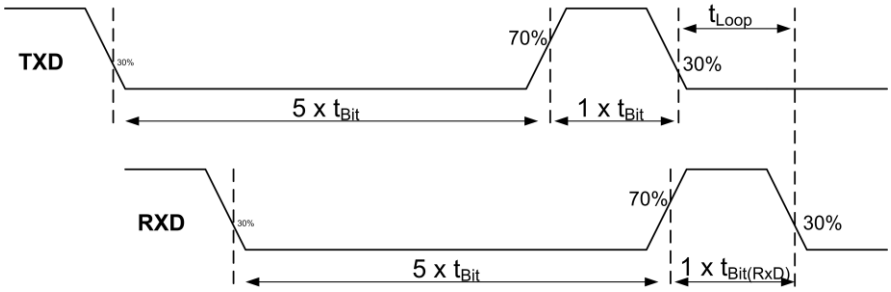

Figure 4: Transceiver Loop delay symmetry specification

Table 1: The RxD recessive bit width (Transceiver Loop Delay symmetry)

Bit rate Data phase	$t_{Bit(RxD)}$ min	$t_{Bit(RxD)}$ max	$t_{Bit(RxD)}$ normal	$t_{(loop)}$	Bus load	Load on RxD
2 Mbit/s	400 ns	550 ns	500 ns	<255 ns	60 Ω ‖ 100pF	15 pF
5 Mbit/s	120 ns	220 ns	200 ns	<255 ns	60 Ω ‖ 100pF	15 pF

is shown. Depends on the asymmetry, the recessive bit width will be shortened or extended. The limits of this parameter are asymmetric to the nominal bit rate. In Figure 5 the impact on recessive bit width is demonstrated. The recessive signal has a wide range of variation and the sample point should be set as late as possible.

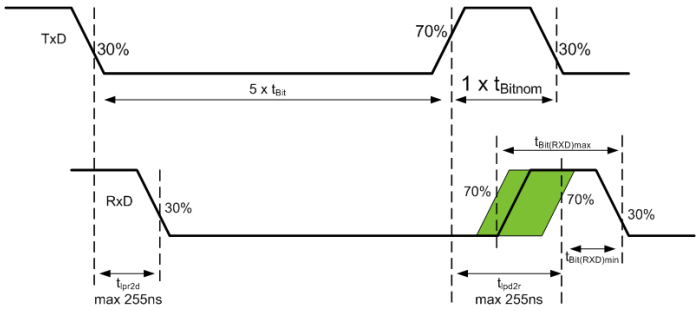

Figure 5: Variation on RxD recessive bit length

The max propagation delay TxD to RxD for both edges is below 255ns.
In general, the asymmetric behavior is caused by

- the busload (resistive and capacitive)
- the maximum differential voltage of the dominant bit
- the temperature dependency of the transceiver internal delays.

2.2 Transceiver Tx delay symmetry

The Transceiver Tx delay is the delay between the TxD input signal and the differential bus output

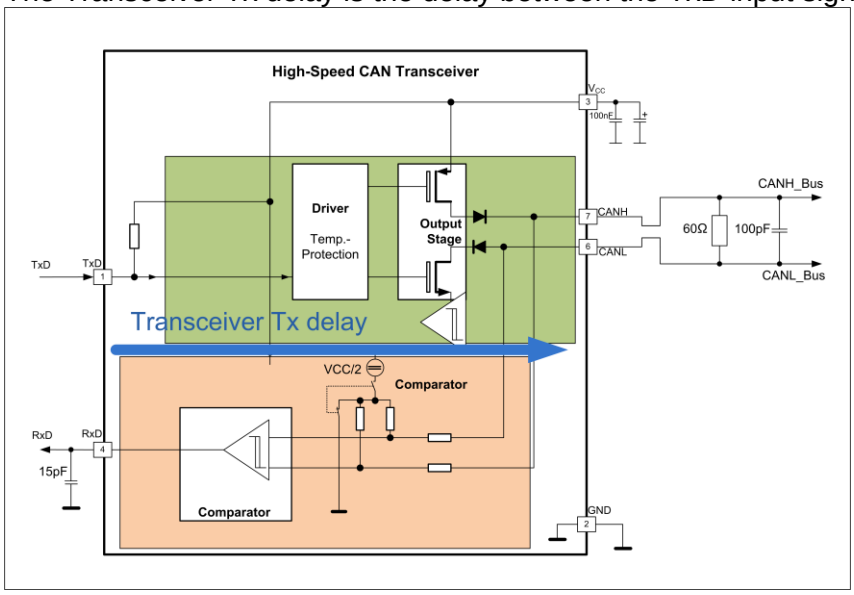

Figure 6: Transceiver Tx delay

signal (see Figure 6). The symmetry is the difference between the recessive to dominant delay and the dominant to recessive delay. The symmetry is specified like for the Loop delay. The recessive bit length is the distance between 500mV of the falling edge to 900mV of the rising edge.(see Figure 7). In Table 2

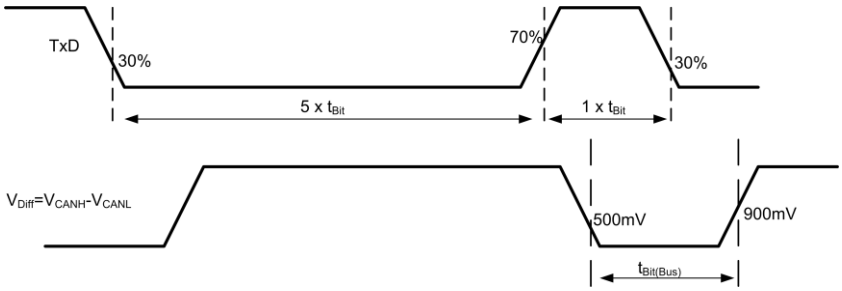

Figure 7: Specification of recessive bit width on the bus

the new ISO parameter for $t_{Bit(Bus)}$ are shown. The variation of the symmetry is smaller like for the Loop delay ($t_{Bit(RxD)}$). This parameter are valid for the defined bus load R_L=60 Ohms and a bus load representative capacitor C_L=100pF. For higher bus load the variation may be different.

Table 2: The Bus recessive bit width (Transmitter Loop Delay symmetry)

Bit rate Data phase	$t_{Bit(Bus)}$ min	$t_{Bit(Bus)}$ max	$t_{Bit(Bus)}$ normal	Bus load
2 Mbit/s	435 ns	530 ns	500 ns	60 Ω ‖ 100pF
5 Mbit/s	155 ns	210 ns	200 ns	60 Ω ‖ 100pF

The impact of the recessive bus width is illustrates in Figure 8. The recessive to dominant edge is controlled by the transceiver, but the dominant to recessive edge is dominated by the bus load.

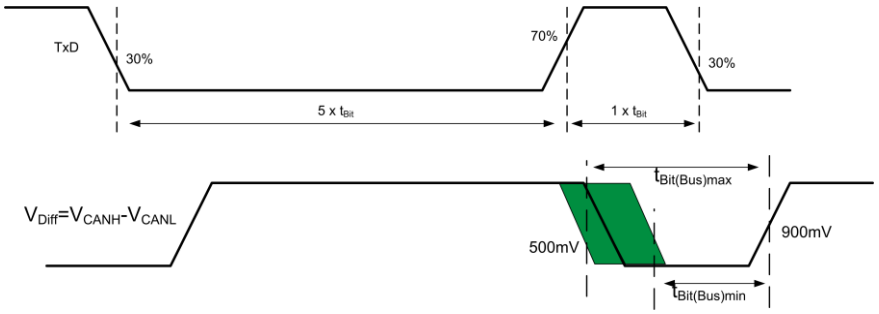

Figure 8: Variation on bus recessive bit length

One reason for the asymmetry is the internal delay from TxD Pin to the output stages. The second reason is the differential voltage level of the dominant signal. This dominant voltage level depends on

- Transmitter supply voltage (VCC)
- Physical bus load
- Transceiver temperature

To reduce the emission of transmitting signals, the slew rates are controlled and as slow as possible for high bit rates too. The voltage difference between the recessive level and the dominant differential threshold level are always 900mV ($V_{diffrec2dom}$) (see Figure 9).The slew rate defines the delay time.

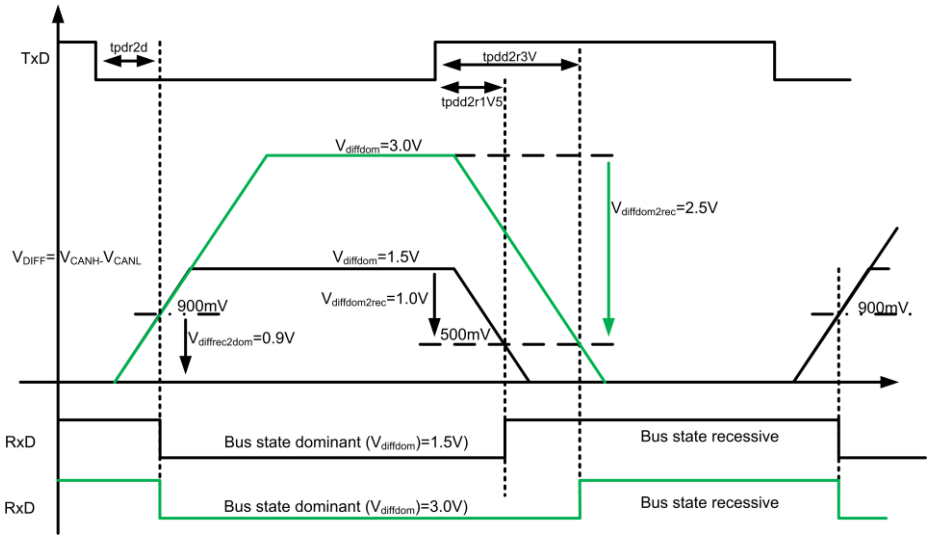

Figure 9: Impact of the dominant voltage level on the recessive bit width

The voltage difference ($V_{diffdom2rec}$) between dominant voltage level and the recessive threshold may differ from 1V (1.5V dominant level minus 500mV recessive threshold) up to 2.5V (3V dominant level minus 500mV recessive threshold). Due to the constant slew rate, the dominant to recessive delay time depends on the voltage level of the dominant signal. These two scenarios are illustrated in Figure 9. As higher the dominant voltage level on the bus as longer will be the dominant bit width or as smaller will be the receive bit width on the RxD Pin. In this scenario the impact of the bus load is ignored. To reduce the variation of the recessive bit width a small range of the Transceiver supply VCC is recommended.

2.3 Transceiver Rx delay symmetry

The Transceiver Rx delay is the propagation delay between the differential bus signal and the RxD output signal. This symmetry depends on

- production dispersion
- Temperature variation
- The Receiver thresholds
- Supply voltage variation
- Bus differential voltage Vdiff slew rate

Δt_{Rec} is a calculated value. The calculation formula is:

$$\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$$

The parameter of the RxD symmetry is also specified in the ISO 11898-2. (Table 3)

Table 3: The tolerance of the Receiver of 2 Mbit/s and 5 Mbit/s transceiver

Bit rate Data phase	$t_{Bit(Bus)}$ min	$t_{Bit(Bus)}$ max	Load on RxD
2 Mbit/s	-65 ns	40 ns	15pF
5 Mbit/s	-45 ns	15 ns	15pF

2.4 Bit timing symmetry in a Network

Figure 10 illustrates a typical communication path from a transmitting node to a receiving node in a network. The bit width will be modified by the Transmitter Tx delay, the network, the asymmetry of the

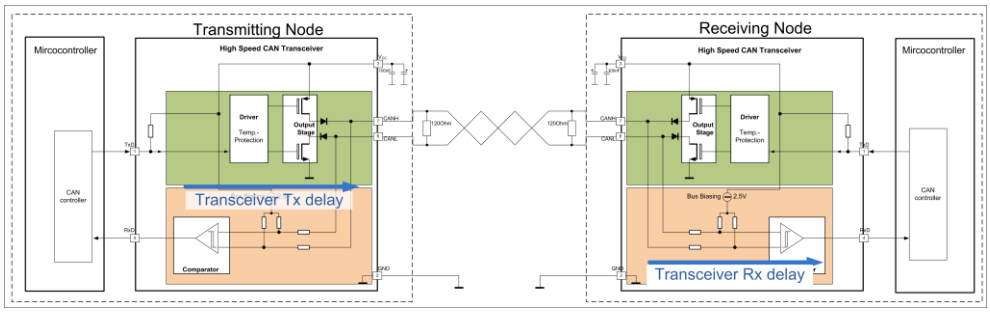

Figure 10: Typical communication path in CAN

Receiver. In a worst case scenario the variation of the RxD recessive bit time on a receiving node is the

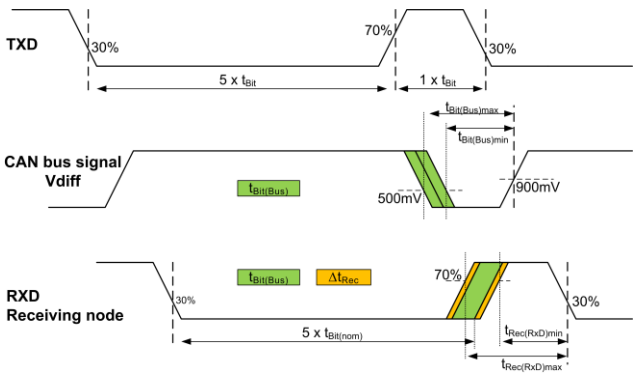

Figure 11: Illustration of the recessive bit width on a receiving node

sum of the Transceiver Tx delay symmetry and the Transceiver Rx delay symmetry (see. Figure 11). In Table 4 the possible variation of the recessive bit width on a receiving node is shown. This calculation

Table 4: Variation of the recessive bit width on a receiving RxD

Bit rate Data phase	$t_{Bit(RxDrec)}$ min	$t_{Bit(RxDrec)}$ max	$t_{Bit(Bus)}$ normal	Bus load
1 Mbit/s			1000 ns	60 Ω ‖ 100pF
2 Mbit/s	370 ns	570 ns	500 ns	60 Ω ‖ 100pF
5 Mbit/s	110 ns	225 ns	200 ns	60 Ω ‖ 100pF

is the sum of the Transceiver Tx delay symmetry and the Transceiver Rx symmetry. The impact of the network is excluded in this calculation. The rising edges may jitter. The falling edges are stable, as this is the edge on which a CAN node synchronizes and this dominant bus level is actively driven by the transmitter and therefore stable. The range marked in green is the variation of the transmitter and the range marked in yellow is the variation of the receiver. To analyze the worst case scenario, both parameters must be added. For 2Mbit/s and 5Mbit/s the calculation scenarios are described in the following chapters.

2.5 Symmetry for networks up to 2Mbit/s

For bit rates between 1Mbit/s and 2Mbit/s a transceiver specified for 2Mbit/s should be chosen. This chapter shows the possibility to calculate the jitter at the RxD pin at the receiving node, for bit rates below 2 Mbit/s. The maximum and minimum recessive bit length tRec(RxD) seen be the receiving node is calculated.

$$t_{Rec(RxD)max} = t_{nom} + (t_{Bit(Bus)max} - t_{nom(2Mbit/s)}) + \Delta t_{Recmax}$$

$$t_{Rec(RxD)min} = t_{nom} + (t_{Bit(Bus)min} - t_{nom(2Mbit/s)}) + \Delta t_{Recmin}$$

A calculation example for 1Mbit/s:

Table 5: Deviation of a 2 Mbit/s Transceiver to the nominal bit time

Parameter for 2 Mbit/s (t_{Bit}= 500ns)					
Parameter	Specification		Deviation to nominal bit time		Unit
	min	max	min	max	
Loop delay symmetry	400	550	-100	50	ns
Transceiver Tx delay symmetry	435	530	-65	30	ns
Transceiver Rx delay symmetry	-65	40	-65	40	ns

In Table 5 the deviation of the symmetry parameter to the nominal bit time is calculated. These deviations of a transceiver are bit rate independent. A transceiver has no information about bit rate and protocol. A transceiver transmits the level on the TxD pin on the bus pins up to the max specified bit rate.

Based on this experience the deviation for 1 Mbit/s with a2 Mbit/s transceiver can be calculated. The deviation is like for the 2 Mbit/s transceiver and the calculated numbers are illustrated in

Table 6: Calculated bit width variation of a 2Mbit/s transceiver used in a 1Mbit/s application

Parameter for 1 Mbit/s (t_{Bit}= 1000ns) application					
Parameter	Calculated Bit width		Deviation to nominal bit time		Unit
	min	max	min	max	
Loop delay symmetry	900	1050	-100	50	ns
Transceiver Tx delay symmetry	935	1030	-65	30	ns
Transceiver Rx delay symmetry	-65	40	-65	40	ns

2.6 Symmetry for networks up to 5Mbit/s

For bit rates up to 5Mbit/s a transceiver specified for 5Mbit/s should be chosen. This chapter shows the possibility to calculate the jitter at the RxD pin at the receiving node, for bit rates below 5 Mbit/s. The maximum and minimum recessive bit length $t_{Rec(RxD)}$ seen be the receiving node is calculated.

Maximum $t_{Rec(RxD)}$= nominal bit time + max TX delay sym. deviation + max value of $\Delta t_{Rec\ for\ 5Mbit/s}$

Minimum $t_{Rec(RxD)}$ = nominal bit time + min TX delay sym. deviation + min value of $\Delta t_{Rec\ for\ 5Mbit/s}$

These values consider only the influence of the Transceiver. Additional effects like clock tolerance and the phase shift of the network are not considered.

Table 7: Deviation of a 5 Mbit/s transceiver compared with the nominal bit time

Parameter for 5 Mbit/s (t_{Bit}= 200ns)					
Parameter	Specification		Deviation to nominal bit time		Unit
	min	max	min	max	
Loop delay symmetry	120	220	-80	20	ns
Transceiver Tx delay symmetry	155	210	-45	10	ns
Transceiver Rx delay symmetry	-45	15	-45	15	ns

In Table 7 the deviation of the symmetry parameter to the nominal bit time is calculated. These deviations are bit rate independent. A transceiver has no information about bit rate and protocol. A transceiver transmits the level on the TxD pin on the bus pins up to the max specified bit rate. Based on this experience the deviation for 4 Mbit/s with a 5 Mbit/s transceiver can be calculated. The calculated deviation for 4 Mbit/s are shown in Table 8.

Table 8: Calculated bit width variation of a 5 Mbit/s transceiver used in a 4 Mbit/s application

Calculated parameter for a 4 Mbit/s application					
Parameter	Calculated Bit width		Deviation to nominal bit time		Unit
	min	max	min	max	
Loop delay symmetry	170	270	-80	20	ns
Transceiver Tx delay symmetry	205	260	-45	10	ns
Transceiver Rx delay symmetry	-45	15	-45	15	ns

In a real network a lot of ringing is available at the end of a dominant to recessive transition. This cause a reduction of the recessive bit time or tailores a network. Using a 5 Mbit/s transceiver in a 2Mbit/s application gives a little more margin for the network. In Table 9 the calculated numbers of the variation of a 5Mbit/s transceiver in a 2Mbit/s application. As you can see, the spread is smaller and especially the recessive bit width variance on the RxD Pin of a receiving node is much smaller compared with 2 Mbit/s transceiver in The same network (see Table 10). The

Table 9: Calculated bit width variation of a 5 Mbit/s transceiver used in a 2 Mbit/s application

Calculated parameter for a 2 Mbit/s application					
Parameter	Calculated Bit width		Deviation to nominal bit time		Unit
	min	max	min	max	
Loop delay symmetry	420	520	-80	20	ns
Transceiver Tx delay symmetry	455	510	-45	10	ns
Transceiver Rx delay symmetry	-45	15	-45	15	ns

Table 10: Comparison of the recessive bit width on a receiving node with 2Mbit/s and 5Mbit/s transceiver

Bit rate **Data phase**	$t_{Bit(RxDrec)}$ min	$t_{Bit(RxDrec)}$ max	$t_{Bit(Bus)}$ normal	**Bus load**
2 Mbit/s **With 5 Mbit/s transceiver**	410 ns	525 ns	500 ns	60 Ω ‖ 100pF
2 Mbit/s **With 2 Mbit/s transceiver**	370 ns	570 ns	500 ns	60 Ω ‖ 100pF

difference is 40 ns. This margin makes your network more reliable against noise and EMC jitter. These are all relevant transceiver parameter for the new CAN FD application. To concept a CAN Physical layer the PLL jitter, the propagation delay and the symmetry are also part of the physical layer and have to be taken into account.. The Interface between microcontroller and transceiver has to be taken into account too and will be described in the next chapter.

2.7 Interface between Microcontroller and Transceiver

The interface between microcontroller and Transceiver cannot be ignored, if higher bit rates will be used in CAN FD networks. Depends on the kind of microcontroller port which will be used for TxD and the length of the board wire, the propagation delay can be up to 50ns. Due to the high capacitive load in case of a long wire on the ECU board, the slew rates will be slow too. To get no additional asymmetry, the TxD input thresholds should be symmetric (CMOS level) to the transceiver I/O supply. A TTL level

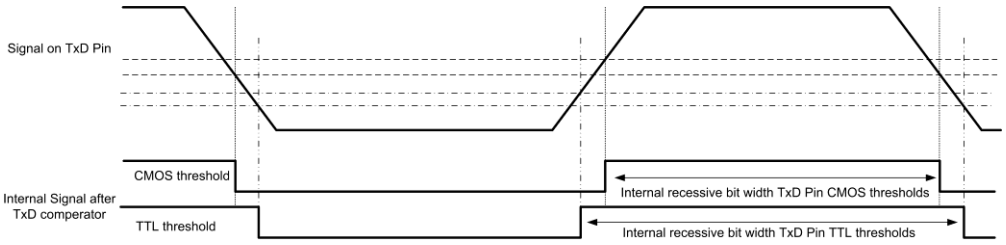

Figure 12: Transceiver internal bit width modification caused by TxD input thresholds

based TxD input threshold cause an internal modification of the bit length depends on the slew rate of the TxD input signal. Figure 12 illustrated such kind of bit width modification. Also the symmetry of the slew rates hast to be taken into account. As higher the bit rate is as more symmetric the slew rate of the microcontrollers TxD signal and the Transceiver RxD signal has to be.

3 Infineon CAN FD product overview

Infineon offers a wide portfolio of stand alone transceiver and System base chips supporting CAN FD. Additional components are in development to support 5Mbit/s too.

Table 11: CAN FD stand alone transceiver product overview

Stand alone Transceiver	Product variant	Classical CAN	CAN FD up to 2Mbit/s	CAN FD up to 5 Mbit/s
Without remote wake up (8 Pin Device)	TLE7250SJ/LE TLE7250VSJ/VLE TLE7250XSJ/XLE	Yes	Yes	No
Without remote wake up (8 Pin Device)	TLE9250SJ/LE TLE9250VSJ/VLE TLE9250XSJ/XLE	Yes	Yes	Yes
With remote wake up (8 Pin Device)	TLE7251VSJ/VLE	Yes	Yes	No
With remote wake up (8 Pin Device)	TLE9251VSJ/VLE	Yes	Yes	Yes
Industrial Transceiver with remote Wake up	IFX1051	Yes	Yes	

Table 12: System Basis chip with CAN FD and CAN partial Network product overview

System Base Chip	Product variant	Classical CAN	CAN FD up to 2Mbit/s	CAN FD up to 5Mbit/s	CAN PN + CAN FD tolerance
Mid Range SBC DCDC SBC	TLE9260QX(V33) TLE9261QX(V33) TLE9262QX(V33) TLE9263QX(V33)	Yes	Yes	No	No
	TLE9260-3QX(V33) TLE9261-3QX(V33) TLE9262-3QX(V33) TLE9263-3QX(V33)	Yes	Yes	No	Yes
DCDC SBC	TLE9271QX(V33) TLE9272QX(V33) TLE9273QX(V33) TLE9274QX(V33)	Yes	Yes	No	No
Multi-CAN Power SBC	TLE9278QX(V33)	Yes	Yes	Yes	No
	TLE9278-3QX(V33)	Yes	Yes	Yes	Yes

List of Figures

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Publications

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Part 2: High-Speed medium access unit
(edition 2016)

CiA 601-1 CAN node and system design
Part 1: Physical interface implementation (2015)
CAN in Automation (CiA) e.V.

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Infineon Technologies AG
85579 Neubiberg, Germany

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