

System Simulation & Design Creation Tool (Transformer, BOM and IC Parameters)

Single-Stage PFC Flyback Dimmable Constant-Current Controller

ICL8105

.dp digital power 2.0

About this document

Scope and purpose

This document is a guide to using the Infineon ICL8105 system simulation and design creation tool. It enables users to generate transformer, bill of materials (BOM) and IC parameter designs based on the system simulation/calculation output.

The Infineon ICL8105 is a digital controller for high-performance single-stage flyback converter, targeting LED lighting applications.

Intended audience

This document is intended for anyone wishing to evaluate the performance of the Infineon ICL8105 for their own application tests or to use it as a base/reference for a new Infineon ICL8105-based development.

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Key features

1 Key features

1.1 System simulation/calculation

Single-stage PFC Flyback is the most cost-effective topology for lighting applications which have low output power and require isolation. However, system optimization of such a topology is not so straightforward as it mostly requires trade-off with other performance factors. For instance, increasing output capacitance will reduce output current ripple but the trade-off could be a longer startup time at low dimming. Therefore, the system simulation and calculation with this tool is intended to help ICL8105 customers when creating a board design with overall-balanced performance profiles which fit best to their requirements.

Below is a list of system simulation and calculation outputs generated by the tool:

- Normalized primary average current curve simulation for iTHD optimization (see example in [Figure 1](#))
- Controller operating mode (quasi-resonant /discontinuous conduction/ continuous conduction) during non-dimmed operation
- Minimum and maximum on-times during non-dimmed operation
- Minimum and maximum switching frequencies during non-dimmed operation
- Maximum primary peak current, primary rms current, secondary rms current calculations
- Output current estimation at minimum dimming
- Maximum output current ripple estimation
- Maximum startup time estimation
- Maximum MOSFET drain voltage and output diode reverse voltage estimation
- Transformer conduction loss, core loss estimation at minimum and maximum input voltages
- Minimum and maximum value selection for passive components (capacitors & resistors)
- Maximum power loss estimation of selected values of ICL8105 CS pin resistor, ZCD pin resistors and bleeder resistor.

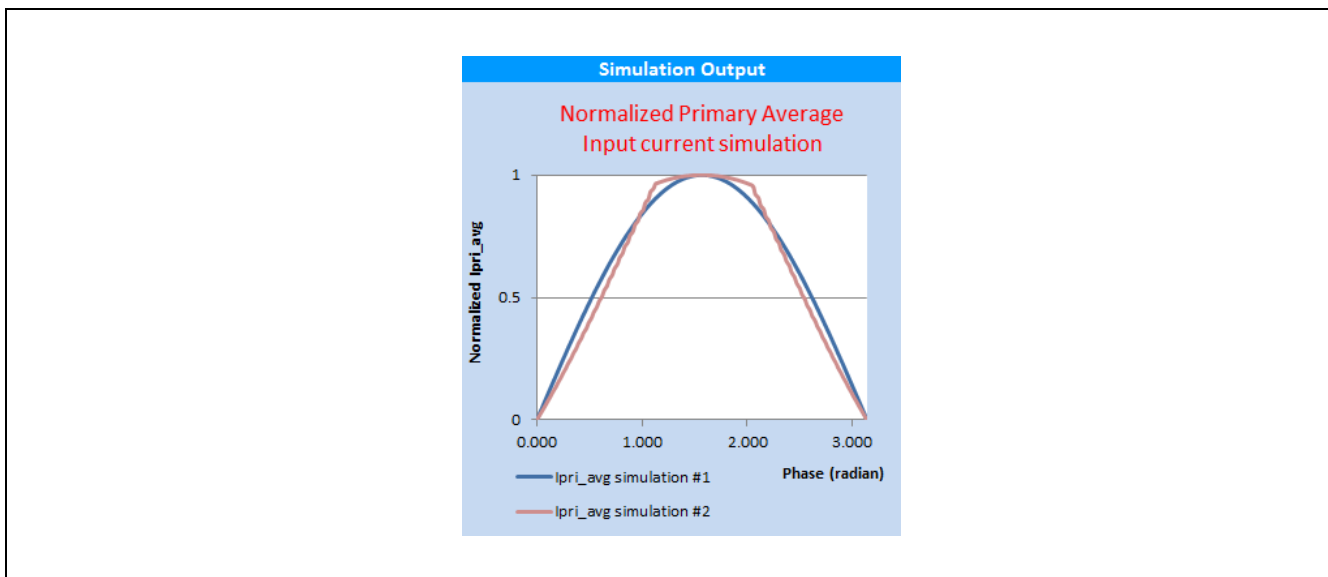


Figure 1 Example of normalized primary average current curve simulation (for iTHD optimization)

Note: iTHD refers to input current harmonics distortion.

Key features

1.2.2 Auto-generated BOM and IC parameters

The ICL8105 is a high-performance digital controller which allows custom parameterization by designers or end users. For instance, the ICL8105 allows changes to non-dimmed output current settings on the same board with no change in hardware. There are a total of 69 IC parameters which can be configured using a GUI called .dpVision.

Based on the design inputs of each step, the tool will recommend the minimum and maximum values of parameters and components dimensioning in order to guide users in the selection of appropriate values. After completing the final step with no error detected, BOM and IC parameters will be automatically generated – as shown in **Figure 3**.

Auto-generated BOM						Auto-generated IC Parameters		
Auto-Generated BOM						Auto-Generated IC Parameters		
Note: Please refer to sheet "SCH". EMI Line Filter & Bridge not included in BOM						Hardware configuration		
Schematic Section	Symbol	Value	Rating	Supplier	Part Number/Package	Parameter	Value	Unit
FB_PRI	T1	Lp: 0.544mH; Np: 58; Nr: 15; Naux: 15; Nre-aux: 15				L _{out_rot}	880.0	mA
	IC3	ICL8105	-	INFINEON	ICL8105 (DSO-8)	N _{LP}	58	turns
	Q1	IPD80R1K0CE	800V	INFINEON	IPD80R1K0CE (DPAK)	N _{LA}	15	turns
	D3	≥1A	≥800V	DIODES	RS3MB-13-F (SMB)	N _{LA}	15	turns
	D20, D21	1A	600V	FAIRCHILD	ES1J (SMA)	L _{LP}	0.544	mH
	C3	6800pF	≥567V	ANY	Discrete or SMD 1206	R _{OS}	0.22	ohm
	C4	0.22uF	≥498V	ANY	Film cap	V _{OCF1}	0.51	V
	C5	100pF	50V, COG	ANY	SMD Package: 0603	R _{ZCD_1}	56.2	kohm
	R2	20kohm	1%	ANY	SMD Package: 0603	R _{ZCD_2}	2.00	kohm
	R4+R5+R6	66kohm	1%	ANY	SMD Package: 1206 (3 per, in series)	V _{CC_SUPPLY}	Wide	
	R7+R8	174.8kohm	±5%	ANY	Power rating: ≥0.67W	C _{VCC}	33.00	uF
	R10	56.2kohm	1%	ANY	SMD Package: 1206	V _{out_caprating}	63	V
	R11	2kohm	1%	ANY	SMD Package: 0603	R _{HV}	66	kohm
	R14	0.22ohm	1%	ANY	Power rating: ≥0.11W	L _{GD_pk}	49	mA
AUX VCC SUPPLY	R16	10kohm	1%	ANY	SMD Package: 0805	Protection timer		
	Q2	NPN Transistor	V _{ceo} : 50V	INFINEON	BDP953 (SOT-223)	t _{outa_restart}	1.0	s
	D4	≥0.25A	≥237V	ANY	BAV103 (SOD-80C)	t _{outa_restart_fart}	0.4	s
	D12	0.25A	200V	ANY	BAV102 (SOD-80C)	Reaction_OVP_Vout	Auto-Restart	
	ZD1	Zener 15V	±5%	ANY	SOD-323 arrimilar	Speed_OVP_Vout	Slow	
	C6	4.7uF	≥59V	ANY	Electrolytic Cap	V _{outOV}	48.4	V
	C8	33uF	25V	ANY	E-Cap or SMD 1206	EN_UVP_Vout	Enabled	
	C38	0.1uF	≥25V	ANY	SMD Package: 0603	t _{start_max}	18.40	ms
	R17	47kohm	1%	ANY	SMD Package: 1206	EN _{laout_max_avg}	Enabled	
	R18	4.7kohm	1%	ANY	SMD Package: 1206	EN _{laout_max_peak}	Enabled	
	IC30	Schmitt trig. IC	Invert out	TI	74LVC04DBVR	L _{out_max_peak}	1980	mA
	IC100	CDM10V adapter board	-	INFINEON	CDM10V adapter board	Speed_OCF _{laout}	Slow	
	PC1	Optocoupler	≥4kV, UL	VISHAY	VO617A-2	EN_UVP _{in}	Enabled	
	Q100	NPN Transistor	V _{ceo} : 55V	INFINEON	BCX56 (SOT-89)	EN_OVP _{in}	Enabled	
	ZD30	Zener 5.1V	±2.5%	ANY	SOD323 arrimilar	V _{inOV}	329	V
DIMMING	D100	0.25A	200V	ANY	BAV102 (SOD-80C)	V _{in_{start}_max}	329	V
	D105	0.2A	30V	INFINEON	BAT54-05 (SOT-23)	V _{in_{start}_min}	72	V
	ZD100	Zener 15V	±5%	ANY	SOD-323 arrimilar	V _{inUV}	62	V
	C33	0.68uF	16V	ANY	SMD Package: 0603	Debug_Mode	Disabled	
	C34	4.7uF	25V	ANY	SMD Package: ≥0805	Temperature guard		
	C35, C36	0.1uF	25V	ANY	SMD Package: 0603	T _{critical}	119	°C
	C102	2.2uF	≥58V	ANY	Electrolytic Cap	EN_ITP	Enabled	
	C103	10uF	25V	ANY	SMD Package: 1206	T _{hat}	110	°C
	R31	2.2kohm	1%	ANY	SMD Package: 0805	L _{out_red}	220	mA
	R32	30kohm	1%	ANY	SMD Package: 0603	t _{stop}	10	s
	R33	5.1kohm	1%	ANY	SMD Package: 0603	Startup & shutdown		
	R34	47kohm	1%	ANY	SMD Package: 0603	t _{rr}	0.5	ms
	R36	18kohm	1%	ANY	SMD Package: 0603	V _{out_dim_min}	11.9	V
	R37	2.2kohm	1%	ANY	SMD Package: 0805	V _{out_start}	9.5	V
FB_SEC	R100	4.7kohm	1%	ANY	SMD Package: 1206	Central _{loop_init}	DCM	
	R101	47kohm	1%	ANY	SMD Package: 1206	N _{ABM_{init}}	100	
	D101	≥8.1A	≥237V	ONSEMI	MBRB40250TG	Central loop		
	C7	0.1uF	≥70V	ANY	SMD Package: ≥0805	PL _{KP_QRM}	550	
	C12+1013	940uF	63V	ANY	Electrolytic Cap	PL _{KL_QRM}	8	
	C99	OPEN	-	-	-	PL _{KL_DCM}	17000	
	R99	OPEN	-	-	-	PL _{KL_DCM}	200	
	Q3, Q4	2N7002	60V	INFINEON	2N7002 (SOT-23)	PL _{KP_ABM}	64	
	D7	Dual Diode	≥237V	INFINEON	BAT240A (SOT-23)	PL _{KL_ABM}	32	
	D8, D9	OPEN	-	-	-	Dimming		
	ZD4, ZD5	Zener 12V	±5%	ANY	SOD-323 arrimilar	EN_DIM	Enabled	
	C10	1000pF	≥296V	ANY	Discrete or SMD 1206	V _{DIM_min}	0.11	V
	C11	0.1uF	≥25V	ANY	SMD Package: 0603	L _{out_dim_min}	88.0	mA
	R24+R29+R30	1.3kohm	1%	ANY	Power rating: 1W	C_DIM	Linear	
OUTPUT BLEEDER	R27, R28	1kohm	1%	ANY	SMD Package: 0805	EN_DIM _{TO_OFF}	Disabled	
	R9	OPEN	-	-	-	V _{DIM_{off}}	0.1	V
	C9	2200pF	≥277V _{ac}	ANY	Safety Ceramic Cap	EN _{SQW}	Disabled	
	C31	470p	50V, COG	ANY	SMD Package: 0603	Holding mode		
	J4	3 pin	-	ANY	3 pin	f _{rru_max}	180.50	kHz
	F1	UL safety fuse	≥0.95A	ANY	-	t _{on_max}	11.3	us
	M0V1	surge arrester	≥332.4	ANY	Radial, Disc Type	t _{on_min}	1.2	us
	D1+D2	surge arrester	≥391.7	ANY	Car Style: 15KE	f _{rru_min_DCM}	12.00	kHz
	R1, R50, R51	0ohm	-	ANY	SMD Package: 0603	EN_ABM	Disabled	
						Power Factor Correction		
						EN_EFFC	Enabled	
						C _{EMI}	0.100	uF
						Fine tuning		
						t _{min_dcmag}	3.0	us
Y-CAP						t _{PDC}	250	ns
						t _{ZCDPD}	410	ns
						T _{coupling}	1.020	
						R _{in}	15	ohm
						N _{DCM_{mod}_gain}	8	
						a_DIM	0	mV/K
DEBUG/PROGRAMMING								
SAFETY & LINE SURGE								
JUMPERS								

Figure 3 Example of auto-generated BOM and IC parameters

2 Overview

This section provides general information about the tool.

2.1 Software and version

- Software name: Microsoft Excel
- Software version: 2010 or later
- Excel file format: *.xlsm (macro-enabled Excel sheet)

2.2 Worksheets

There are 3 worksheets in this Excel tool by default.

- The “SCH” worksheet shows a schematic of the auto-generated BOM
- The “Wire” worksheet shows wire table used in the calculation of the auto-generated transformer drawing
- The “Simulation & Design” worksheet is the tool itself with which users can enter design inputs and where the simulation output/system design will be generated

Note: “SCH” and “Wire” worksheets are for reference only. The workbook structure is protected by password.

2.3 Cell protection and legend

The “Simulation & Design” worksheet is protected by password. Users can only enter or modify values in the design input cell, which is light-green-coloured, as shown in [Figure 4](#).

Cell Legend:		
Design Input	Read/Write	
Info	Read Only	
Output	Read Only	

Figure 4 Cell legend of “Simulation & Design” worksheet

2.4 Cell comments

Comments are available to provide explanations or give guidance on every design input and calculation output. For an example, refer to [Figure 5](#).

Est. System I _{out_min} (mA)	<Calculation output> Estimated System I_{out} at minimum dimming
88.0	Values shown here should be same or very close to I _{out_dim_min} for good output accuracy.
88.1	Note: This value is just an estimation based on calculation. Please check actual board performance to confirm.

Figure 5 Example of a cell comment explanation

2.5 Expand/collapse button and status bar

Each design step and generated output can be expanded or collapsed according to the user's preference. The expand/collapse button is available on the left side (See [Figure 6](#)).

Also, the status of each step will be shown in the status bar on the right side (See [Figure 6](#)):

- “OK” means that no error or warning has been found.
- “WARNING” means that a warning, but no error has been found. The user should pay attention to the warnings.
- “ERROR” means an inappropriate design input has been found. The user should adjust the design input.

<div> <div>Press “+” to expand</div> <div>Press “-” to collapse</div> </div>	10	Step 1: System Simulation & Transformer Design	OK	Status Bar
	73			
	105	Step 2: Transformer Construction (Optional)	OK	
	165			
	166	Generate: TRANSFORMER DRAWING	OK	
	254			
	255	Step 3: Finalize System Design	OK	
	298			
	324	Generate: BOM & IC PARAMETERS	OK	
	4001			

Figure 6 Expand/collapse button and status bar

2.6 Other important notes

- The Excel macro must be enabled to use the tool when opened and must be saved in *.xlsm format.
- The Excel zoom level setting should be set to a minimum of 90% for proper content display.
- The user can click the “Optimize View” shortcut button for the best view settings (zoom level: 110%, full screen, formula bar disabled). To exit full-screen mode, press the “ESC” key.
- Press the “Enter” key on the design input cell whenever its value is modified. This will ensure that the output results are updated with the calculation based on the new modified value. Depending on the CPU resources, the output results update could take up to 3 seconds.

3 User guide

This section provides a detailed guide on each of the 3 main design steps given below:

- Step 1: System simulation and transformer design
- Step 2: Transformer construction
- Step 3: System design finalization

3.1 STEP 1 – System simulation and transformer design

In this step, the system design outlined below is based on the simulation/calculation output:

- Transformer design (primary inductance, turns ratios of all windings)
- Maximum switching frequency parameter setting
- Output and input OVP-related parameters setting
- Minimum dimming level-related parameters setting
- Input and output capacitor values
- HV pin series resistor value
- Vcc supply source selection
- Voltage regulator circuit design (if necessary)
- Vcc capacitor value
- Secondary 0-10V dimming circuit design (if necessary)
- MOSFET and output diode voltage rating

+	10	Step 1: System Simulation & Transformer Design	OK
	73		
+	105	Step 2: Transformer Construction (Optional)	OK
	165		
+	166	Generate: TRANSFORMER DRAWING	OK
	254		
+	255	Step 3: Finalize System Design	OK
	298		
+	324	Generate: BOM & IC PARAMETERS	OK
	4001		

Figure 7 STEP 1 – System simulation and transformer design

3.1.1 Project specification input

The first half of the step 1 main design input (as circled in red in [Figure 8](#)) is related to project specification, so is straightforward to fill in.

- **V_{in}:** AC input voltage range
- **V_o:** Output load voltage range (LED forward voltage range) at non-dimming
- **I_{out_set} setting:** Non-dimmed I_{out} setting by IC parameterization
- **V_{outOV} setting:** Output OVP level setting by IC parameterization (based on typ. value)
- **Efficiency:** System efficiency estimation
- **I_{out} Dimming?:** Output dimming (No / Primary side Dimming / Secondary 0-10V dimming)
- **EN_OVP_In setting:** Input OVP enabled/disabled setting by IC parameterization

- **V_inOV setting:** Input OVP level setting by IC parameterization (based on typ. value)

If necessary, please refer to the cell comments or to the “Tips and Interactive Info” section for guidance and details.

Step 1: System Simulation & Transformer Design				
Main Design Input				
	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	20.0	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	305.0	328	351.0	Range: 297.9 ~ 396.2; Tolerance: +/- 7%
Np/Ns Selection		3.870		Higher for better Ithd. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 543 ~ 787
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz (if TJ≤125°C), ≤136.4kHz (if TJ >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:8, Min:32, Off:0)
t_on_min setting (us)		1.2		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed. (Perfect Sine is just for reference purpose.)
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			

ENTER DESIGN INPUT

Figure 8 Project specification (Step 1 Main design input)

3.1.2 Transformer electrical spec. input

N_p/N_s selection refers to the turn ratio of primary main winding turns to secondary main winding turns. Based on quasi-resonant (QR) constant on-time operation, higher N_p/N_s values give lower iTHD. However, please take note that MOSFET drain voltage will increase with higher N_p/N_s values and it should not exceed the MOSFET drain voltage rating.

L_p is the primary main winding inductance of the transformer. Too high a value could force the system to enter CCM protection mode, while too low a value could cause discontinuous conduction mode (DCM) high-switching frequency operation at non-dimming level and high output current at min-dimming level.

Tips are available in the “Tips and Interactive Info” section to help users to find the right N_p/N_s and L_p values by dynamically calculating a recommended value range based on project specification input (as shown in the red-highlighted text in [Figure 9](#)). It is recommended (but not mandatory) to follow the tips given there.

Step 1: System Simulation & Transformer Design				
Main Design Input				
	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	20.0	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	305.0	328	351.0	Range: 297.9 ~ 396.2; Tolerance: +/- 7%
Np/Ns Selection		3.870		Higher for better Ithd. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 543 ~ 787
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:8, Min:32, Off:0)
t_on_min setting (us)		1.2		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed. (Perfect Sine is just for reference purpose.)
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			

ENTER DESIGN INPUT

ENTER DESIGN INPUT

Figure 9 Transformer electrical spec (Step 1 Main design input)

The ICL8105 flyback transformer **L_p** and **N_p/N_s selection** have to consider many factors relating to performance, such as the power factor, optimized iTHD ([Section 3.1.5](#)), optimum switching frequency range ([Section 3.1.6](#)), minimum dimming current ([Section 3.1.7](#)) and voltage rating of the MOSFET/output diode ([Section 3.1.11](#)). By referring to the system simulation/calculation output of these performance factors in this step, the user can find the optimized values for these 2 design inputs.

Of course, it is important to take note that whatever design is finalized in step 1 can only be valid provided the transformer inductance and all numbers of winding turns can fit in the transformer construction with the desired core/bobbin size (decided by the board form factor) and acceptable losses (conduction and core loss). Such transformer construction checks can be carried out easily with step 2 afterwards.

3.1.3 Input capacitor and MOSFET parasitic capacitor values input

C_{in}, input capacitor refers to the DC capacitor placed after the bridge rectifier. Higher C_{in} values give better EMI but worse power factors, and vice versa. However, please take note that different values here could have a slight impact on the minimum dimming level.

MOSFET Co(tr) refers to the MOSFET time-related effective output capacitance. It is mainly used to estimate the LC resonant period for more precise QR frequency estimation. As a start, please refer to the cell comment for a list of Co(tr) values based on Infineon MOSFETs.

Tips are available in the “Tips and Interactive Info” section to help the user to get the rough values of these inputs (as shown in the red-highlighted text in [Figure 10](#))

Step 1: System Simulation & Transformer Design				
Main Design Input				
	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	20.0	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	305.0	328	351.0	Range: 297.9 ~ 396.2; Tolerance: +/- 7%
Np/Ns Selection		3.870		Higher for better Ithd. Tips: Use 3.82 ~ 4.58
Lp (uH)		544.0		Higher for lower dim current. Tips: Use 543 ~ 787
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz (if Tj≤125°C), ≤136.4kHz (if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:8, Min:32, Off:0)
t_on_min setting (us)		1.2		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed. (Perfect Sine is just for reference purpose.)
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			

ENTER DESIGN INPUT

Figure 10 Input capacitor and MOSFET parasitic capacitor values input (Step 1 Main design input)

3.1.4 IC timing parameters input

f_{sw_max} setting refers to the controller maximum switching frequency parameterization. As shown in the tips (see red highlighted text in [Figure 11](#)), the maximum configurable value is limited according to the maximum operating junction temperature.

The lower f_{sw_max} setting could give better iTHD in most cases, particularly during high input voltage, because the system will shift more of its operating point over the half-sine wave period from quasi-resonant (QRM) to discontinuous conduction mode (DCM). For more details, please refer to [Section 3.1.5](#) or [Figure 13](#).

N_DCM_MOD_GAIN setting refers to the modulation gain of the maximum allowable switching frequency over a half sine wave period. Its main purpose is to improve light quality when dimming with DCM switching. Furthermore, it also helps to improve the iTHD in most cases. User can adjust the modulation gain as following:

- Select “8” for maximum modulation gain
- Select “16” for medium modulation gain
- Select “32” for minimum modulation gain
- Select “0” for no modulation

Note: “0” setting option is only available if I_{out} dimming is set to “No” in step 1 main design input.

The lower N_DCM_MOD_GAIN setting (except value “0”) could give better iTHD in most cases, particularly during high input voltage, because the system will shift more of its operating point over the half-sine wave period from quasi-resonant (QRM) to discontinuous conduction mode (DCM). For more details, please refer to [Section 3.1.5](#) or [Figure 13](#)

t_{on_min} setting refers to the ICL8105 controller minimum on-time. Please use lower value to achieve a lower dimming level. However, if it is set too low, please beware that it could result to current steps while dimming. The setting range is shown in the tips (see red highlighted text in [Figure 11](#)).

Step 1: System Simulation & Transformer Design				
Main Design Input				
	min	typ	max	Tips & Interactive Info
Vin (Vrms)	90	230	277	AC input voltage (normal operation)
Vo (V)	18.0	20.0	45.0	Non-Dimming LED output voltage range
V_outOV setting(V)	46.0	48.4	55.6	Autoset to Vo_max/0.93; tolerance: -5%, +15%
I_out_set setting (A)		0.88		Output current at non-dimming condition
Efficiency (%)		90%		Est. Efficiency (Vin_min, Pout_max)
Iout Dimming?	Yes (Secondary side 0-10V dimming)			Iout Dimming option (see comment for details)
EN_OVP_In setting	Enabled			Input OVP (Enabled/Disabled?)
V_inOV setting (V)	305.0	328	351.0	Range: 297.9 ~ 396.2; Tolerance: +/- 7%
Np/Ns Selection		3.870		Higher for better Ithd. Tips: Use 3.82 ~ 4.58
L_p (uH)		544.0		Higher for lower dim current. Tips: Use 543 ~ 787
Cin, Input capacitor (uF)		0.220		Tips: <40W: 0.15uF; 40 ~ 60W: 0.22uF
MOSFET Co(tr) (pF)		69.0		Tips: See comment for list of MOSFET Co(tr) values
f_sw_max setting (kHz)		180.80		Tips: ≤180.8kHz(if Tj≤125°C), ≤136.4kHz(if Tj >125°C)
N_DCM_MOD_GAIN setting		8		Tips: See comment. Modulation(Max:8, Min:32, Off:0)
t_on_min setting (us)		1.2		Tips: see comment. Range: 1~2.5
Normalized Ipri_avg simulation #1	Perfect Sine			Select checkpoint for iTHD optimization, if needed. (Perfect Sine is just for reference purpose.)
Normalized Ipri_avg simulation #2	Vin_typ, Vo_max			

ENTER DESIGN INPUT

Figure 11 IC timing parameters input (Step 1 Main design input)

3.1.5 Simulation output: Primary average input current curve

For low iTHD, the primary average input current curve should be as close as possible to the shape of a positive half-sine waveform. Based on the step 1 main design input, this tool will simulate the normalized primary average input current curve across a half-sine wave period for iTHD optimization. The simulation output is shown in the blue area on the right side of [Figure 12](#).

The input and output voltage (V_{in}, V_o) conditions of the current curve simulation are based on checkpoint #1 and #2 in the main design input of step 1, as shown in the red circled box in [Figure 12](#). Users can select any of the following for each simulation checkpoint:

- Perfect Sine
- V_{in_min}, V_{o_max}
- V_{in_min}, V_{o_min}
- V_{in_typ}, V_{o_max}
- V_{in_typ}, V_{o_typ}
- V_{in_typ}, V_{o_min}
- V_{in_max}, V_{o_max}
- V_{in_max}, V_{o_typ}
- V_{in_max}, V_{o_min}

Note: All checkpoints are based on a non-dimmed condition.

A practical use case example for users would be to choose either of the following options:

- Simultaneously simulate 2 current curves with different V_{in}, V_{out} conditions **OR**
- Simulate 1 current curve while having the other checkpoint set as “Perfect Sine” for reference/comparison.

In the example shown in [Figure 12](#), the user is comparing the primary average input current curve at “V_{in_typ}, V_{o_max}” (typical input voltage, maximum output voltage) with the “Perfect Sine” reference.

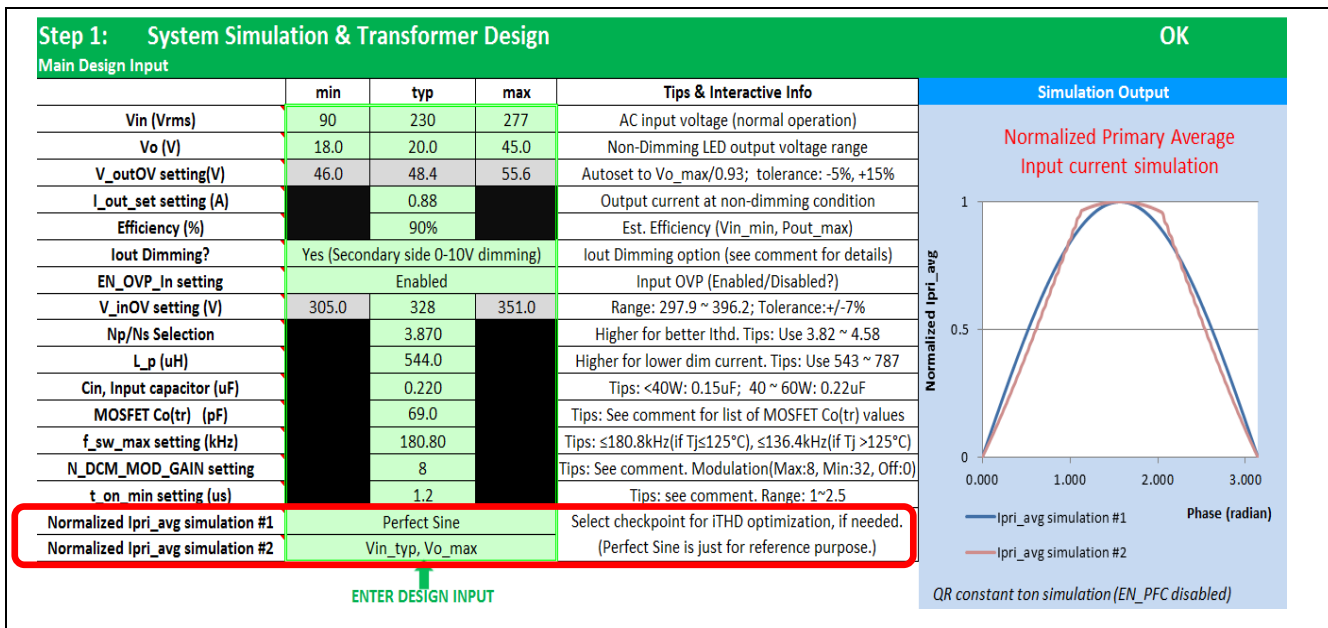

ENTER DESIGN INPUT

Figure 12 Normalized primary average current curve simulation checkpoint (for iTHD optimization)

It is possible to improve iTHD especially at high input voltages with the ICL8105 by reducing the **f_{sw_max} setting** or **N_{DCM_MOD_GAIN} setting** as this will increase the DCM operating area across the current curve (see the example in [Figure 13](#) & [Figure 14](#)).

However, please take note that there could be an impact on the efficiency if the DCM operating area increases too much (QR operating area reduces too much).

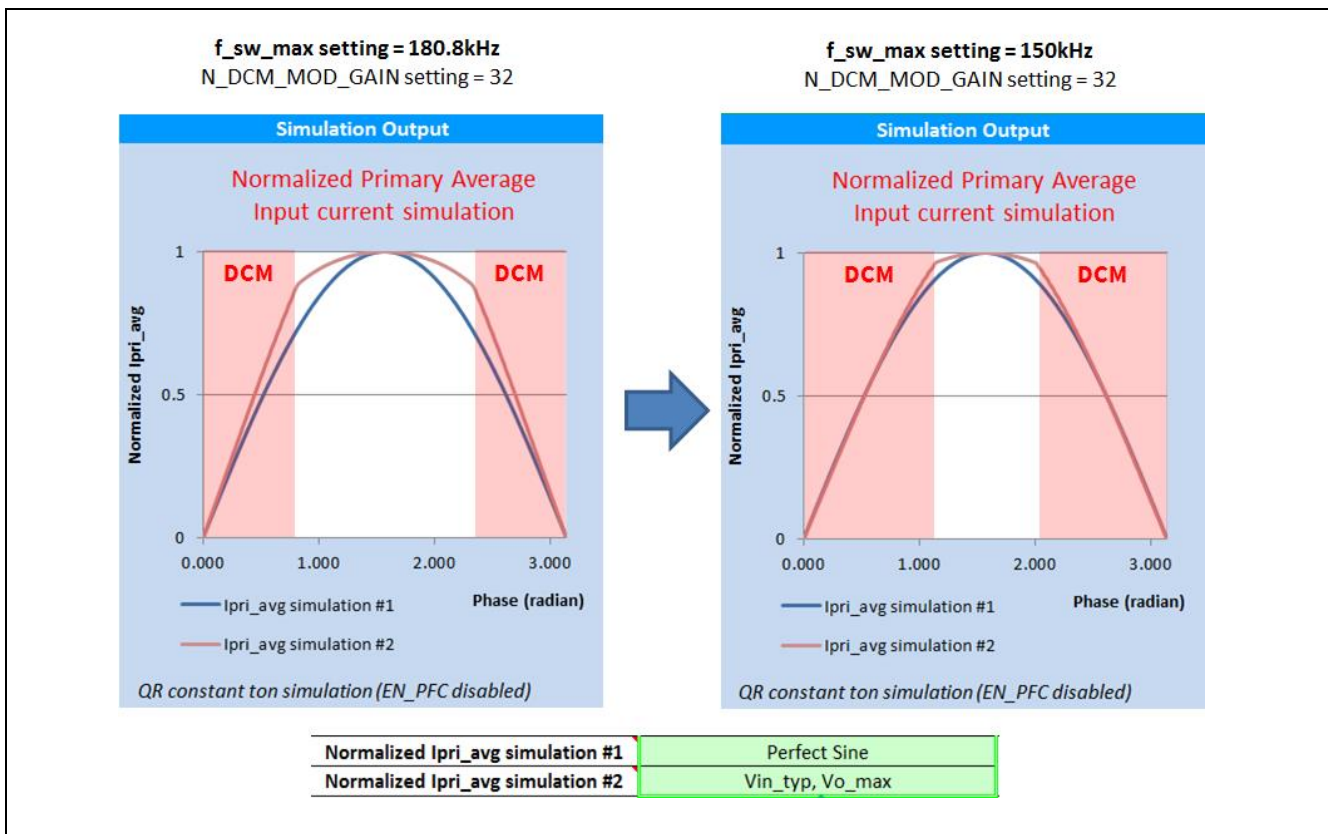


Figure 13 iTHD improvement by switching frequency setting reduction

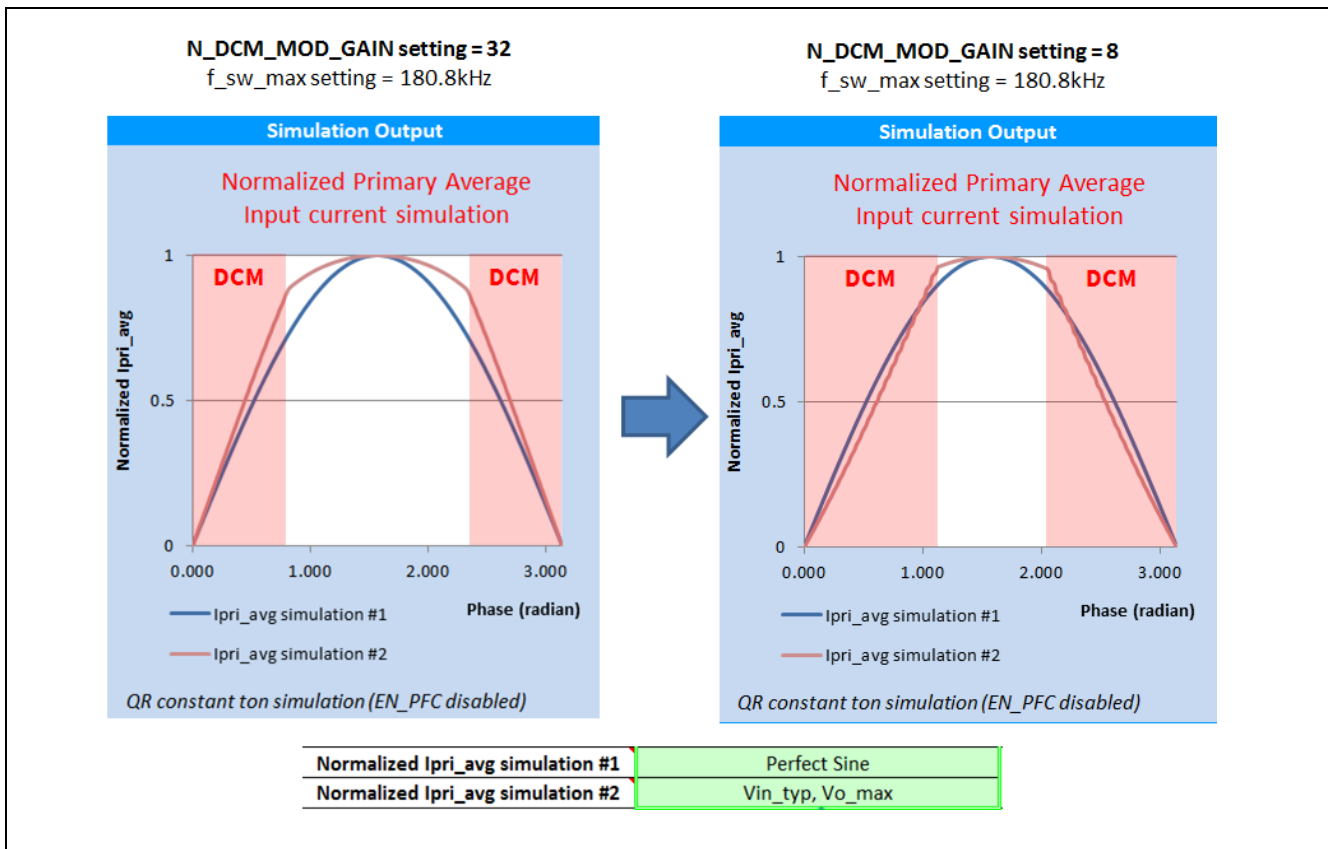


Figure 14 iTHD improvement by N_DCM_MOD_GAIN setting reduction

3.1.6 Non-dimming system switching behavior estimation

In step 1 section I, there will be a simulation/calculation of the system switching behavior with non-dimming at the peak of the input voltage sine wave (as shown in [Figure 15](#)).

Simulation/Calculation Output									
I. Non-dimming System switching behaviour at peak of input voltage sine wave									
V_{in} (Vrms)	V_o (V)	I_{out} (A)	$t_{on} / (t_{on} + t_{demag})$	$t_{valley1}$ (us)	Switching	I_{pri_pk} (A)	t_{on} (us)	f_{sw} (kHz)	
90	18.0	0.88	0.35	0.61	QR	1.436	6.14	55.68	
90	45.0	0.88	0.58	0.61	QR	2.311	9.88	56.47	
230	18.0	0.88	0.18	0.61	QR	1.149	1.92	86.91	
230	20.0	0.88	0.19	0.61	QR	1.190	1.99	91.19	
230	45.0	0.88	0.35	0.61	QR	1.694	2.83	114.51	
277	18.0	0.88	0.15	0.61	QR	1.127	1.56	91.14	
277	20.0	0.88	0.17	0.61	QR	1.168	1.62	95.79	
277	45.0	0.88	0.31	0.61	QR	1.711	2.38	120.03	

Figure 15 Non-dimming system switching behavior (Step 1 Simulation/calculation output I)

t-valley1 refers to the timing between the end of demagnetization and the first QR valley. It is just a rough estimation based on the half-resonant period of L_{pri} & MOSFET $C_o(tr)$. In [Section 3.1.3](#), the suggestion is to enter a MOSFET $C_o(tr)$ value based on the MOSFET datasheet – but keep in mind that other parasitics are not yet considered, which could affect the accuracy of this calculation output.

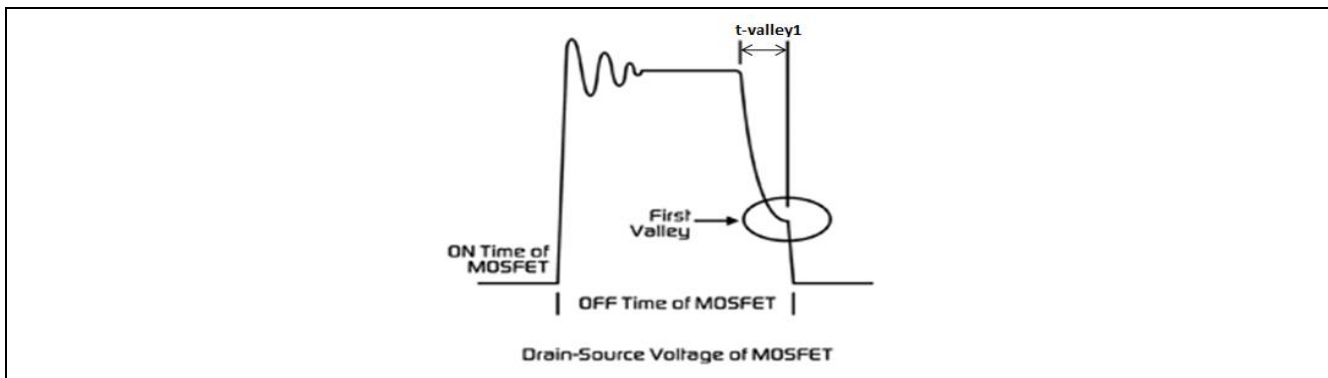


Figure 16 Example of t_{valley1} timing in MOSFET drain voltage waveform

Switching refers to the switching characteristics and controller operation. There are 4 possible outputs here:

- QR: Quasi-resonant switching with t_{on} controlled (OK)
- DCM: DCM switching with t_{on} controlled and $f_{\text{sw_max}}$ (OK)
- ERROR: Invalid calculation as the system enters period-controlled DCM (NOT GOOD)
- CCM: Continuous conduction mode protection (NOT GOOD)

Ipri_pk refers to the primary peak current. If the tool detects that the $I_{\text{pri_pk}}$ value (at $V_{\text{in_min}}$, $V_{\text{o_max}}$) is not the maximum of all conditions, an error will be shown.

ton refers to the MOSFET on-time. If $t_{\text{on}} < t_{\text{on_min}}$, **switching** will show “ERROR” because it means the controller enters the period-controlled DCM too early, which should not happen in non-dimming conditions.

fsw refers to the switching frequency. If $f_{\text{sw}} < 20 \text{ kHz}$, **switching** will show “CCM”, which is not supported by the controller and the CCM protection will be triggered. If $f_{\text{sw}} = f_{\text{sw_max}}$, **switching** will show “DCM”, which means the entire current curve is in DCM operation.

3.1.7 Vcc supply source selection and minimum output current estimation

In step 1 section II, the user has to select a **Vcc supply source** for the design and check the estimated minimum output current (see red-circled boxes in [Figure 17](#)).

There are 2 possible choices, as shown below.

- External: The Vcc supply is not from the flyback AUX winding (e.g. external standby power circuit)
- Flyback AUX: The Vcc supply source is from the flyback AUX winding

If **Vcc supply source** = “Flyback AUX”, the minimum output current estimation can be lower than compared to **Vcc supply source** = “External” due to energy being drawn from the transformer via the AUX winding for the Vcc supply.

As shown in [Figure 17](#), there are other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the output current at minimum dimming.

EN_ABM setting refers to an IC parameterization input that enables or disables the active burst mode (ABM). If disabled, the controller will only operate in quasi-resonant (QR) mode and discontinuous conduction mode (DCM).

fsw_min_DCM setting refers to an IC parameterization input that sets the minimum DCM switching frequency. The configurable range is 3 ~ 20 kHz. Lower minimum output current can be achieved with lower $f_{\text{sw_min_DCM}}$ setting but please beware of audible noise if configured to be less than 18 kHz.

ΔV of V_{o_min} @ min dim is a design input that defines the change percentage of V_{o_min} at minimum dimming. The selectable value is 0%, -5%, -10%, ... , -25%. This input is needed because V_{o_min} (step 1 main design input) is defined for a non-dimmed condition; therefore the LED voltage at minimum dimming should be lower than V_{o_min} by a certain percentage. For instance, if $V_{o_min} = 18$ V and ΔV of V_{o_min} @ min dim is -10%, it means the voltage of a minimum number of LEDs is approx. 16.2 V at the **I_out_dim_min setting**.

I_out_dim_min setting refers to an IC parameterization input that sets the controller target output current at minimum dimming. The configuration range here is from 10 mA to I_out_set setting. It is highly recommended not to set this value too low to have reasonable output accuracy and startup time (see **Est. Worst Case Startup Time** calculation in [Section 3.1.8](#)).

Est. System Iout_min refers to the simulation output of the estimated system output current at the minimum dimming level. This value should be same or close to the **I_out_dim_min setting** for good output accuracy. If Iout Dimming is set to “No” in step 1 main design input, Est. System Iout_min will show “No Dimming”.

II. Vcc supply source select & Iout_min estimation						
Vin (Vrms)	Line Freq(Hz)	Vcc supply source select	EN_ABM setting	f_sw_min_DCM setting (kHz)	ΔV of V_{o_min} @ min dim (%)	I_out_dim_min setting (mA)
277	50	Flyback AUX	Disabled	12.00	-10%	88.0
	60					88.1

SELECT VCC SOURCE
ADJUST IF NEEDED

Figure 17 Vcc supply source select and minimum output current estimation (Step 1 Simulation/calculation output II)

3.1.8 Maximum output ripple, worst case startup time estimation

In step 1 section III, the user has to choose the optimum **output capacitor selection** based on the simulation results of maximum output ripple and worst case startup time estimation (see red-circled boxes in [Figure 18](#)).

As shown in [Figure 18](#), there are also other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect either the output ripple or the startup time.

Output Cap tolerance is the design input that defines the tolerance specification of the **output capacitor selection**. Based on this tolerance value, the minimum and maximum output capacitance will be used for estimating the maximum output ripple and worst case startup time, respectively.

NLED in series @ V_{o_min} is the design input which specifies the number of LEDs at V_{o_min} . For example, based on $V_{o_min} = 18$ V, the user can select either 6 or 7 from the dropdown box.

Dynamic resistance for each series LED @ I_out_set is the design input that specifies the dynamic resistance of a single LED at I_out_set setting which can be calculated from the I-V curve in the LED datasheet. The multiplication of this value with **NLED in series @ V_{o_min}** will be used to simulate **Est. Max Iout ripple**.

ΔV of V_{o_max} @ min dim is the design input that defines the percentage change of V_{o_max} at minimum dimming. The selectable value is 0%, -5%, -10%, ... , -25%. This input is needed because V_{o_max} (step 1 main design input) is defined for the non-dimmed condition; therefore the LED voltage at minimum dimming should be lower than V_{o_max} by a certain percentage. For instance, if $V_{o_max} = 45$ V and the selected value is -10%, the voltage of the maximum number of LEDs is approx. 40.5 V at **I_out_dim_min setting**. The selected value here should be the same as **ΔV of V_{o_min} @ min dim** else there will be a warning.

R_HV setting refers to the design input of the resistor value connected in series with the ICL8105 HV pin and it is also an IC parameterization value. This value only has an effect on the startup time but not on the output

User guide

ripple. The configurable range is dependent on the main design input. If the user inputs an out-of-range value, an error will pop up along with the configurable range.

Est. Max Iout Ripple is the simulation output that estimates the maximum output current peak-to-peak ripple percentage and it is likely at the V_{o_min} , I_{out_set} condition.

Est. Worst Case startup is the simulation output that estimates the worst case startup time and is likely at the V_{in_min} , V_{o_max} , I_{out_min} condition (for non-dimming designs, it is based on **I_out_set setting** instead).

III. Max Output Ripple, Worst Case Startup Time estimation									
V_o , I_{out}	$V_{in@50Hz}$ (Vrms)	Output Capacitor selection (uF)	Output Cap Tolerance (+/- x %)	NLED in series @ V_{o_min}	Dynamic Resistance for each series LED @ I_{out_set} (Ω)	ΔV of V_{o_max} @ min dim (%)	R_{HV} setting (k Ω)	Est. Max Iout Ripple (+/- xx %)	Est. Worst Case Startup Time (sec)
V_{o_min} , I_{out_set}	90.0	940	20%	6	0.40		66.0	58.6%	
	277.0							63.6%	
V_{o_max} , I_{out_min} (est. 88 mA)	90.0					-10%			1.00

SELECT CAP VALUE
ADJUST IF NEEDED

Figure 18 Max output ripple, worst startup time estimation (Step 1 Simulation/calculation output III)

3.1.9 Primary aux turns ratio and Vcc circuit design calculation

In Step 1 section IV, the user has to decide on the **Vcc cap** value and primary auxiliary winding turns ratio, **Na/Ns selection** based on the calculation output of **min Vcc cap**, **min Na/Ns** and **max Na/Ns** (see red-circled boxes in [Figure 19](#)).

Please take note that changing **Vcc cap** value would have an effect on the **Est. Worst Case Startup Time** in [Section 3.1.8](#).

For the Vcc circuit design, the tool will also check and output whether **Pri Aux winding Vcc regulator needed** applies in the design based on the step 1 main design input and selected Vcc supply source in section II.

If Pri Aux winding Vcc regulator needed is “Yes”, the tool will calculate the **Vcc reg. min input cap** value as well.

IV. Pri Aux turns ratio, Vcc circuit design						
Pri Aux winding Vcc regulator Required?	Vcc reg. Min input cap (uF)	Min Vcc cap (uF)	Min Na/Ns	Max Na/Ns	Vcc Cap (uF)	Na/Ns selection
Yes	4.7	22.00	0.991	1.090	33.00	1.000

SELECT CAP VALUE & TURNS RATIO

Figure 19 Primary aux turns ratio and Vcc circuit design (Step 1 Simulation/calculation output IV)

3.1.10 Secondary aux turns ratio and IEC60929-compliant 0-10 V circuit design (with CDM10V)

In step 1 section V, the user has to decide on the secondary auxiliary winding turns ratio, **Nsec_aux/Ns selection** based on the calculation output of **Min Nsec_aux/Ns** and **Max Nsec_aux/Ns** (see red-circled boxes in [Figure 20](#)).

CDM10V is a fully integrated 0-10V dimming interface IC from Infineon which transmits secondary side analog voltage based signals from 0-10V dimmer to primary side, by driving an external opto-coupler with a 5mA current based PWM signal. The secondary auxiliary winding is necessary to supply the operating voltage of CDM10V. For more details about CDM10V, please visit Infineon website: <http://www.infineon.com/cdm10v>

Therefore, please note that this section is only necessary if the I_{out} dimming option selected in step 1 main design input is “Secondary side 0-10 V Dimming”.

V. Sec Aux turns ratio, IEC60929 Compliant 0-10V Dimming design (using CoolDim CDM10V)

Min Nsec_aux/Ns	Max Nsec_aux/Ns	Nsec_aux/Ns selection
0.89	1.07	0.98

← SELECT TURNS RATIO

Figure 20 Secondary aux turns ratio, IEC60929-compliant 0-10 V dimming design (Step 1 Simulation/calculation output V)

3.1.11 MOSFET Vds_max, output diode Vr_max estimation

Similar to any flyback transformer design, the maximum MOSFET drain voltage, **MOSFET Vds_max** and maximum output diode reverse voltage, **Output diode Vr_max** have to be calculated. Therefore, in step 1 section VI, the user has to check if these calculation outputs are ok for the component selection (see red-circled box in **Figure 21**).

The calculation will be based on 2 kinds of conditions, as shown below:

- Vin_max, V_outOV_Max (Output over-voltage protection at maximum input voltage)
- V_inOV_max, V_out_max (Input over-voltage protection at maximum output voltage)

Note: If input over-voltage protection, EN_OVP_In setting is “disabled”, calculating condition V_inOV_max above will be replaced by Vin_max instead.

For output over-voltage protection condition, if Vds_max is 800~900 V, there will be a warning; if it exceeds 900 V, there will be an error. For input over-voltage protection condition, if Vds_max exceeds either 800 V or 900 V, there will only be a warning.

As shown in **Figure 21**, there are other design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the MOSFET Vds_max and output diode Vr_max.

MOSFET Vds_spike refers to the spike voltage (due to leakage inductance) on the MOSFET. As a rule of thumb, it should be at least 45% of **Vin_max**. For example, If Vin_max = 300Vac, the minimum value will be 135 V.

Output Diode Vr_spike refers to the spike voltage on the output diode. As a rule of thumb, it should be at least 40% of (**Vreflect_sec** + **V_outOV_max**). Vreflect_sec is the secondary winding reflection voltage when flyback MOSFET is switched on. V_outOV_max refers to maximum output over-voltage level.

If the **MOSFET Vds_max** is too high, the user can either reduce **Np/Ns selection** (Step 1 main design input) or **MOSFET Vds_spike**, but there is a risk of exceeding Vds_max in the actual board test if MOSFET Vds_spike is set too low.

If the **Output Diode Vr_max** is too high, the user can either increase **Np/Ns selection** (Step 1 main design input) or reduce **Output Diode Vr_spike**, but there is a risk of exceeding Vr_max in the actual board test if Output Diode Vr_spike is set too low.

VI. MOSFET Vds_max, Output Diode Vr_max estimation

Vin (Vrms)	Vout (V)	Vreflect_pri (V)	Vreflect_sec(V)	MOSFET Vds_spike(V)	Output Diode Vr_spike(V)	MOSFET Vds_max(V)	Output Diode Vr_max(V)
277	OVP	218.1	101.2	124.7	62.7	734.4	219.6
V_inOV_max	45.0	176.9	128.2			797.8	236.0

← CHECK MOSFET & DIODE VOLTAGE RATING

ADJUST IF NEEDED

Figure 21 MOSFET Vds_max and output diode Vr_max (Step 1 Simulation/calculation output VI)

3.2 STEP 2 – Transformer construction (optional)

In step 2, the user can construct the transformer with suitable wires, core and bobbin for the board design. Upon completion without error in both step 1 and step 2, the transformer drawing is auto-generated.

However, step 2 is optional and can be skipped if not needed, which means that the user can still possibly proceed to complete step 3 for BOM and IC parameters generation despite an error/warning in step 2.

10	Step 1: System Simulation & Transformer Design	OK
73		
105	Step 2: Transformer Construction (Optional)	OK
165		
166	Generate: TRANSFORMER DRAWING	OK
254		
255	Step 3: Finalize System Design	OK
298		
324	Generate: BOM & IC PARAMETERS	OK
4001		

Figure 22 STEP 2 – Transformer construction (optional)

3.2.1 Core and bobbin selection input

Based on the **Bobbin Isolation Type** (Functional/Reinforced) and **Bobbin Mounting Type** (THT/SMD) design input by the user, the **Core Bobbin Selection** dropdown box will be updated and a list of suitable cores and bobbins will be shown (see Figure 23). THT and SMD refer to through-hole and surface mount, respectively.

Step 2: Transformer Construction (Optional)		OK
Main Design Input		
Bobbin Isolation Type	Functional	
Bobbin Mounting Type	THT	
Core Bobbin Selection	PQ2020, THT, 14p [V]	
 SELECT CORE & BOBBIN		

Figure 23 Core and bobbin selection (Step 2 Main design input)

Users can check the core and bobbin properties of the selection, as circled in red in Figure 24.

- Bobbin height, width, length
- Bobbin window, depth, perimeter
- Core effective cross sectional area, A_e and core volume
- Primary margin tape

Step 2: Transformer Construction (Optional)				OK
Main Design Input				
Bobbin Isolation Type	Functional			
Bobbin Mounting Type	THT			
Core Bobbin Selection	PQ2020, THT, 14p [V]			
 SELECT CORE & BOBBIN				
Transformer Parameters	min	typ	max	Tips & Interactive Info
Bobbin Height (mm)			24.14	Please refer Bobbin figures on the right if necessary, to understand these dimensionings
Bobbin Width (mm)			24	
Bobbin Length (mm)			24	
Bobbin Window (mm)	11.7			
Bobbin Depth (mm)	3.15			
Bobbin Perimeter (mm)		34.54		
Core A_e (mm ²)		62		Cross sectional area of the core
Core Volume (mm ³)		2850		Core volume
Primary Margin Tape (mm)		0		Margin Tape not needed
$I_{pri_pk_max}$ (A)			2.311	Step 1 calculation output at V_{in_min} , P_{out_max}
$I_{rms_pri_max}$ (Arms)			0.712	
$I_{rms_sec_max}$ (Arms)			1.9317	Step 1 calculation output at V_{in_max} , P_{out_max}
Max average switching freq. (kHz)			165.5	
Skin Depth (mm)		0.1868		Copper 100°C Skin Depth = $760/\sqrt{f_{sw,max_avg}}$
Max wire size (AWG)		27		based on skin depth; TEX-E 0.37 equivalent
Primary Wire Type		MW Grade 1		based on Magnet Wire (Single Insulation) Table

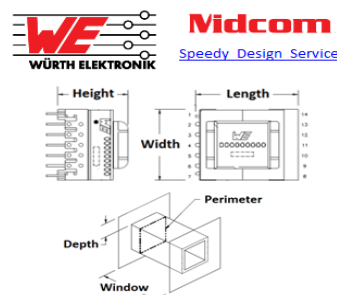
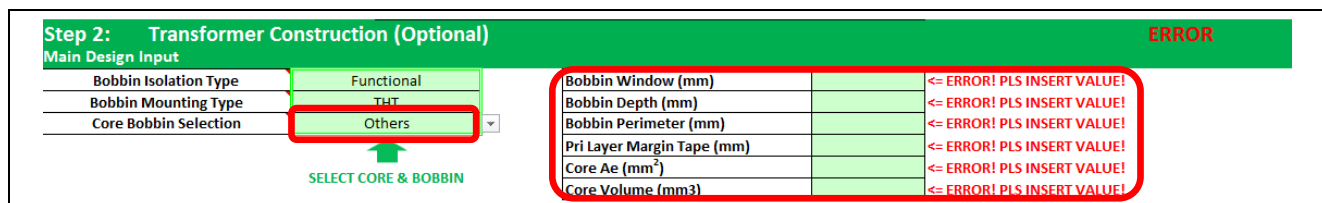


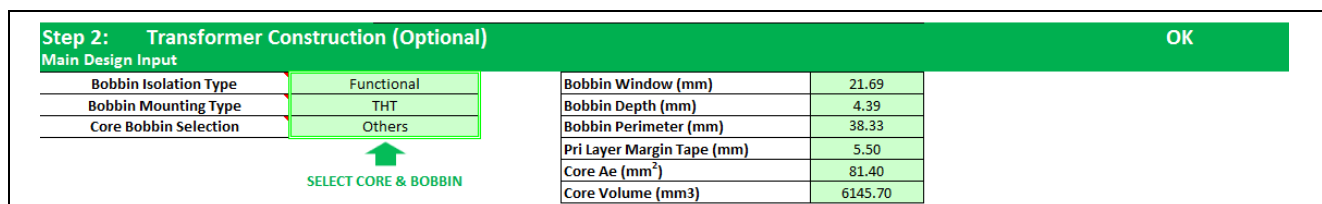
Figure 24 Selected core and bobbin properties display

Alternatively, users can define the core and bobbin properties by selecting “Others” in **Core Bobbin Selection** if the desired part is not in the list. A small table will appear on the right (circled in red in **Figure 25**), which allows the user to enter self-defined property values. There will be errors beside the table at first but once the table is filled up, these errors will disappear (as shown in **Figure 26**).



Step 2: Transformer Construction (Optional)			ERROR
Main Design Input			
Bobbin Isolation Type	Functional		
Bobbin Mounting Type	THT		
Core Bobbin Selection	Others		
SELECT CORE & BOBBIN			
Bobbin Window (mm)		<= ERROR! PLS INSERT VALUE!	
Bobbin Depth (mm)		<= ERROR! PLS INSERT VALUE!	
Bobbin Perimeter (mm)		<= ERROR! PLS INSERT VALUE!	
Pri Layer Margin Tape (mm)		<= ERROR! PLS INSERT VALUE!	
Core Ae (mm ²)		<= ERROR! PLS INSERT VALUE!	
Core Volume (mm ³)		<= ERROR! PLS INSERT VALUE!	

Figure 25 Self-defined core and bobbin properties by selecting “Others”



Step 2: Transformer Construction (Optional)			OK
Main Design Input			
Bobbin Isolation Type	Functional		
Bobbin Mounting Type	THT		
Core Bobbin Selection	Others		
SELECT CORE & BOBBIN			
Bobbin Window (mm)	21.69		
Bobbin Depth (mm)	4.39		
Bobbin Perimeter (mm)	38.33		
Pri Layer Margin Tape (mm)	5.50		
Core Ae (mm ²)	81.40		
Core Volume (mm ³)	6145.70		

Figure 26 Example of inserting values of self-defined core and bobbin properties

Note: The user is not required to enter the bobbin height, width and length if “Others” is selected because these dimensions will only affect the board form factor but not the transformer winding construction itself.

3.2.2 Transformer electrical spec. (read-only information)

Apart from primary inductance and all turn ratios, the following step 1 calculation output will be passed to the step 2 design input (as circled in red box of **Figure 27**) for transformer construction calculation:

- **I_{pri_pk_max}:** Maximum primary peak current (Vin_min, Pout_max)
- **I_{rms_pri_max}:** Maximum primary rms current (Vin_min, Pout_max)
- **I_{rms_sec_max}:** Maximum secondary rms current (Vin_min, Pout_max)
- **Max average switching freq:** Maximum average switching frequency (Vin_max, Pout_max)

Users cannot modify these values because they are read-only information in step 2. Therefore, it is very important to complete step 1 with no errors before proceeding to step 2.

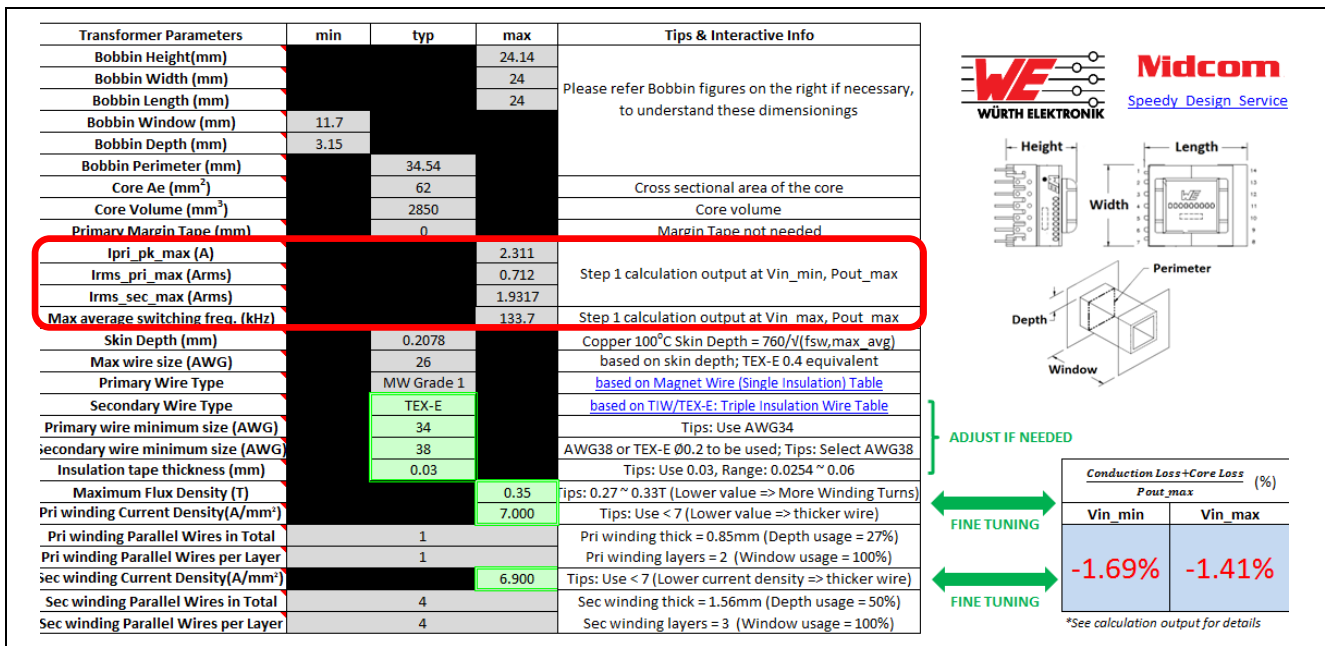


Figure 27 Transformer electrical spec. (read-only information in Step 2)

3.2.3 Skin depth and max wire size (read-only information)

AC electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. Based on the average maximum switching frequency (at Vin_max, Pout_max condition), the skin depth will be calculated based on copper material at 100 °C.

This tool will then select the maximum wire size (AWG) based on the calculated skin depth. This is to avoid selecting wires with a high skin effect. This max wire size (AWG) is applied to the primary wire and TIW-type secondary wire while the max wire size for the TEX-E type secondary wire will also be shown in the "Tips & Interactive Info". Please refer to [Section 3.2.4](#) for details about the wire type.

The skin depth and max wire size information is shown in the red box in [Figure 28](#).

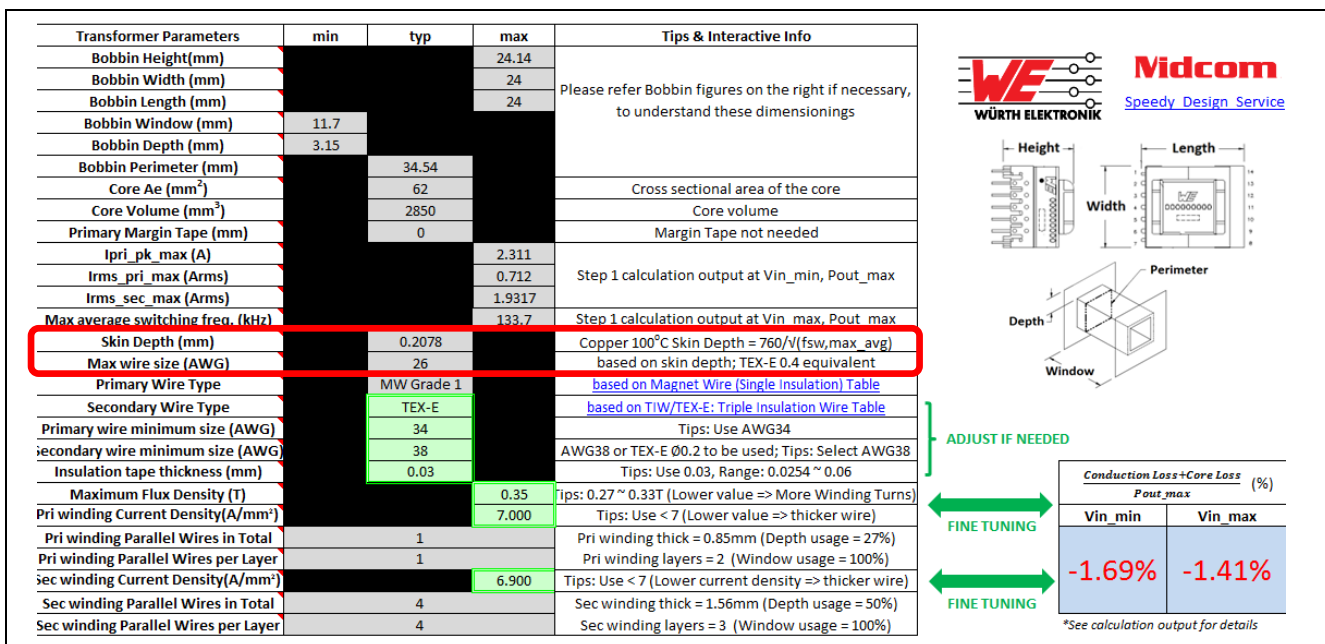


Figure 28 Skin depth and maximum wire size (read-only information of Step 2)

3.2.4 Wire type, minimum wire size and insulation tape thickness input

The **Primary wire type** is fixed as “MW Grade 1”, which means a magnet wire single insulation wire. 2 types of triple insulation wire can be selected for **Secondary wire types**:

- TIW (more common wire type, but the wire diameter is generally larger than TEX-E)
- TEX-E (preferred wire type if available because the wire diameter is generally smaller than TIW)

There is generally a limitation on using overly thin wire in transformer manufacturing. Therefore, the **Primary Wire minimum size** and **Secondary Wire minimum size** have to be specified. Users are recommended to follow the tips suggesting AWG34 for primary wire and AWG38 for secondary wire (as shown in [Figure 29](#)) or else it is also possible to select other wire size, according to their transformer supplier requirement.

Insulation tape is typically applied after each winding layer so it is necessary to specify the **insulation tape thickness**. Please follow the recommended value of 0.03 mm. Otherwise, the user can also specify the desired value within the range of 0.0254 ~ 0.06mm.

Transformer Parameters	min	typ	max	Tips & Interactive Info
Bobbin Height (mm)			24.14	Please refer Bobbin figures on the right if necessary, to understand these dimensionings
Bobbin Width (mm)			24	
Bobbin Length (mm)			24	
Bobbin Window (mm)	11.7			
Bobbin Depth (mm)	3.15			
Bobbin Perimeter (mm)		34.54		
Core Ae (mm ²)		62		Cross sectional area of the core
Core Volume (mm ³)		2850		Core volume
Primary Margin Tape (mm)		0		Margin Tape not needed
I _{pri_pk_max} (A)			2.311	Step 1 calculation output at Vin_min, Pout_max
I _{rms_pri_max} (Arms)			0.712	
I _{rms_sec_max} (Arms)			1.9317	
Max average switching freq. (kHz)			133.7	Step 1 calculation output at Vin_max, Pout_max
Skin Depth (mm)		0.2078		Copper 100°C Skin Depth = 760/√(fsw,max_avg)
Max wire size (AWG)		26		based on skin depth: TEX-E 0.4 equivalent
Primary Wire Type		MW Grade 1		based on Magnet Wire (Single Insulation) Table
Secondary Wire Type		TEX-E		based on TIW/TEX-E: Triple Insulation Wire Table
Primary wire minimum size (AWG)		34		Tips: Use AWG34
Secondary wire minimum size (AWG)		38		AWG38 or TEX-E Ø0.2 to be used; Tips: Select AWG38
Insulation tape thickness (mm)		0.03		Tips: Use 0.03, Range: 0.0254 ~ 0.06
Maximum Flux Density (T)			0.35	Tips: 0.27 ~ 0.33T (Lower value => More Winding Turns)
Pri winding Current Density(A/mm ²)			7.000	Tips: Use < 7 (Lower value => thicker wire)
Pri winding Parallel Wires in Total		1		Pri winding thick = 0.85mm (Depth usage = 27%)
Pri winding Parallel Wires per Layer		1		Pri winding layers = 2 (Window usage = 100%)
Sec winding Current Density(A/mm ²)			6.900	Tips: Use < 7 (Lower current density => thicker wire)
Sec winding Parallel Wires in Total		4		Sec winding thick = 1.56mm (Depth usage = 50%)
Sec winding Parallel Wires per Layer		4		Sec winding layers = 3 (Window usage = 100%)

Primary Wire Type: MW Grade 1

Secondary Wire Type: TEX-E

Primary wire minimum size (AWG): 34

Secondary wire minimum size (AWG): 38

Insulation tape thickness (mm): 0.03

ADJUST IF NEEDED

FINE TUNING

FINE TUNING

Conduction Loss+Core Loss Pout_max (%)	
Vin_min	Vin_max
-1.69%	-1.41%

*See calculation output for details

Figure 29 Wire type, min. wire size and tape thickness (Step 2 Main design input)

3.2.5 Maximum flux density and current density input (fine-tuning)

Maximum Flux Density input is required to calculate the number of turns needed for each winding. More turns are needed if the **Maximum Flux Density** input is lower, and vice-versa. The recommended value will be between 0.27 ~ 0.33 teslas. Maximum value is 0.35 teslas. These design inputs are shown in the red box in [Figure 30](#).

Based on the **Pri Winding Current Density** and **Sec Winding Current Density** input, this tool will find the best combination of the following outputs from the wire tables (as shown in the “Wire” worksheet) that fits the calculated numbers of turns of each winding with the minimum bobbin depth usage.

- Wire Size
- Parallel Wire Number (total)
- Parallel Wire Number (for each layer)

Note: This wire information is shown in the red box in [Figure 30](#).

User guide

In general, the depth usage or winding thickness will be higher if the current density input is lower and vice versa. As a rule of thumb, it is recommended to select a value $< 7 \text{ A/mm}^2$. To start, the user can set the following as an initial check to see if the selected core/bobbin could fit the design.

- Maximum flux density = 0.35 teslas
- Both primary winding current density and secondary winding current density = 7 A/mm^2

If an error shows that the build is too thick, the user should consider selecting a larger core/bobbin or reduce L_p in step 1.

Step 2: Transformer Construction (Optional)
OK

Main Design Input

Bobbin Isolation Type	Functional
Bobbin Mounting Type	THT
Core Bobbin Selection	PQ2020, THT, 14p [V]

↑
SELECT CORE & BOBBIN

Transformer Parameters	min	typ	max	Tips & Interactive Info
Bobbin Height(mm)			24.14	Please refer Bobbin figures on the right if necessary, to understand these dimensionings
Bobbin Width (mm)			24	
Bobbin Length (mm)			24	
Bobbin Window (mm)	11.7			
Bobbin Depth (mm)	3.15			
Bobbin Perimeter (mm)		34.54		
Core Ae (mm ²)		62		Cross sectional area of the core
Core Volume (mm ³)		2850		Core volume
Primary Margin Tape (mm)		0		Margin Tape not needed
Ipri_pk_max (A)			2.311	Step 1 calculation output at Vin_min, Pout_max
Irms_pri_max (Arms)			0.712	
Irms_sec_max (Arms)			1.9317	
Max average switching freq. (kHz)			133.7	Step 1 calculation output at Vin_max, Pout_max
Skin Depth (mm)		0.2078		Copper 100°C Skin Depth = $760/\sqrt{fsw_max_avg}$
Max wire size (AWG)		26		based on skin depth; TEX-E 0.4 equivalent
Primary Wire Type		MW Grade 1		based on Magnet Wire (Single Insulation) Table
Secondary Wire Type		TEX-E		based on TIW/TEX-E: Triple Insulation Wire Table
Primary wire minimum size (AWG)		34		Tips: Use AWG34
Secondary wire minimum size (AWG)		38		AWG38 or TEX-E 0.2 to be used; Tips: Select AWG38
Insulation tape thickness (mm)		0.03		Tips: Use 0.03, Range: 0.0254 ~ 0.06
Maximum Flux Density (T)			0.35	Tips: 0.27 ~ 0.33T (Lower value => More Winding Turns)
Pri winding Current Density(A/mm ²)			7.000	Tips: Use < 7 (Lower value => thicker wire)
Pri winding Parallel Wires in Total		1		Pri winding thick = 0.85mm (Depth usage = 27%)
Pri winding Parallel Wires per Layer		1		Pri winding layers = 2 (Window usage = 100%)
Sec winding Current Density(A/mm ²)			6.900	Tips: Use < 7 (Lower current density => thicker wire)
Sec winding Parallel Wires in Total		4		Sec winding thick = 1.56mm (Depth usage = 50%)
Sec winding Parallel Wires per Layer		4		Sec winding layers = 3 (Window usage = 100%)

Maximum Flux Density (T) 0.35

Pri winding Current Density(A/mm²) 7.000

Pri winding Parallel Wires in Total 1

Pri winding Parallel Wires per Layer 1

Sec winding Current Density(A/mm²) 6.900

Sec winding Parallel Wires in Total 4

Sec winding Parallel Wires per Layer 4

ADJUST IF NEEDED

FINE TUNING

FINE TUNING

Conduction Loss+Core Loss Pout_max (%)

Vin_min	Vin_max
-1.69%	-1.41%

*See calculation output for details

Calculation Output
Manufacturability Check: OK
Build (mm): 3.132
Unused Depth: 0.02mm (1%)

I. Winding turns number calculation

Np (Turns)	58
Ns (Turns)	15

Figure 30 Maximum flux density and current density input (Step 2 Main design input)

If the initial check is ok, the user can fine-tune these 3 design inputs to further optimize the transformer design based on the following guide information generated by the tool (See red-circled parts a, b, c and d in **Figure 31**)

- Bobbin Depth and Window Usage Percentage

For each primary and secondary winding, the bobbin depth and window usage percentage will be calculated (see red-circled part a in **Figure 31**). It is suggested to maximize window usage (best case up to 100%).

- Manufacturability Check

Based on the total wire and tape layers of each winding with corresponding wire and tape thickness, the total build thickness is calculated. If it is less than the bobbin depth, the manufacturability check shows “OK”, else “NG” (see red-circled part b in **Figure 31**). Please note that this manufacturability check is just based on theoretical calculation, so it is important to confirm the manufacturability in actual production environment with the transformer supplier based on the auto-generated transformer drawing (see **section 3.2.9**)

User guide

• Build Information

If the manufacturability check is “OK”, the unused depth (in mm and percentage of bobbin depth) will be shown (see red-circled part c in **Figure 31**). If the manufacturability check is “NG”, for example, if the build thickness is 5 mm but the bobbin depth is 4 mm, the build information will show “ERROR! Build too thick(120% of Bobbin Depth used)”. For an optimized transformer design, the unused bobbin depth should not be too high.

• Conduction and Core Loss Percentage

The flux density and current density input fine-tuning should minimize the conduction and core losses of part d in **Figure 31**. This calculation does not include losses from other main components like the MOSFET and diode.

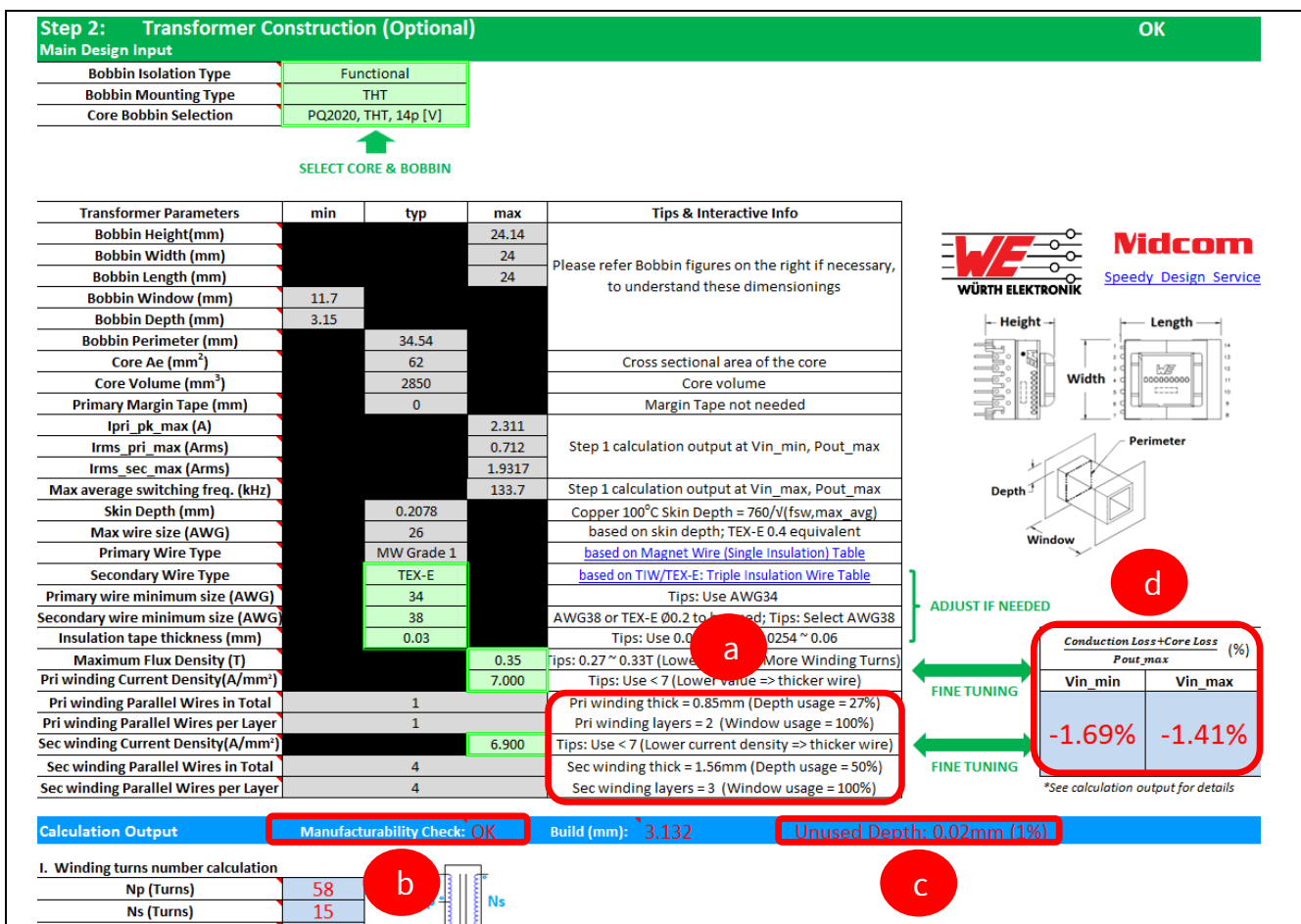


Figure 31 Guide information for fine-tuning of maximum flux density and current density

3.2.6 Calculation output for number of winding turns

In step 2 section I (see **Figure 32**), the number of winding turns for **Np** is calculated using the equation below:

$$N_p = \frac{L_p * I_{pri_pk_max}}{A_e * B_{max}}$$

Where

L_p: Primary inductance

I_{pri_pk_max}: Maximum primary peak current

B_{max}: Maximum flux density

User guide

Ae: Effective core area

The absolute number of winding turns for **Ns**, **Na** and **Nsec_aux** will then be calculated based on the **Np/Ns**, **Na/Ns** and **Nsec_aux/Ns** selection from step 1.

Calculation Output		Manufacturability Check: OK	Build (mm): 3.132	Unused Depth: 0.02mm (1%)
I. Winding turns number calculation				
Np (Turns)	58			
Ns (Turns)	15			
Na (Turns)	15			
Nsec_aux (Turns)	15			

Figure 32 Calculation of number of winding turns (Step 2 Calculation output I)

3.2.7 Winding turns ratio check and comparison

Despite using the step 1 design input turns ratio to calculate the absolute number of winding turns for **Ns**, **Na** and **Nsec_aux** in the calculation output section I, the ratios of turns (based on the step 2 transformer construction) might vary due to limited ratio combinations. Therefore, the ratios of winding turns can be checked and compared in calculation output section II, as shown in **Figure 33**.

II. Winding Turns Ratio Check			
	Step 2 Calculation	Step 1 Design Input	Calculation Output vs Design Input might vary due to windings limited integers ratio combination. Pls do fine tuning in Step 1 Design input if needed
Np/Ns	3.867	3.870	
Na/Ns	1.000	1.02	
Nsec_aux/Ns	1.000	0.98	

Figure 33 Check and compare ratio of winding turns (Step 2 Calculation output II)

3.2.8 Estimated transformer losses

The transformer losses are calculated for the following two conditions:

- Vin_min, Pout_max (calculation output section III in **Figure 34**)
- Vin_max, Pout_max (calculation output section IV in **Figure 34**)

III. Transformer Loss Calculation (Vin_min, Pout_max)				IV. Transformer Loss Calculation (Vin_max, Pout_max)			
Pri winding est. conduction loss (W)	0.301	[Rdc(100°C) ≈ 0.59Ω]		Pri winding est. conduction loss (W)	0.097	[Rdc(100°C) ≈ 0.59Ω]	
Sec winding est. conduction loss (W)	0.207	[Rdc(100°C) ≈ 0.06Ω]		Sec winding est. conduction loss (W)	0.207	[Rdc(100°C) ≈ 0.06Ω]	
Est. Total conduction loss (W)	0.508			Est. Total conduction loss (W)	0.304		
Est. Total Core Loss (W)	0.160	[Pcv(100°C) ≈ 56.23mW/cm³]		Est. Total Core Loss (W)	0.253	[Pcv(100°C) ≈ 88.73mW/cm³]	
Total Loss / Pout_max (%)	-1.69%			Total Loss / Pout_max (%)	-1.41%		

Figure 34 Estimated transformer losses (Step 2 Calculation output sections III & IV)

The following calculated outputs are generated for each section or condition.

- Primary winding estimated conduction loss

$$= I_{pri_rms}^2 \times Rdc_pri(100^\circ C) \quad [\text{unit: W}]$$

$$Rdc_pri(100^\circ C) = \frac{\rho_{copper}(100^\circ C) \times l_{pri}}{N_{total(pri)} \times A_{wire(pri)}} \quad [\text{unit: } \Omega]$$

where:

$$\rho_{copper}(100^\circ C) = 2.22 \times 10^{-8} \quad [\text{unit: } \Omega m]$$

$$l_{pri} = N_p \times \{bobbin\ perimeter + (bobbin\ depth \times 4)\} \quad [\text{unit: m}]$$

User guide

$N_{total(pri)}$ = number of primary parallel wires in total

$A_{wire(pri)}$ = conductor cross section area of each primary parallel wire [unit: m²]

Secondary winding estimated conduction loss

$= I_{sec_rms}^2 \times Rdc_sec(100^\circ C)$ [unit: W]

$Rdc_sec(100^\circ C) = \frac{\rho_{copper(100^\circ C)} \times l_{sec}}{N_{total(sec)} \times A_{wire(sec)}}$ [unit: Ω]

Where:

$\rho_{copper(100^\circ C)} = 2.22 \times 10^{-8}$ [unit: Ωm]

$l_{sec} = N_s \times \{bobbin\ perimeter + (bobbin\ depth \times 4)\}$ [unit: m]

$N_{total(sec)}$ = number of secondary parallel wires in total

$A_{wire(sec)}$ = conductor cross section area of each secondary parallel wire [unit: m²]

Estimated total conduction loss

$= I_{pri_rms}^2 \times Rdc_pri(100^\circ C) + I_{sec_rms}^2 \times Rdc_sec(100^\circ C)$ [unit: W]

Estimated total core loss

$= Pcv_{100^\circ C, PC44} \times core\ volume$ [unit: W]

$Pcv_{100^\circ C, PC44} = \frac{1}{\pi} \times \int_{\theta=0}^{\pi} 6.674 \times 10^{-7} \times f_{sw}(\theta)^{1.412} \times B(\theta)^{2.567} d\theta$

where:

$f_{sw}(\theta)$ = switching frequency of AC input sine phase angle

$B(\theta)$ = flux density of AC input sine phase angle

Total loss percentage over Pout_max

$= \frac{Est.\ conduction\ loss + core\ loss}{Pout_max} \times 100\%$

3.2.9 Auto-generated transformer drawing

If no error is found in both steps 1 and 2, a transformer drawing will be generated, as shown in **Figure 35**.

Please note that it is still necessary for the user to input the transformer pin assignment (see the light-green cells in **Figure 35**) based on the board schematic and PCB layout design to finalize the transformer drawing.

10	Step 1: System Simulation & Transformer Design	OK
73		
105	Step 2: Transformer Construction (Optional)	OK
165		
166	Generate: TRANSFORMER DRAWING	OK
254		
255	Step 3: Finalize System Design	OK
298		
324	Generate: BOM & IC PARAMETERS	OK
1001		

Step 3: Finalize System Design					OK
Main Design Input					
Parameters	min	typ	max	Tips & Interactive Info	
CS Resistor Preference	Lower Power Dissipation			Higher R _{CS} (Output accuracy) or Lower R _{CS} (Power Dissipation)	
Transformer Leakage Inductance (%)		0.5%		Leakage Inductance / Primary Inductance x 100%	ADJUST IF NEEDED
Output Bleeder Selection	Active (Auto-Discharge Circuit)			Active bleeder discharge output fast if no switching (no loss in normal op.); Passive bleeder discharge output slower (low loss in normal op.)	
EN_DIM_TO_OFF setting	Disabled			Dim To Off (Enabled/Disabled?) Note: Active voltage source needed to exit dim-to-off.	

Figure 37 CS resistor preference (Step 3 Main design input)

3.3.2 Transformer leakage inductance percentage input

The **Transformer Leakage Inductance** (in percentage) over primary inductance needs to be input by the user for RCD snubber design calculation (see [Section 3.3.7](#)). The value of a typical design would be around 1%. The user can select a value of 0.5%, 1.0%, 1.5%, 2.0%, 2.5% or 3.0%.

Step 3: Finalize System Design					OK
Main Design Input					
Parameters	min	typ	max	Tips & Interactive Info	
CS Resistor Preference	Lower Power Dissipation			Higher R _{CS} (Output accuracy) or Lower R _{CS} (Power Dissipation)	
Transformer Leakage Inductance (%)		0.5%		Leakage Inductance / Primary Inductance x 100%	ADJUST IF NEEDED
Output Bleeder Selection	Active (Auto-Discharge Circuit)			Active bleeder discharge output fast if no switching (no loss in normal op.); Passive bleeder discharge output slower (low loss in normal op.)	
EN_DIM_TO_OFF setting	Disabled			Dim To Off (Enabled/Disabled?) Note: Active voltage source needed to exit dim-to-off.	

Figure 38 Transformer leakage inductance percentage (Step 3 Main design input)

3.3.3 Output bleeder selection input

Selection of an output bleeder is mandatory for flyback primary side control to ensure the output will not be over-charged under no-load condition (e.g. LED not connected). There are two options available:

- Active (auto-discharge circuit)

An output will only be discharged by the bleeder resistor when transformer switching is stopped (e.g. during AC-off or dim-to-off). The component count is higher but there is no drop in efficiency and fast discharge occurs with low bleeder resistances.

- Passive (dummy resistor)

An output will be always discharged by a dummy resistor connected in parallel with output LEDs. The component count is the lowest but there is a slight drop in efficiency and slow discharge with high bleeder resistances.

Step 3: Finalize System Design					OK
Main Design Input					
Parameters	min	typ	max	Tips & Interactive Info	
CS Resistor Preference	Lower Power Dissipation			Higher R _{CS} (Output accuracy) or Lower R _{CS} (Power Dissipation)	
Transformer Leakage Inductance (%)		0.5%		Leakage Inductance / Primary Inductance x 100%	ADJUST IF NEEDED
Output Bleeder Selection	Active (Auto-Discharge Circuit)			Active bleeder discharge output fast if no switching (no loss in normal op.); Passive bleeder discharge output slower (low loss in normal op.)	
EN_DIM_TO_OFF setting	Disabled			Dim To Off (Enabled/Disabled?) Note: Active voltage source needed to exit dim-to-off.	

Figure 39 Output bleeder selection (Step 3 Main design input)

3.3.4 Dim-to-off setting input

The ICL8105 allows dim-to-off operation but it requires an active voltage source to exit from dim-to-off.

The **EN_DIM_TO_OFF** setting allows users to enable/disable such operations but it is strongly recommended to enable it only when the application design is for primary side dimming and an external Vcc supply. Therefore, step 3 will show a warning if this setting is enabled but the step 1 design inputs (**I_{out} Dimming** and **Vcc supply source**) do not meet these two requirements.

Step 3: Finalize System Design				OK
Main Design Input				
Parameters	min	typ	max	Tips & Interactive Info
CS Resistor Preference	Higher Output accuracy			Higher R _{CS} (Output accuracy) or Lower R _{CS} (Power Dissipation)
Transformer Leakage Inductance (%)		1.0%		Leakage Inductance / Primary Inductance x 100%
Output Bleeder Selection	Active (Auto-Discharge Circuit)			Active bleeder fast discharge output if no switching (no loss in normal state); Passive bleeder is slow discharge resistor (low loss in normal state)
EN_DIM_TO_OFF setting	Disabled			Dim To Off (Enabled/Disabled?) Note: Active voltage source needed to exit dim-to-off.

Figure 40 Dim-to-off setting (Step 3 Main design input)

3.3.5 CS pin-related design calculation

In step 3 section I, the user has to decide on an **R_{CS} Selection** or CS shunt resistor selection (see red-circled part in [Figure 41](#)). The selection value should be between the calculation outputs for **Min R_{CS}** and **Max R_{CS}**.

I_{OCP1} refers to transformer primary winding current which triggers input overcurrent protection level 1. It is automatically set to the maximum of **I_{pri_pk}** (from Step 1 calculation output section I).

If **CS Resistor Preference** is set to “higher output accuracy”,

$$\text{Min } R_{CS} = \frac{0.98}{I_{OCP1}} \quad \text{Max } R_{CS} = \frac{1.08}{I_{OCP1}} \quad [\text{unit: } \Omega]$$

$$V_{OCP1} = R_{CS} \text{ Selection} \times I_{OCP1} \quad [\text{unit: V}]$$

$$V_{OCP2} = 1.6 \quad [\text{unit: V}]$$

If **CS Resistor Preference** is set to “lower power dissipation”,

$$\text{Min } R_{CS} = \frac{0.49}{I_{OCP1}} \quad \text{Max } R_{CS} = \frac{0.54}{I_{OCP1}} \quad [\text{unit: } \Omega]$$

$$V_{OCP1} = R_{CS} \text{ Selection} \times I_{OCP1} \quad [\text{unit: V}]$$

$$V_{OCP2} = 0.8 \quad [\text{unit: V}]$$

Note: **V_{OCP1}** refers to the CS resistor voltage threshold setting for input overcurrent protection level 1.

V_{OCP2} refers to the CS resistor voltage threshold setting for input overcurrent protection level 2.

R_{CS} Selection Max Power Loss refers to the maximum power loss calculation based on the R_{CS} Selection input by the user. The equation is as shown below:

$$P_{\text{loss,max}(R_{CS})} = I_{\text{pri_rms}}^2 \times R_{CS} \text{ Selection} \quad [\text{unit: W}]$$

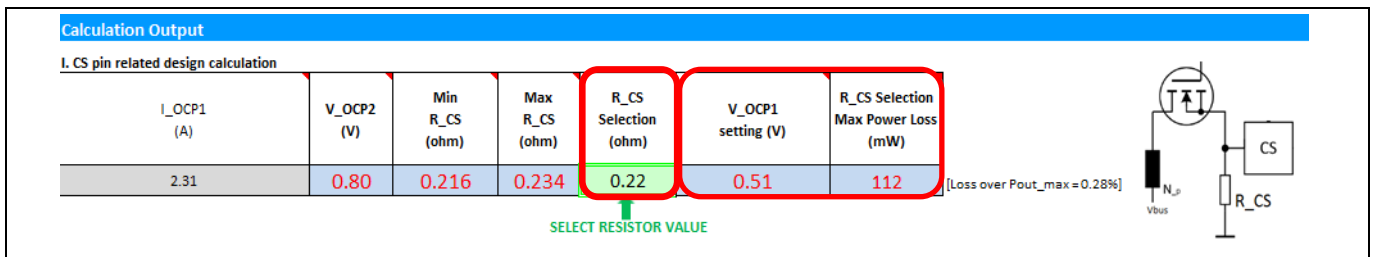


Figure 41 CS pin-related design calculation (Step 3 Calculation output I)

3.3.6 ZCD pin-related design calculation

In step 3 section II, the user has to decide on the R_ZCD_1 selection and R_ZCD_2 selection (see the red-circled part in [Figure 42](#)).

R_ZCD_1 Selection should be between the calculation outputs for **Min R_ZCD_1** and **Max R_ZCD_1**, which are based on the equations below:

$$\text{Min } R_{ZCD_1} = \frac{(V_{in_max} \times 107\%) \times \sqrt{2} \times \frac{N_a}{N_p} - 0.22}{3} \quad [\text{unit: k}\Omega]$$

$$\text{Max } R_{ZCD_1} = \frac{(V_{in_max} \times 107\%) \times \sqrt{2} \times \frac{N_a}{N_p} - 0.15}{1.9} \quad [\text{unit: k}\Omega]$$

Note: The highest value for Max R_ZCD_1 is 100 kΩ. If input OVP is enabled, Vin_max in the equations will be replaced by V_inOV typical value.

R_ZCD_2 Selection should be between the calculation outputs for **Min R_ZCD_2** and **Max R_ZCD_2**, which are based on the equations below:

$$\text{Min } R_{ZCD_2} = \frac{R_{ZCD_1 \text{ Selection}}}{(V_{outOV_max} \times \frac{N_a}{N_s} \div 1.9) - 1} \quad [\text{unit: k}\Omega]$$

$$\text{Max } R_{ZCD_2} = \frac{R_{ZCD_1 \text{ Selection}}}{(V_{outOV_max} \times \frac{N_a}{N_s} \div 2.3) - 1} \quad [\text{unit: k}\Omega]$$

R_ZCD_1 Selection Max Power Loss refers to the maximum power loss calculation based on the **R_ZCD_1 Selection** input by the user.

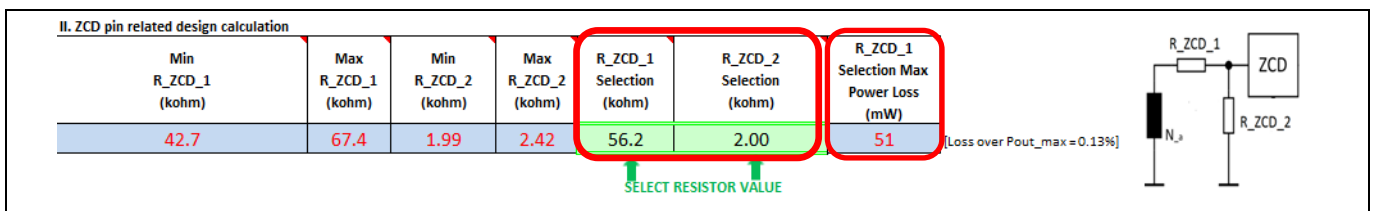


Figure 42 ZCD pin-related design calculation (Step 3 Calculation output II)

3.3.7 Primary RCD snubber design calculation

In step 3 section III, the user has to decide on the **Csn Selection** for the primary RCD snubber (see red-circled part in [Figure 43](#)). The primary RCD snubber is to clamp the MOSFET spike voltage, caused by the transformer leakage inductance. Generally, higher Csn values will result in lower Rsn values needed in the RCD snubber design. Please choose a standard capacitor value for **Csn Selection** within the range of 2200 ~ 47000 pF.

L_{p_lk} is calculated by multiplying the **L_p** and **Transformer leakage inductance** percentage inputs.

MOSFET V_{ds_spike} is read-only and refers to the MOSFET drain voltage spike based on the step 1 section VI input.

Recommended Initial R_{sn} for the primary RCD snubber is calculated based on the equation below:

$$R_{sn} = \frac{t_{discharge}}{C_{sn} \cdot \ln\left(\frac{\Delta V_{C_{sn}} - V_{ds_spike}}{V_{ds_spike}}\right)}$$

where:

$$t_{discharge} = \frac{1}{f_{sw}(V_{in_max}, P_{out_max})} - \frac{\pi}{2} \cdot \sqrt{L_{p_lk} \cdot C_{sn}}$$

$$\Delta V_{C_{sn}} = V_{ds_max} - \sqrt{V_{ds_max}^2 - \frac{L_{p_lk} \cdot I_{pri_pk}(V_{in_max}, P_{out_max})^2}{C_{sn}}}$$

$$V_{ds_max} = V_{in_max} \cdot \sqrt{2} + \frac{N_p}{N_s} \cdot V_{out_max} + V_{ds_spike}$$

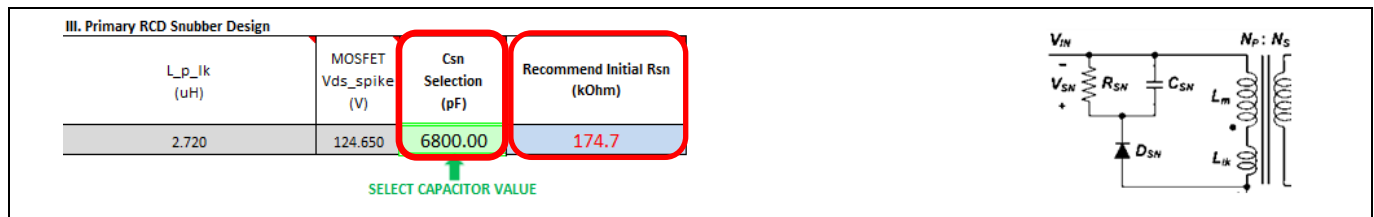


Figure 43 Primary RCD snubber design calculation (Step 3 Calculation output III)

3.3.8 Output bleeder design calculation

Based on the **output bleeder selection** in the step 3 main design input, the user has to make a **bleeder resistor selection**.

As shown in **Figure 44**, there are also design inputs that can be adjusted if needed. These design inputs are placed in this section because they mainly affect the output bleeder design calculation.

- **Reaction_OVP_Vout setting:**

IC parameterization to set the reaction of the output over-voltage protection (selectable value is "Auto-Restart" or "Latch")

- **t_{auto_restart} setting:**

IC parameterization to set the auto restart time for all protections with reaction = "Auto-Restart" and speed of reaction = "Slow" (selectable value is **t_{auto_restart_fast}** ~ 10 sec)

- **t_{auto_restart_fast} setting:**

IC parameterization to set the auto restart time for all protections with reaction = "Auto-Restart" and speed of reaction = "Fast" (selectable value is 0.2 ~ 10 sec)

- **Speed_OVP_Vout setting:**

IC parameterization to set the speed of reaction for the output over-voltage protection (selectable value is "Slow" or "Fast")

User guide

The calculation output below will then be generated:

- Vout OVP auto-restart time:

Output over-voltage protection auto-restart time based on the IC parameterization above.

- Max Bleeder Resistance:

Maximum bleeder resistance calculation output. **Bleeder resistor Selection** should not exceed this value.

IV. Output Bleeder Design - Active						Column M&N	Column O	
Reaction _OVP_Vout setting	t_auto _restart setting (sec)	t_auto _restart_fast setting (sec)	Speed _OVP_Vout setting	Vout OVP auto-restart time (sec)	Max Bleeder Resistance (kΩ)	Bleeder Resistor Selection (kΩ)	Bleeder Resistor selection Est. OVP Vout drop after auto-restart time(V)	Bleeder Resistor OVP auto-restart Est. loss (mW)
Auto-Restart	1.0	0.4	Slow	1.0	5.2	1.3	27.04	985
ADJUST IF NEEDED				SELECT RESISTOR VALUE				

Figure 44 Output bleeder design calculation (Step 3 Calculation output V)

In the column M&N calculation output (see [Figure 44](#)), the tool will then calculate the estimated output voltage drop with the selected bleeder resistor value over a period of time dependent on the **Reaction_OVP_Vout setting**, as shown in [Table 1](#).

Table 1 Calculation output of column M&N based on conditions

Reaction_OVP_Vout setting	Calculation output (column M&N)
Auto-restart	Bleeder Resistor Selection Est. OVP Vout drop after auto-restart time
Latch mode	Bleeder Resistor Selection Est. OVP Vout drop after 3-sec. discharge

In the column O calculation output (See [Figure 44](#)), the estimated loss of the bleeder resistor selection is calculated based on the **Reaction_OVP_Vout setting** and the highest loss condition, as shown in [Table 2](#).

Table 2 Calculation output for column O based on conditions

Reaction_OVP_Vout setting	Est. Loss of Bleeder Resistor Selection		Calculation Output (Column O)
	OVP auto-restart	Normal Operation	
Auto-restart	Higher	Lower	Bleeder Resistor OVP auto-restart Est. Loss
	Lower	Higher	Bleeder Resistor Normal Operation Est. Loss
Latch mode	Not applicable	Any value	

3.3.9 Auto-generated BOM & IC parameters

If the user has completed step 2 with the desired core and bobbin without errors, please **select generate option for T1** as “AUTO GENERATE BASED ON STEP 2” (see [Figure 45](#)).

Otherwise, please select “MANUAL KEY IN” which requires the user to enter **N_p** manually (see [Figure 46](#)).

Note: T1 refers to the reference designator of flyback transformer

ERROR CHECK here will detect if there are any errors in each of the steps. If detected, it will show in which step the error is located and the user should resolve the error or errors accordingly (as shown in [Figure 45](#) with “NO ERROR FOUND”). This is to ensure that the generated BOM and IC parameters are correct.

WARNING CHECK here will detect if there are any warnings in each of the steps. If detected, it will show in which step the warning is located. It is recommended to resolve the warnings (as shown in [Figure 45](#) with “NO WARNING FOUND”) but this is not mandatory. The BOM and IC parameters can still be generated with warnings.

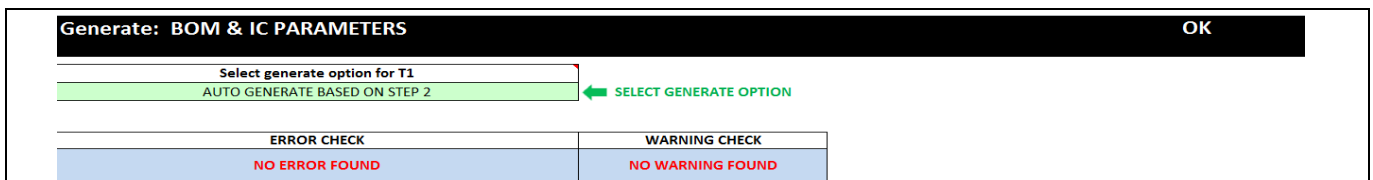


Figure 45 Flyback transformer, T1 parameter-generating option (“AUTO GENERATE BASED ON STEP 2”)

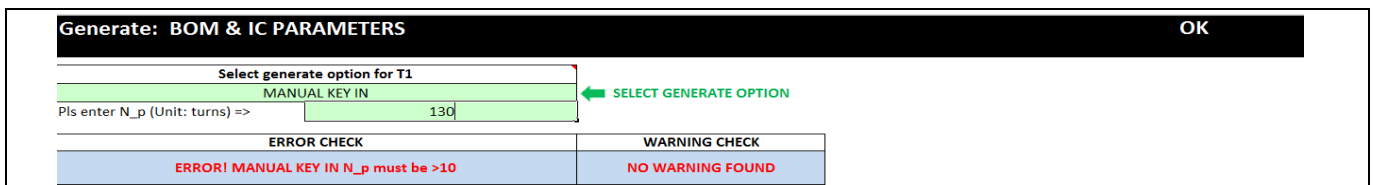


Figure 46 Flyback transformer, T1 parameter-generating option (“MANUAL KEY IN”)

[Figure 47](#) shows an example of the generated BOM and IC parameters.

The BOM reference designators are based on the schematic of ICL8105-CDM10V Reference Design. For easy reference, the schematic is available in the “SCH” worksheet of the excel tool.

By opening the ICL8105 parameterization file (*.csv) with the GUI called .dpVision, user can enter the generated IC parameters from the excel tool and burn these parameters into the IC, using the .dp Interface Board Gen 2.

Please note that there are a few IC parameters which could not be calculated but require fine-tuning at system level. These parameters are as shown in the green-highlighted cell in the IC parameters table in [Figure 47](#). Please refer to the “ICL8105-CDM10V 40W Reference Design Application Note” for the fine-tuning guide.

Also, there are a few IC parameters which are each generated with an initial default value as shown below, instead of dynamically adapted based on the input or output from the design steps before. If necessary, user can adjust each of these parameter values later in .dpVision according to the application needs.

- | | |
|--|-------------------------------|
| • Output current dimming curve, C_DIM: | Quadratic(default) or Linear |
| • Enable output under-voltage protection, EN_UVP_Vout: | Enabled (default) or Disabled |
| • Enable maximum average output current protection, EN_Iout_max_avg: | Enabled (default) or Disabled |
| • Enable maximum peak output current protection, EN_Iout_max_avg: | Enabled (default) or Disabled |
| • Auto restart speed for output current protection, Speed_OCP_Iout: | Slow (default) or Fast |
| • Enable input under-voltage protection, EN_UVP_In: | Enabled (default) or Disabled |

Auto-Generated IC Parameters		
Hardware configuration		
L _{out_reset}	880.0	mA
N _{LP}	58	turns
N _L	15	turns
N _{Lo}	15	turns
L _{LP}	0.544	mH
R _{OS}	0.22	ohm
V _{OCP1}	0.51	V
R _{ZCD_1}	56.2	kohm
R _{ZCD_2}	2.00	kohm
V _{CC_SUPPLY}	Wide	
C _{VCC}	33.00	uF
V _{out_sourcing}	63	V
R _{HW}	66	kohm
L _{GD_pk}	49	mA
Protection		
t _{auto_restart}	1.0	s
t _{auto_restart_fast}	0.4	s
Reaction_OVP_Vout	Auto-Restart	
Speed_OVP_Vout	Slow	
V _{autoOV}	48.4	V
EN_UVP_Vout	Enabled	
t _{start_max}	18.40	ms
EN _{lout_max_avg}	Enabled	
EN _{lout_max_peak}	Enabled	
L _{out_max_peak}	1980	mA
Speed_OCP _{lout}	Slow	
EN_UVP _{ln}	Enabled	
EN_OVP _{ln}	Enabled	
V _{inOV}	329	V
V _{in_restart_max}	329	V
V _{in_restart_min}	72	V
V _{inUV}	62	V
Debug_Mode	Disabled	
Temperature guard		
T _{critical}	119	°C
EN_ITP	Enabled	
T _{hot}	110	°C
L _{out_red}	220	mA
t _{stop}		s
Startup & shutdown		
t _{rr}	0.5	ms
V _{out_dim_min}	11.9	V
V _{out_start}	9.5	V
Control _{loop_init}	DCM	
N _{ABM_init}	100	
Control loop		
PL_KP_QRM	550	
PL_KL_QRM	8	
PL_KL_DCM	17000	
PL_KL_DCM	200	
PL_KP_ABM	64	
PL_KL_ABM	32	
Dimming		
EN_DIM	Enabled	
V _{DIM_min}	0.11	V
L _{out_dim_min}	88.0	mA
C_DIM	Linear	
EN_DIM_TO_OFF	Disabled	
V _{DIM_off}	0.1	V
EN_SQW	Disabled	
Multimode		
f _{sw_max}	180.80	kHz
t _{on_max}	11.3	us
t _{on_min}	1.2	us
f _{sw_min_DCM}	12.00	kHz
EN_ABM	Disabled	
Power Factor Correction		
EN_EPFC	Enabled	
C _{EMI}	0.100	uF
Fine tuning		
t _{min_demaq}	3.0	us
t _{PDC}	250	us
t _{ZCDPD}	410	us
T _{coupling}	1.020	
R _{in}	15	ohm
N _{DCM_mod_gain}	8	
g _{DIM}	0	mV/K

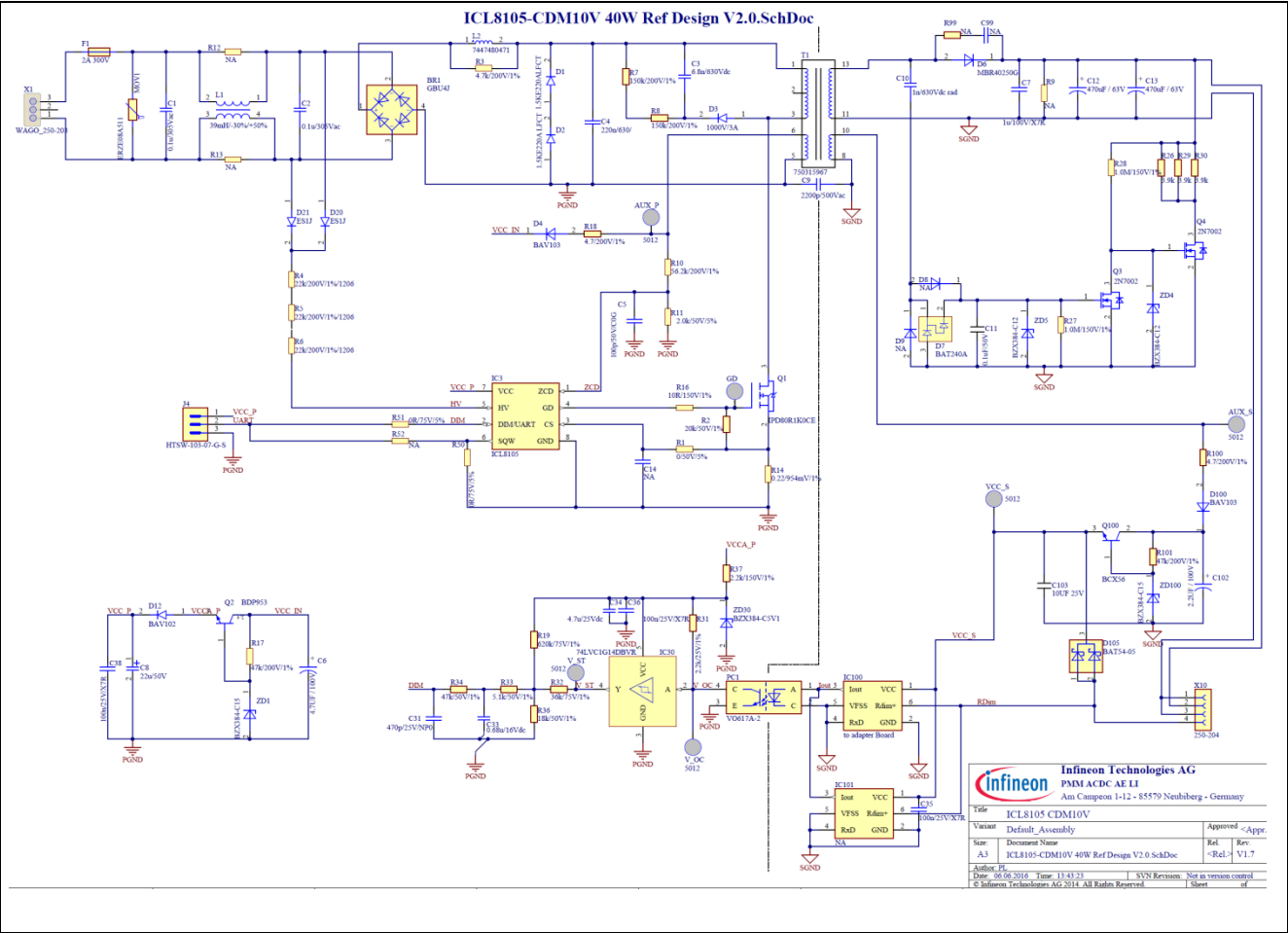


Figure 48 Schematic for the auto-generated BOM (Refer “SCH” Worksheet in the excel tool)

Revision History

Major changes since the last revision

Page or Reference	Description of change

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Edition 2016-03-31

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

AN_201603_PL21_14

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