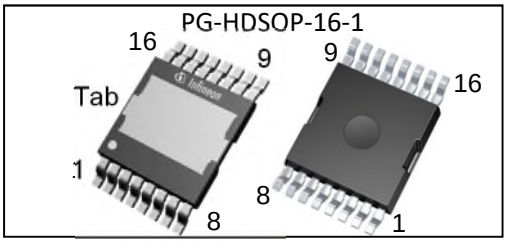
Automotive MOSFET

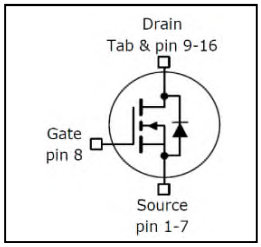
OptiMOS™ 5 Power-Transistor

RoHS Infineon Automotive Quality AEC Qualified



Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – enhancement mode – normal level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- RoHS compliant
- 100% avalanche tested
- Very low reverse recovery charge (Q_{rr})



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	120	V
$R_{DS(on)}$	1.8	mΩ
I_D (chip limited)	309	A

Type	Package	Marking
IAUTN12S5N018T	PG-HDSOP-16-1	5N12N018

Table of Contents

Maximum ratings

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	V_{GS}=10 V, Chip limitation[1,2)]	309	A
		V_{GS}=10V, DC current[3)]	300	
		T_a=100 °C, V_{GS}=10 V, R_{thJA} on top[2,4)]	85	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25 °C, t_p= 100 µs	1150	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=150 A	510	mJ
Avalanche current, single pulse	I_{AS}	–	300	A
Gate source voltage	V_{GS}	–	±20	V
Power dissipation	P_{tot}	T_C=25 °C	358	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	Top	-	-	0.42	K/W
		Bottom (Pin 1-7)	-	9	-	
		Bottom (Pin 9-16)	-	3	-	
Thermal resistance, junction - ambient[4)]	R_{thJA}	Top	-	2.8	-	
		Bottom (through PCB)	-	40	-	

Electrical characteristics

at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(Br)DSS}$	V_{GS}=0 V, I_D=1 mA	120	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=270 µA	2.6	3.1	3.6	
Zero gate voltage drain current	I_{DSS}	V_{DS}=120 V, V_{GS}=0 V, T_j=25 °C	–	0.3	3	µA
		V_{DS}=120 V, V_{GS}=0 V, T_j=100 °C[2)]	–	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=7 V, I_D=50 A	–	2.0	2.8	mΩ
		V_{GS}=10 V, I_D=100 A	–	1.5	1.8	
Gate resistance[2)]	R_G	–	–	1.1	–	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=60 V, f=1 MHz	–	8260	10740	pF
Output capacitance	C_{oss}		–	2369	3080	
Reverse transfer capacitance	C_{rss}		–	45	68	
Turn-on delay time	$t_{d(on)}$	V_{DD}=60 V, V_{GS}=10 V, I_D=100 A, R_G=3.5 Ω	–	28	–	ns
Rise time	t_r		–	55	–	
Turn-off delay time	$t_{d(off)}$		–	45	–	
Fall time	t_f		–	53	–	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=60 V, I_D=100 A, V_{GS}=0 to 10 V	–	43	55	nC
Gate to drain charge	Q_{gd}		–	23	35	
Gate charge total	Q_g		–	111	145	
Gate plateau voltage	$V_{plateau}$		–	5.2	–	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25 °C	–	–	309	A
Diode pulse current[2]	$I_{S,pulse}$	T_C=25 °C, t_p= 100 µs	–	–	1150	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	–	0.85	0.95	V
Reverse recovery time[2]	t_{rr}	V_R=60 V, I_F=50A, di_F/dt =100 A/µs	–	45	67	ns
Reverse recovery charge[2]	Q_{rr}		–	34	68	nC

[1] Practically the current is limited by the overall system design including the customer-specific PCB.

[2] The parameter is not subject to production testing – specified by design.

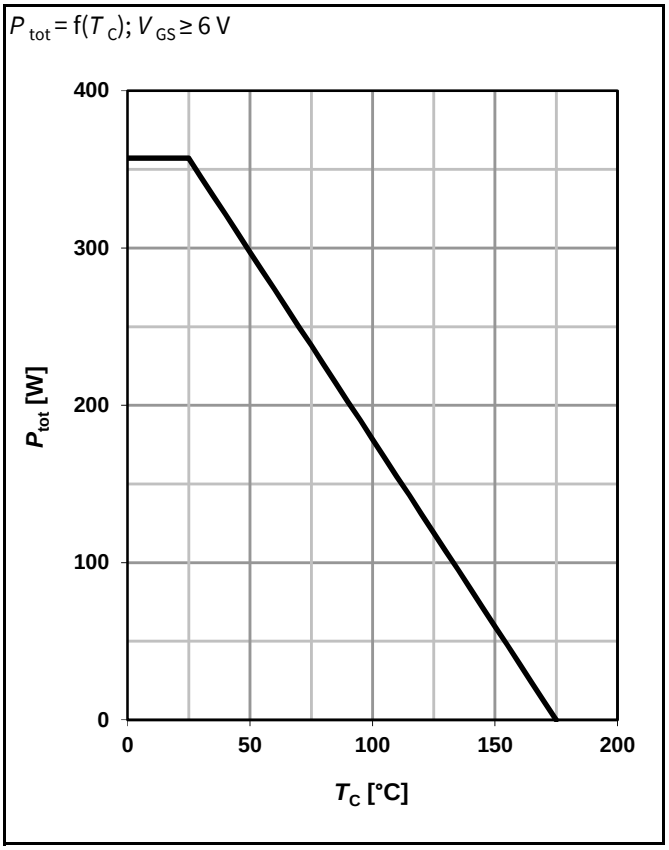
[3] Current is limited by package.

[4] Device on a four-layer 2s2p FR4 PCB with topside cooling. Thermal insulation material is 100 µm thick and has a conductivity of 0.7 W/m/K. Top surface of heat sink is fixed at ambient temperature. Bottom surface of PCB is left at free convection. Values may vary depending on the customer-specific design.

Electrical characteristics diagrams

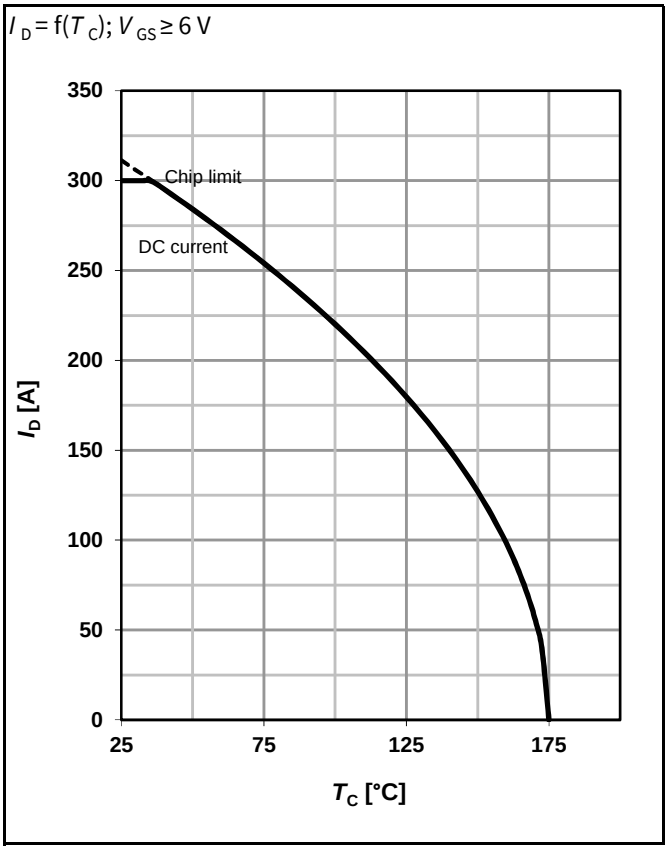
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



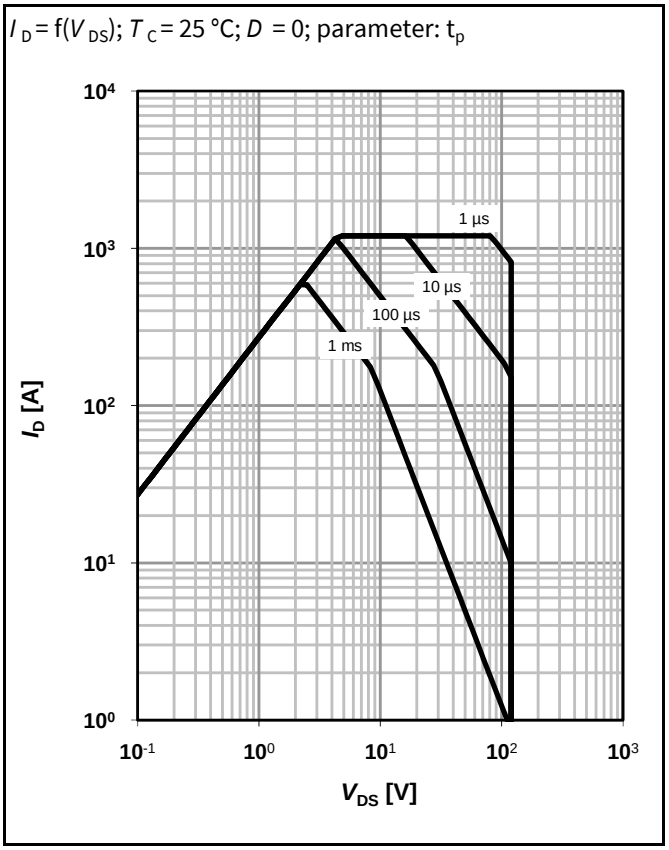
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6$ V



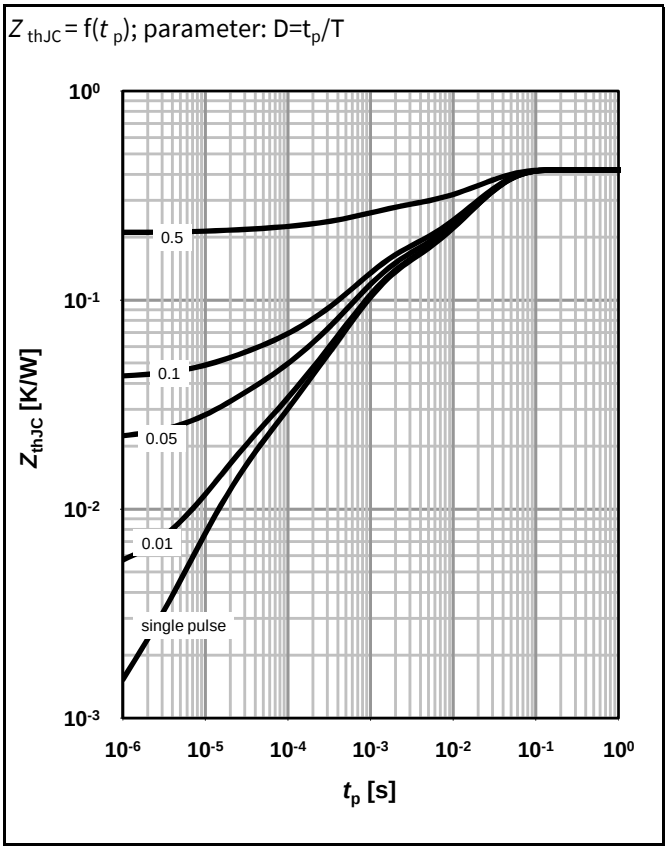
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



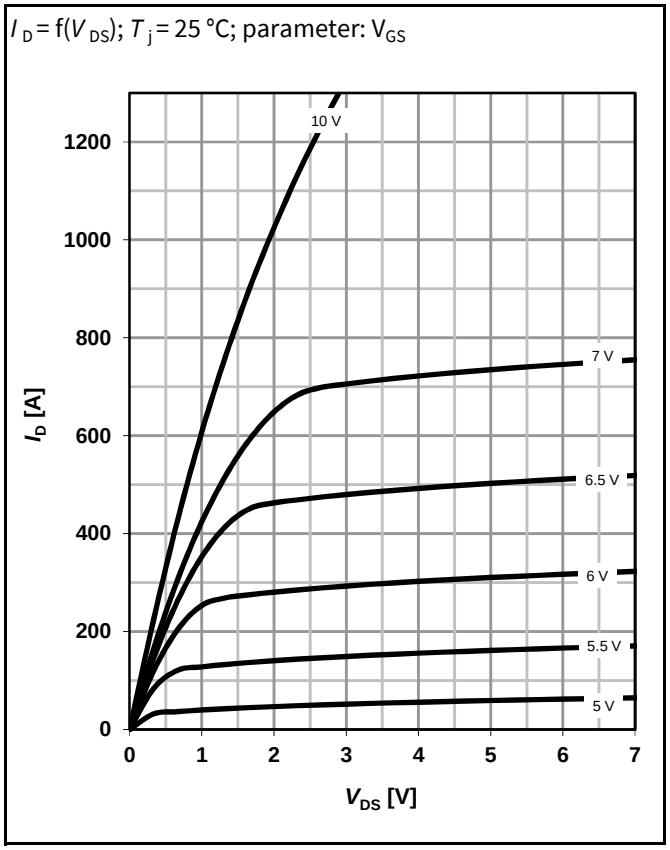
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D=t_p/T$



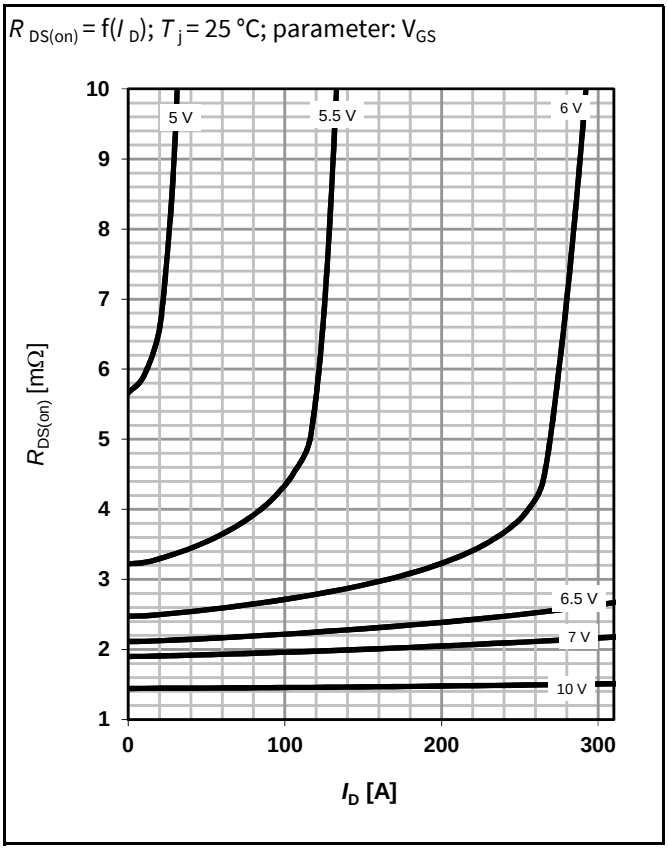
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



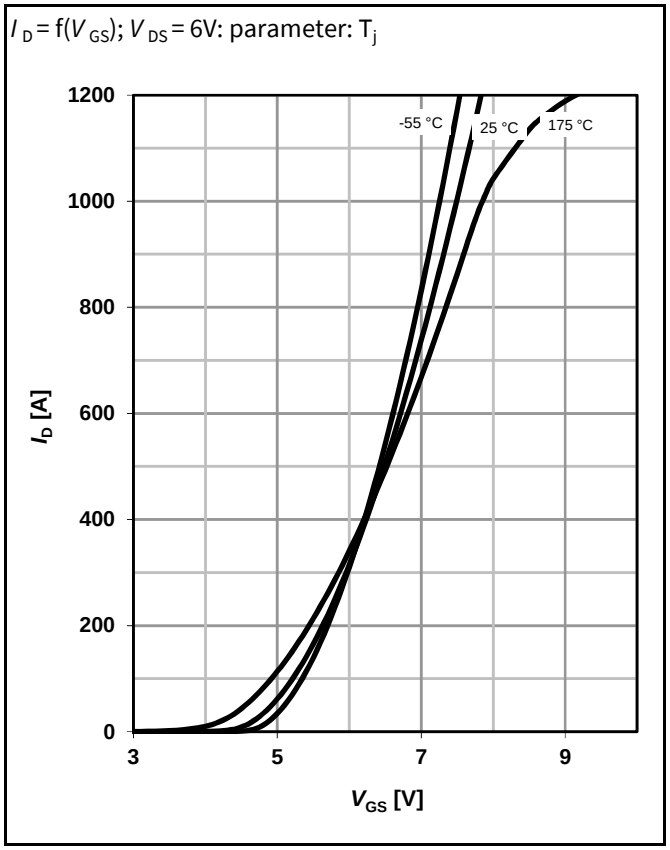
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



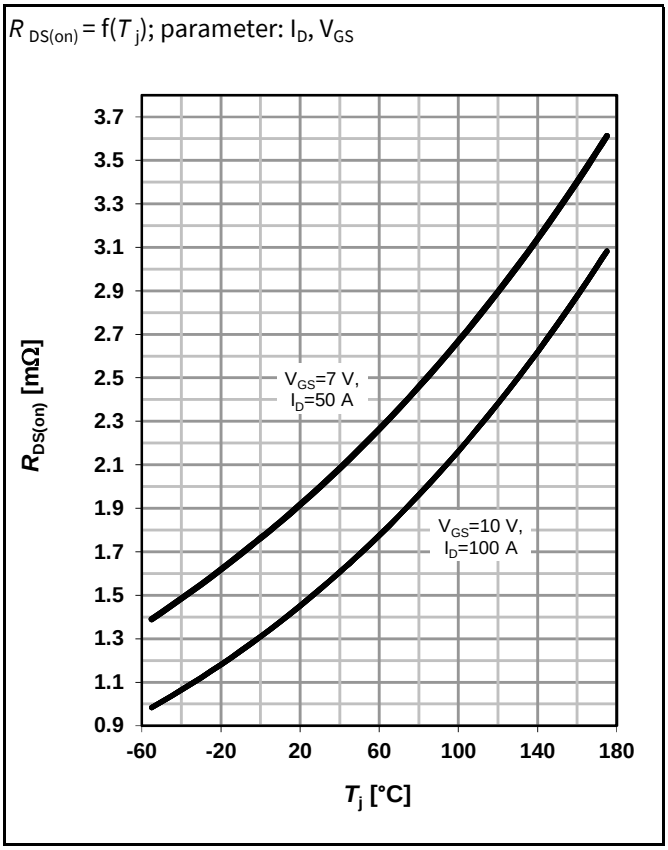
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V: parameter: T_j



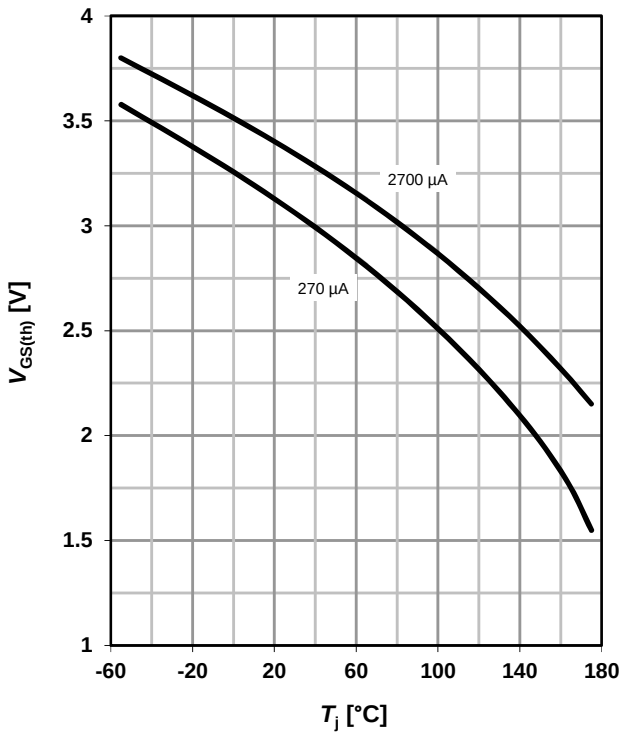
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; parameter: I_D, V_{GS}



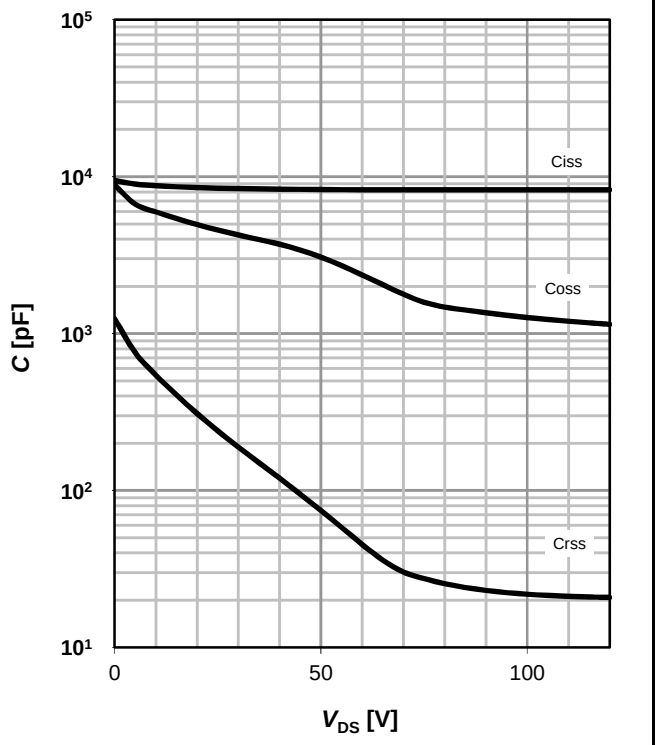
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



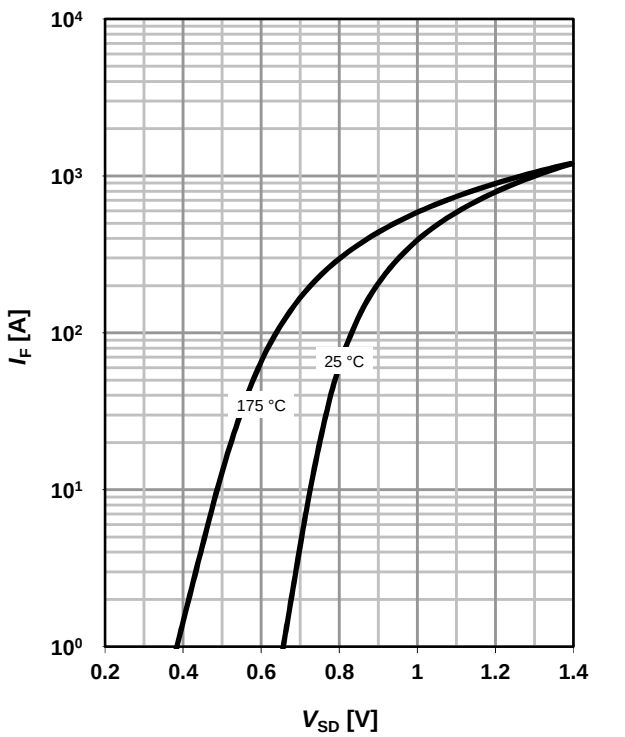
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



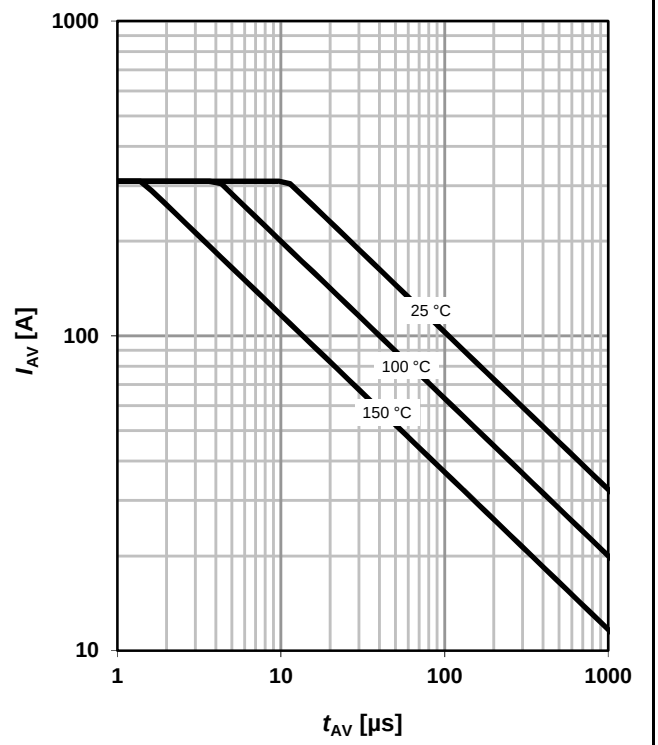
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j

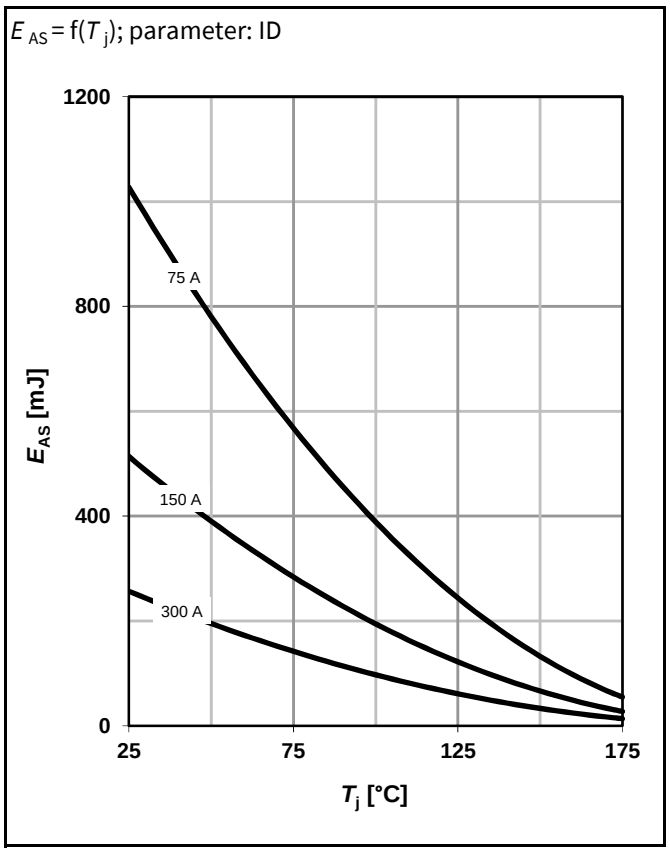


12 Typ. avalanche characteristics

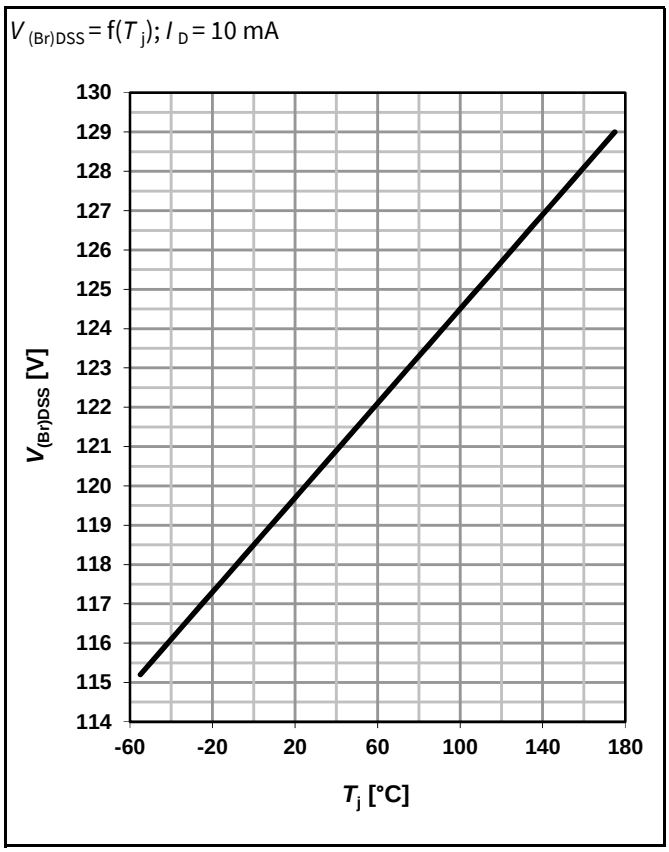
$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



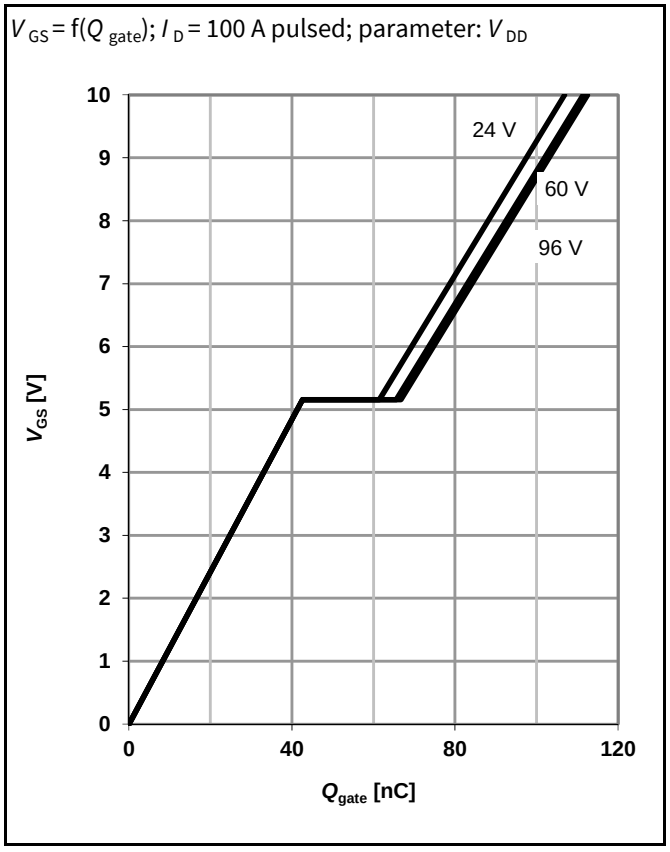
13 Typical avalanche energy



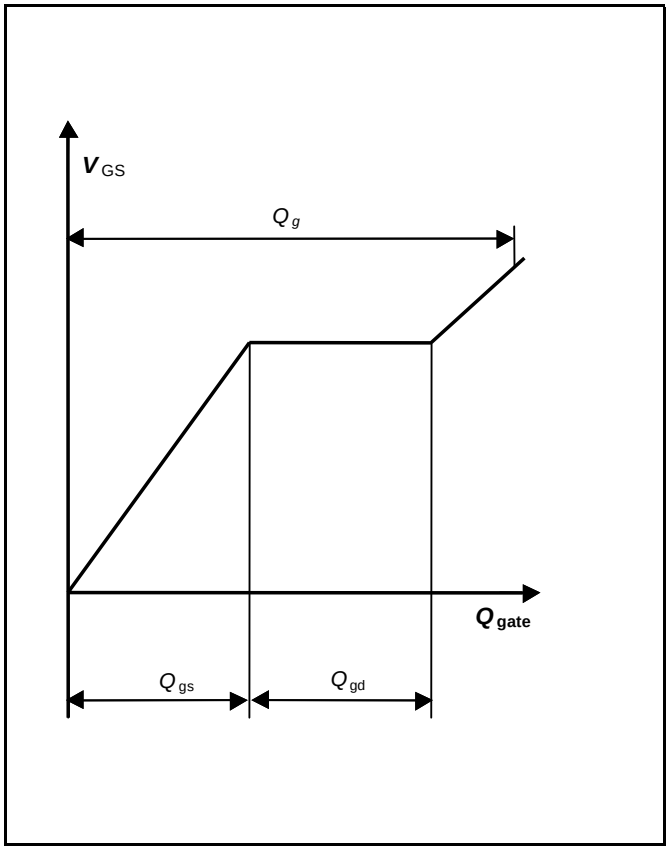
14 Drain-source breakdown voltage



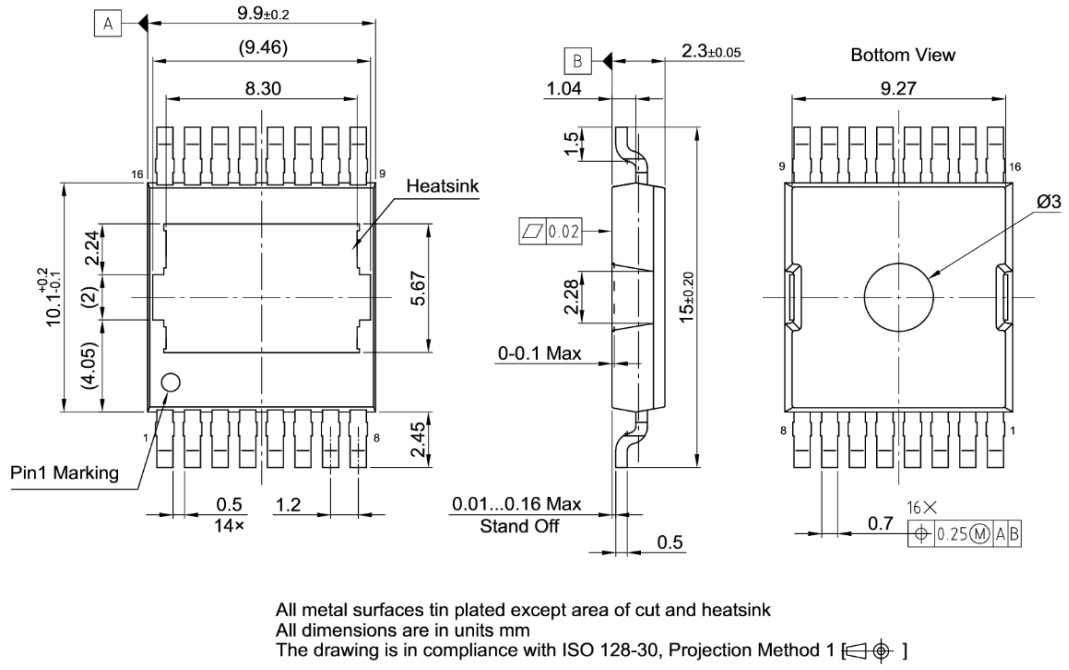
15 Typ. gate charge



16 Gate charge waveforms

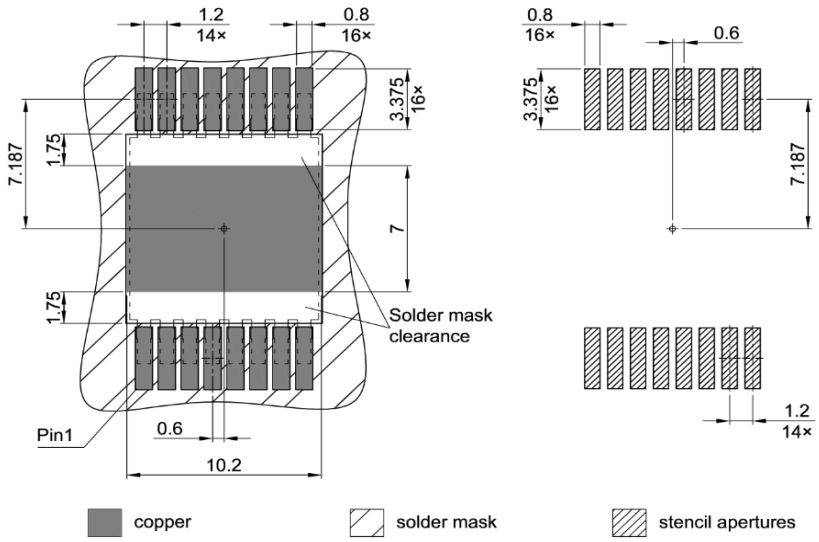


Package Outline



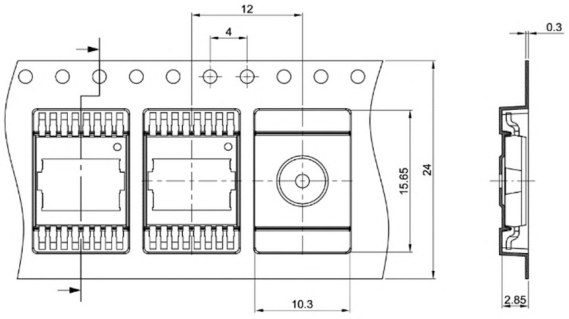
All metal surfaces tin plated except area of cut and heatsink
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Footprint



Based on stencil thickness 0.20 mm
All dimensions are in units mm

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Revision History

Revision	Date	Changes
Revision 1.0	2022-12-15	Final data sheet
Revision 1.01	2023-08-29	Reduced typical on-state resistance $R_{DS(on)}$
Revision 1.10	2024-11-14	Test conditions in graph 14 updated

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