

Automotive MOSFET

OptiMOS™-5 Power-Transistor



Features

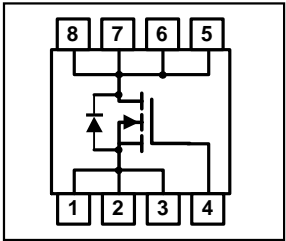
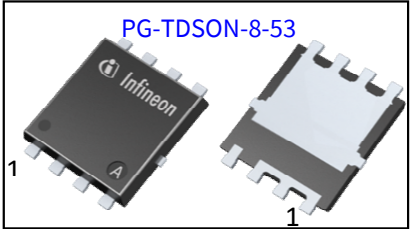
- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Logic Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.



Product Summary

$V_{DS}$	60	V
$R_{DS(on)}$	1.10	mΩ
$I_D$ (chip limited)	310	A

Type	Package	Marking
IAUC120N06S5L011	PG-TDSON-8-53	5N06L011



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## Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$V_{GS}=10\text{ V}$ , Chip limitation <sup>1,2)</sup>	310	A
		$V_{GS}=10\text{ V}$ , DC current <sup>3)</sup>	120	
		$T_a=85\text{ °C}$ , $V_{GS}=10\text{ V}$ , $R_{thJA}$ on 2s2p <sup>2,4)</sup>	39	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$ , $t_p=100\text{ }\mu\text{s}$	1000	
Avalanche energy, single pulse <sup>2)</sup>	$E_{AS}$	$I_D=60\text{ A}$	485	mJ
Avalanche current, single pulse	$I_{AS}$	–	120	A
Gate source voltage	$V_{GS}$	–	$\pm 20$	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	188	W
Operating and storage temperature	$T_j, T_{stg}$	–	$-55 \dots +175$	°C
IEC climatic category; DIN IEC 68-1	–	–	55/175/56	

## Thermal characteristics<sup>2)</sup>

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	$R_{thJC}$	—	—	—	0.80	K/W
Thermal resistance, junction - ambient <sup>4)</sup>	$R_{thJA}$	—	—	26	—	

## Electrical characteristics

at  $T_j=25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$	60	—	—	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=130\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$	—	—	1	$\mu\text{A}$
		$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=100\text{ °C}^{2)}$	—	—	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$	—	—	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}$ , $I_D=60\text{ A}$	—	1.26	1.60	m $\Omega$
		$V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$	—	0.90	1.10	
Gate resistance <sup>2)</sup>	$R_G$	—	—	2.0	—	$\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=30\text{ V}, f=1\text{ MHz}$	–	8770	11400	pF
Output capacitance	$C_{oss}$		–	1580	2050	
Reverse transfer capacitance	$C_{rss}$		–	60	78	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, V_{GS}=10\text{ V}, I_D=60\text{ A}, R_G=3.5\ \Omega$	–	23	–	ns
Rise time	$t_r$		–	26	–	
Turn-off delay time	$t_{d(off)}$		–	72	–	
Fall time	$t_f$		–	19	–	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=30\text{ V}, I_D=60\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	–	25	33	nC
Gate to drain charge	$Q_{gd}$		–	16	24	
Gate charge total	$Q_g$		–	123	160	
Gate plateau voltage	$V_{plateau}$		–	2.9	–	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ °C}$	–	–	120	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	$T_C=25\text{ °C}, t_p=100\ \mu\text{s}$	–	–	1000	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=60\text{ A}, T_J=25\text{ °C}$	–	0.8	1.1	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	–	60	–	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		–	80	–	nC

<sup>1)</sup> Practically the current is limited by the overall system design including the customer-specific PCB.

<sup>2)</sup> The parameter is not subject to production testing – specified by design.

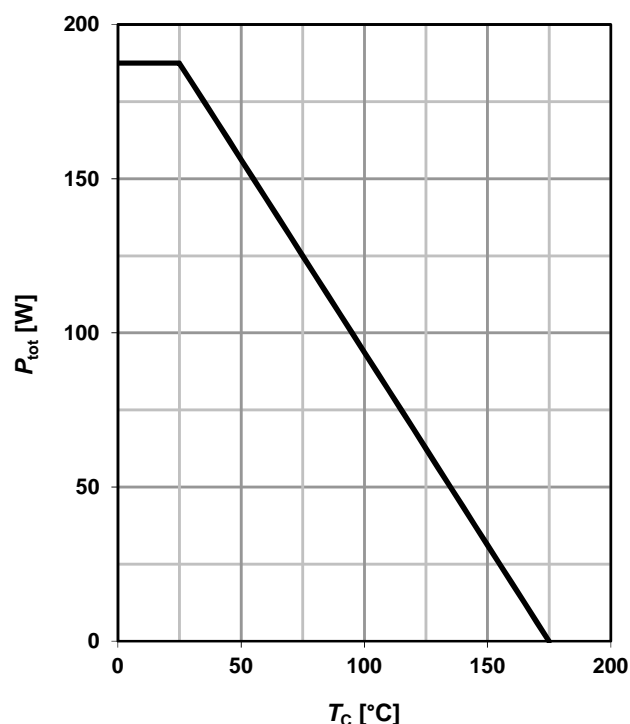
<sup>3)</sup> Current is limited by package.

<sup>4)</sup> Device on 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5, -7). PCB is vertical in still air.

## Electrical characteristics diagrams

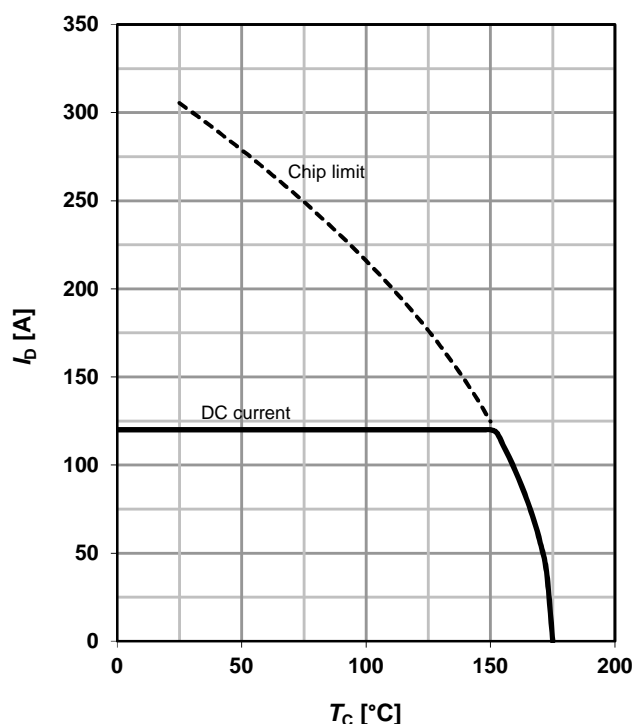
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



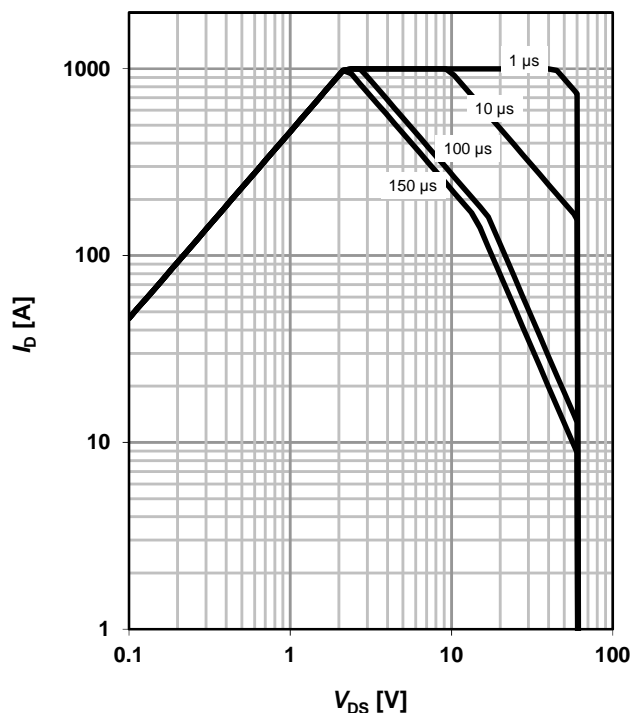
### 2 Drain current

$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



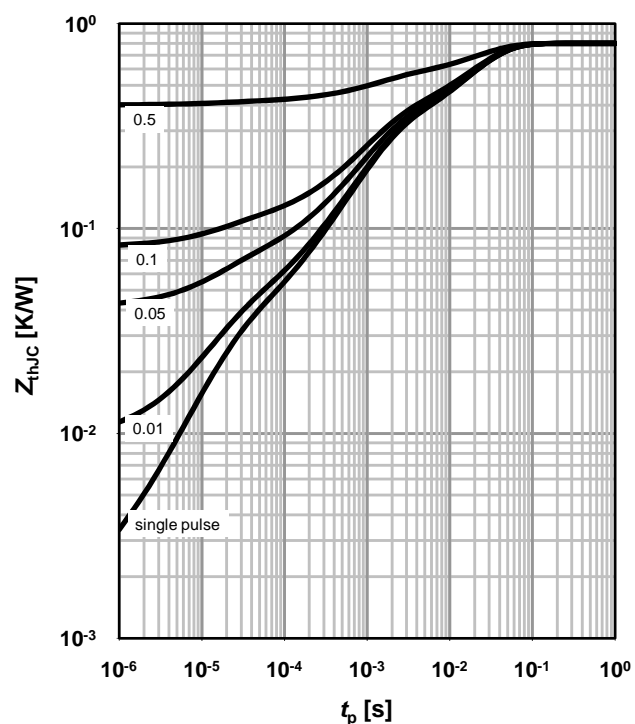
### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0; \text{parameter: } t_p$$



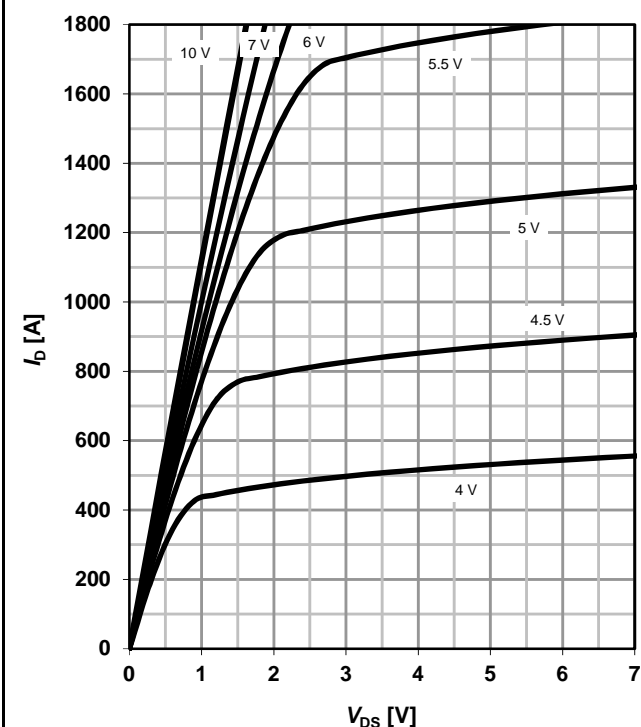
### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p); \text{parameter: } D = t_p/T$$



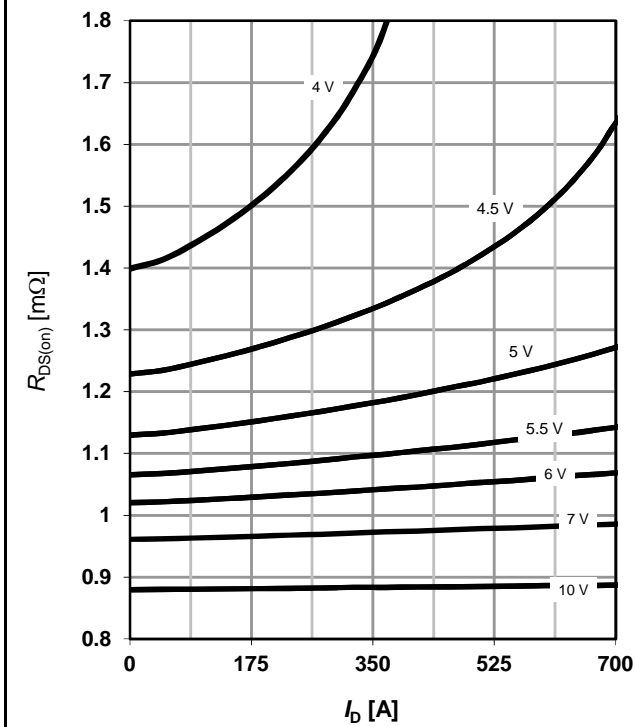
## 5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



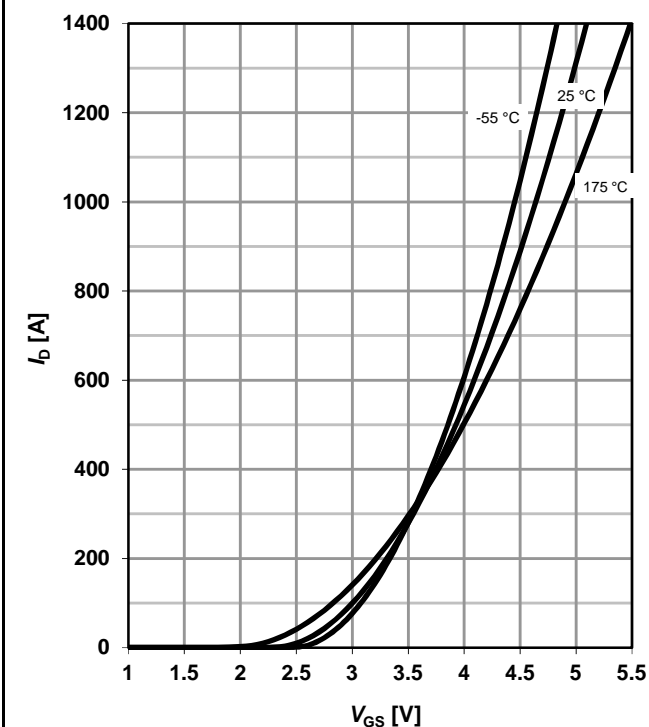
## 6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}; \text{parameter: } V_{GS}$



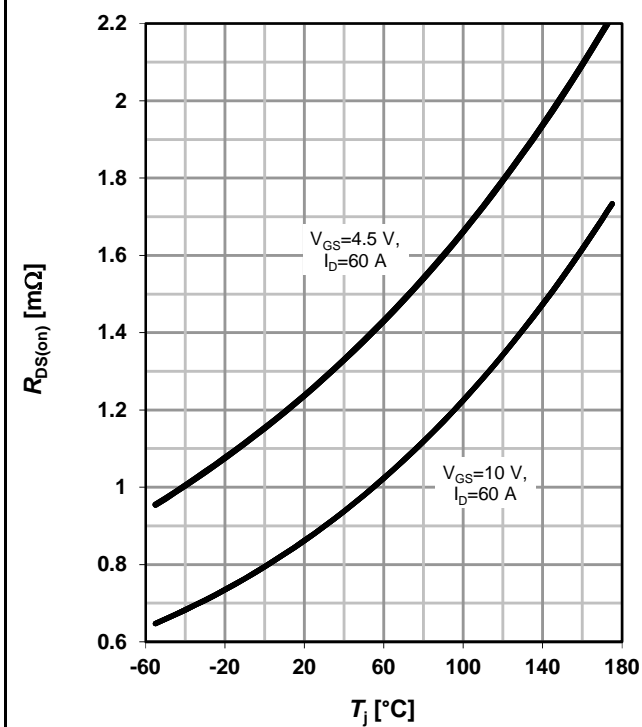
## 7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{ V}; \text{parameter: } T_j$



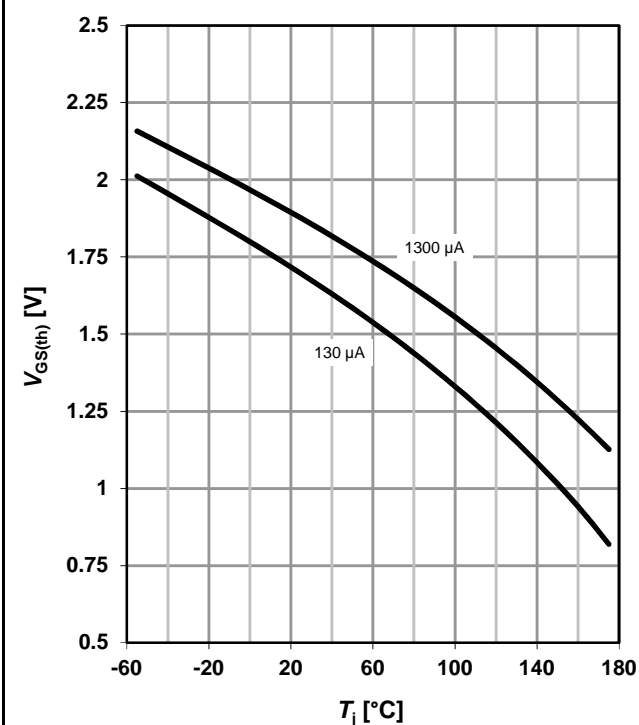
## 8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j); \text{parameter: } I_D, V_{GS}$



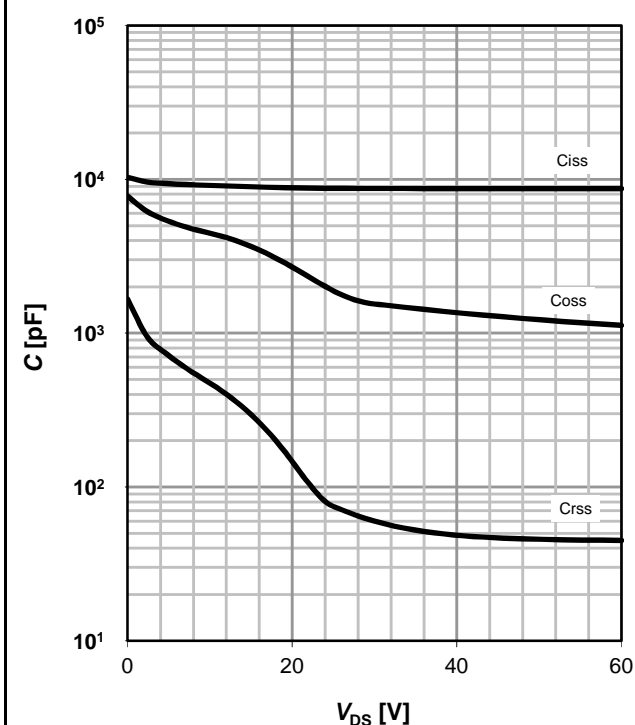
## 9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$ ; parameter:  $I_D$



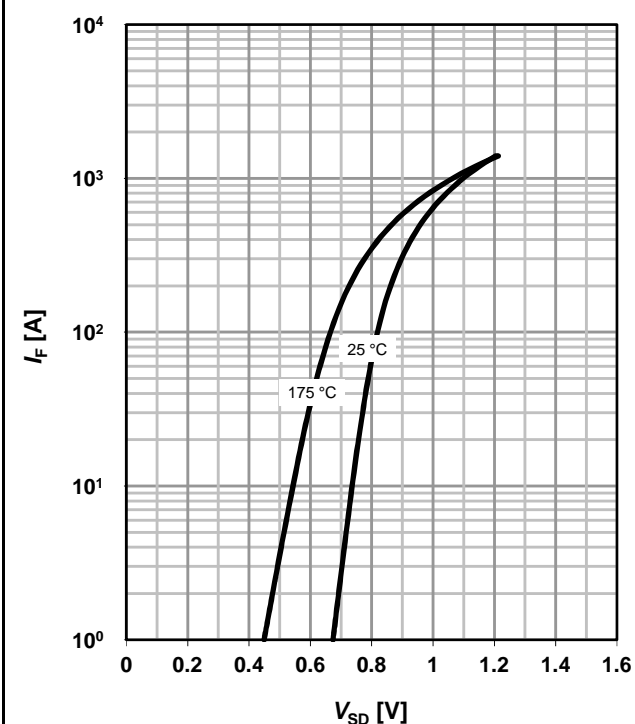
## 10 Typ. capacitances

$C = f(V_{DS})$ ;  $V_{GS} = 0 V$ ;  $f = 1 MHz$



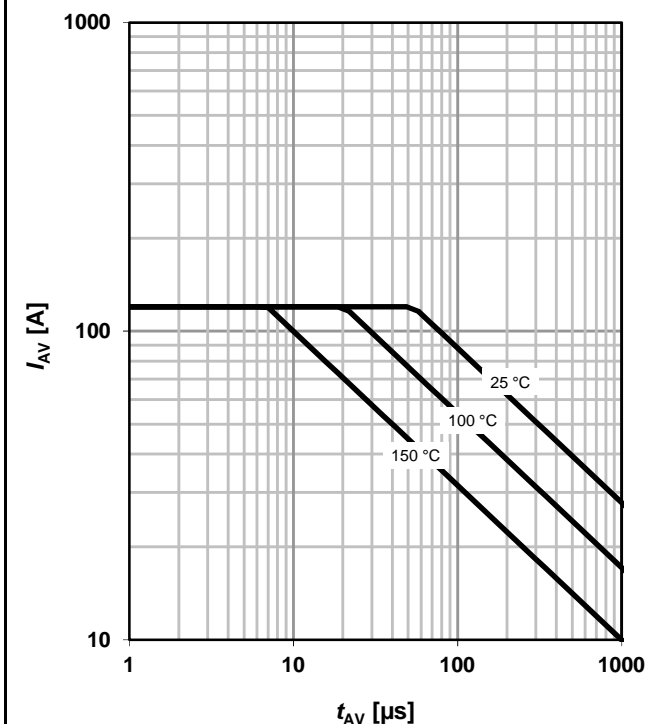
## 11 Typical forward diode characteristics

$I_F = f(V_{SD})$ ; parameter:  $T_j$



## 12 Typ. avalanche characteristics

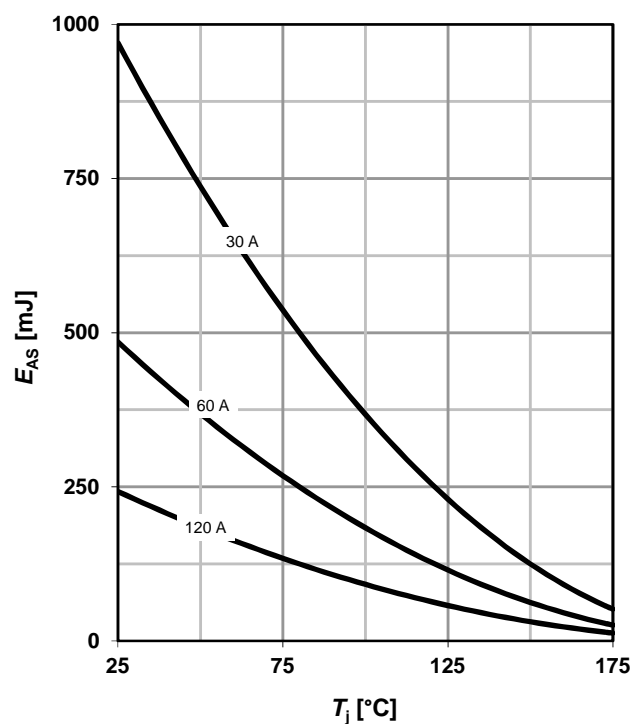
$I_{AS} = f(t_{AV})$ ; parameter:  $T_{j(start)}$





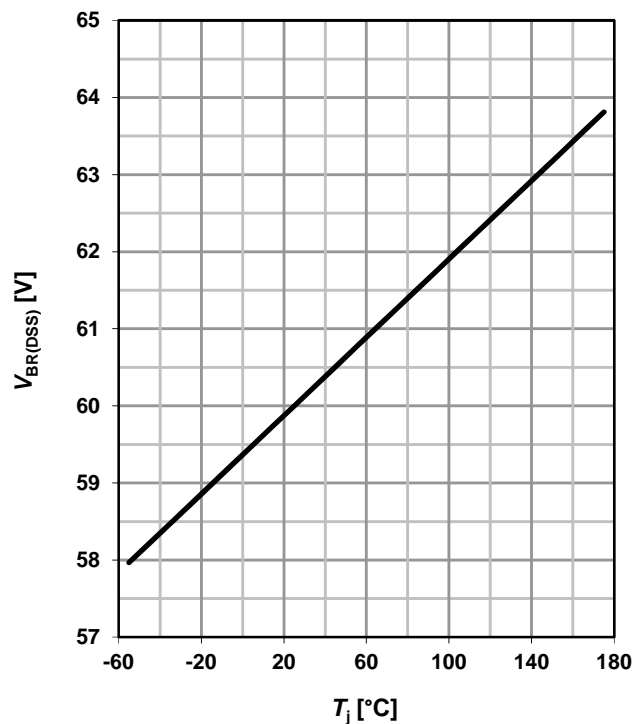
## 13 Typical avalanche energy

$E_{AS} = f(T_j)$ ; parameter:  $I_D$



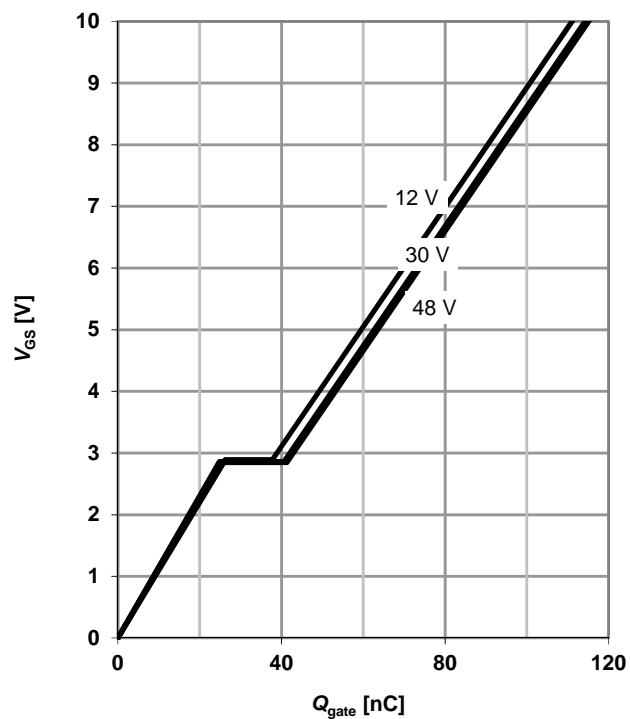
## 14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$ ;  $I_{D\_typ} = 1$  mA

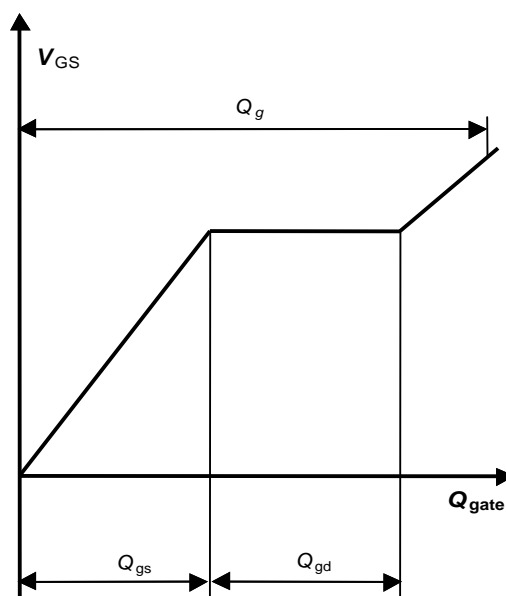


## 15 Typ. gate charge

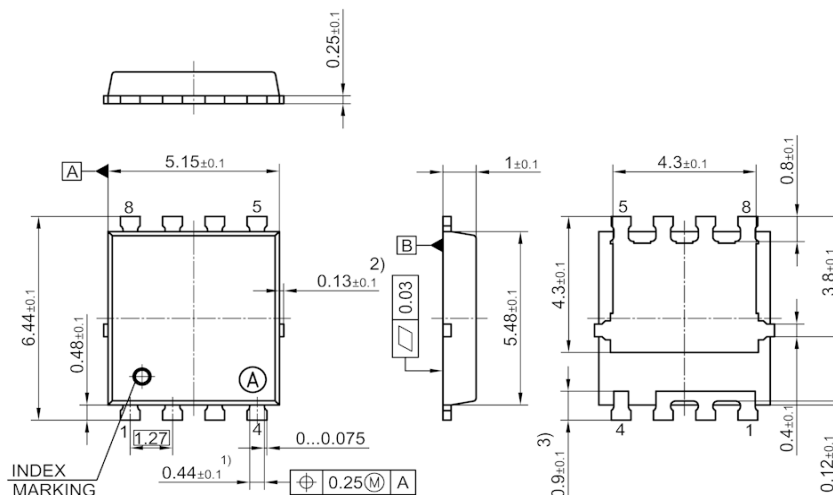
$V_{GS} = f(Q_{gate})$ ;  $I_D = 60$  A pulsed; parameter:  $V_{DD}$



## 16 Gate charge waveforms

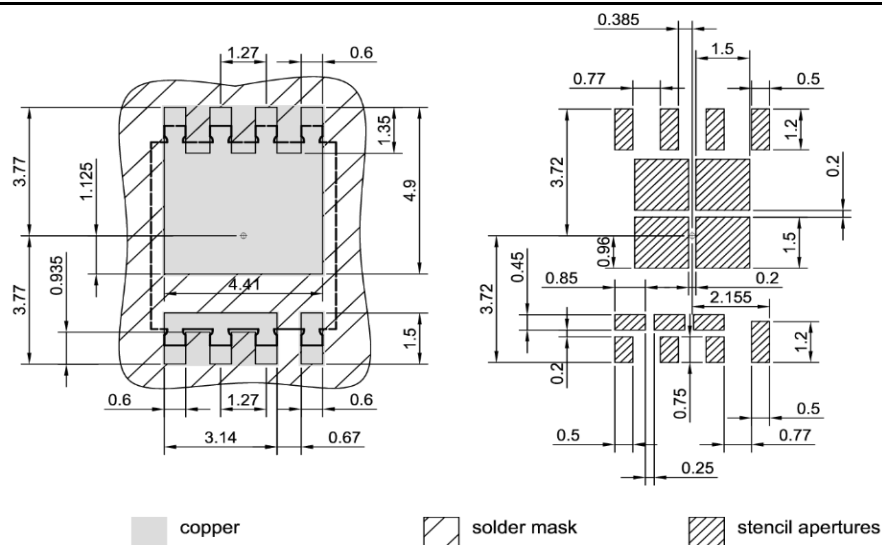


### Package Outline



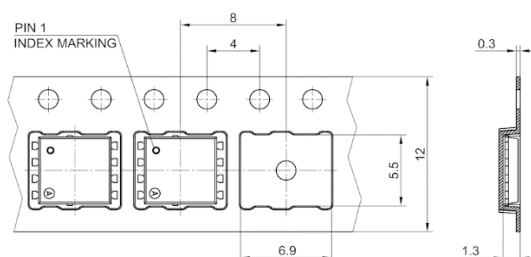
- 1) EXCLUDE MOLD FLASH
  - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
  - 3) LEAD LENGTH UP TO ANTI FLASH LINE
  - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM  
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

### Footprint



All dimensions are in units mm

### Packaging



ALL DIMENSIONS ARE IN UNITS MM  
THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

**Revision History**

Revision	Date	Changes
Revision 1.0	04.02.2022	Final Data Sheet

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**Edition 2022-01-11**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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