Automotive MOSFET

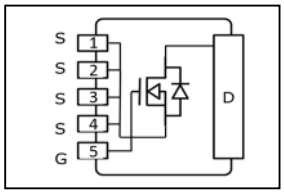
OptiMOS™ 5 Power-Transistor

RoHS Infineon Automotive Quality AEC Qualified

PG-HSOF-5-2

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel – Enhancement mode – Normal Level
- Extended qualification beyond AEC-Q101
- Enhanced electrical testing
- Robust design
- MSL3 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested



Potential applications

General automotive applications.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q101.

Product Summary

V_{DS}	40	V
$R_{DS(on),max}$	1.4	mΩ
I_D (chip limited)	120	A

Type	Package	Marking
IAUA120N04S5N014	PG-HSOF-5-2	5N04N014

Table of Contents

Maximum ratings

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C = 25 °C, V_{GS} = 10 V[1]	120	A
		T_C = 100 °C, V_{GS} = 10 V[2]	120	
Pulsed drain current[2]	$I_{D,pulse}$	T_C = 25 °C	480	
Avalanche energy, single pulse[2]	E_{AS}	I_D = 60 A	190	mJ
Avalanche current, single pulse	I_{AS}	–	120	A
Gate source voltage	V_{GS}	–	±20	V
Power dissipation	P_{tot}	T_C = 25 °C	136	W
Operating and storage temperature	T_j, T_{stg}	–	-55 ... +175	°C

Thermal characteristics[2)]

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	–	–	–	1.10	K/W
Thermal resistance, junction - ambient	R_{thJA}	6 cm² cooling area[3)]	–	–	60	

Electrical characteristics

at Tj=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	40	–	–	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 60 µA	2.2	2.8	3.4	
Zero gate voltage drain current	I_{DSS}	V_{DS} = 40 V, V_{GS} = 0 V, T_j = 25 °C	–	–	1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_j = 125 °C[2)]	–	–	100	
Gate-source leakage current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS} = 7 V, I_D = 60 A	–	1.50	1.60	mΩ
		V_{GS} = 10 V, I_D = 60 A	–	1.20	1.40	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	–	3630	4828	pF
Output capacitance	C_{oss}		–	990	1317	
Reverse transfer capacitance	C_{rss}		–	46	69	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 20 V, V_{GS} = 10 V, I_D = 120 A, R_G = 3.5 Ω	–	7	–	ns
Rise time	t_r		–	4	–	
Turn-off delay time	$t_{d(off)}$		–	14	–	
Fall time	t_f		–	7	–	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD} = 32 V, I_D = 120 A, V_{GS} = 0 to 10 V	–	16	21	nC
Gate to drain charge	Q_{gd}		–	13	20	
Gate charge total	Q_g		–	62	82	
Gate plateau voltage	$V_{plateau}$		–	4.6	–	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C = 25 °C	–	–	120	A
Diode pulse current[2]	$I_{S,pulse}$		–	–	480	
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 60 A, T_j = 25 °C	–	0.8	1.1	V
Reverse recovery time[2]	t_{rr}	V_R = 20 V, I_F = 50 A, di_F/dt = 100 A/µs	–	45	–	ns
Reverse recovery charge[2]	Q_{rr}		–	41	–	nC

[1] Current is limited by package; with a Rthjc = 1.1 K/W the chip is able to carry 230 A at 25°C.

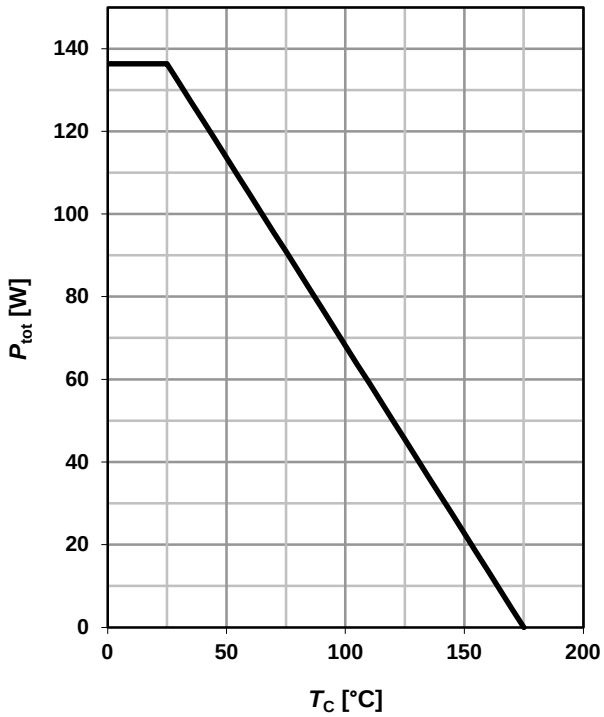
[2] The parameter is not subject to production test- verified by design/characterization.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Electrical characteristics diagrams

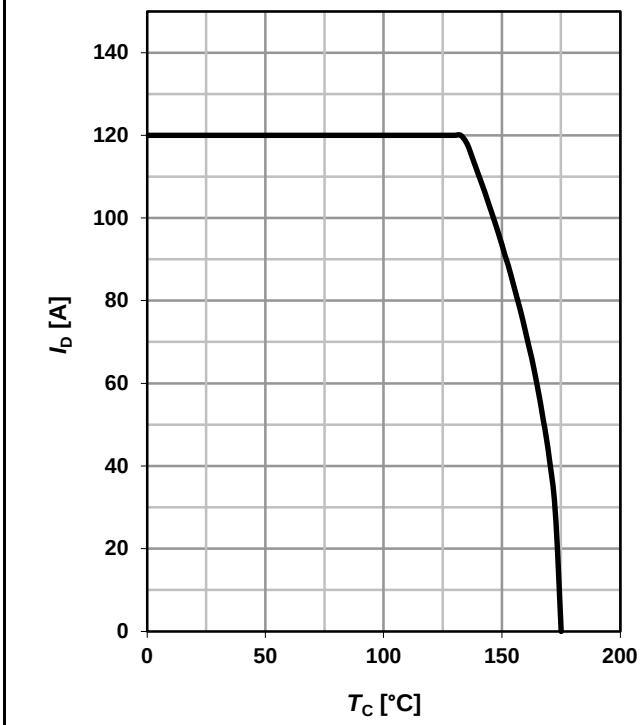
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 10$ V



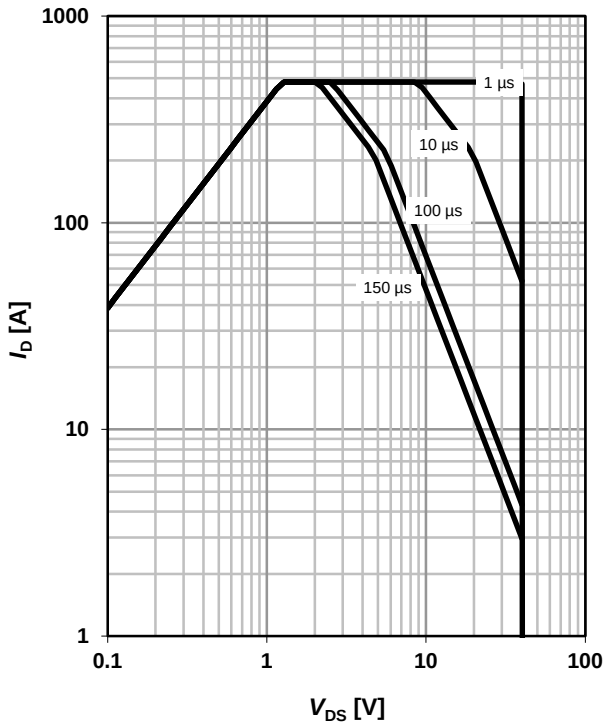
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 10$ V



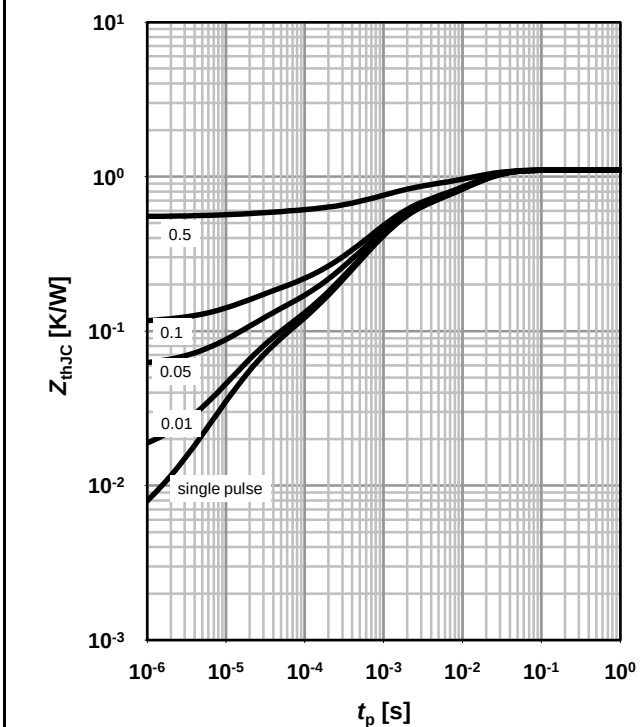
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$; parameter: t_p



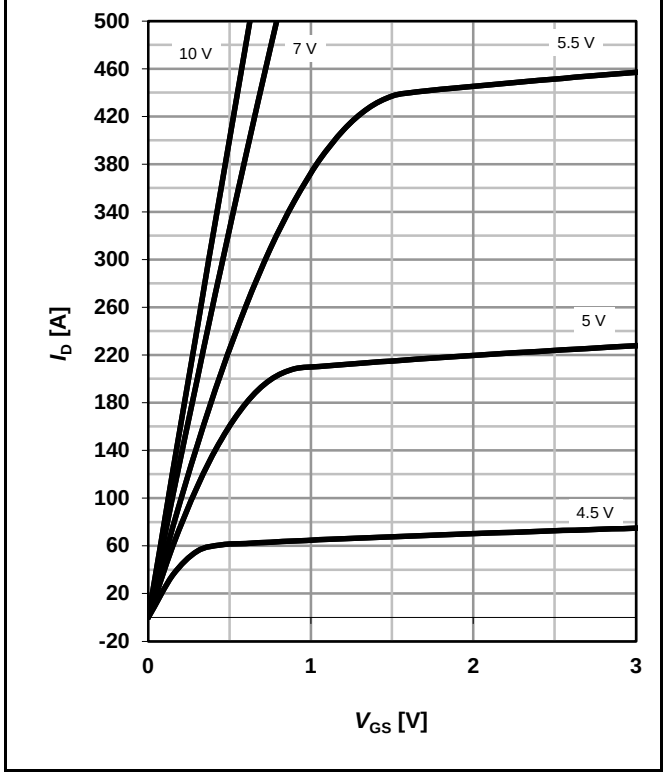
4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$; parameter: $D=t_p/T$



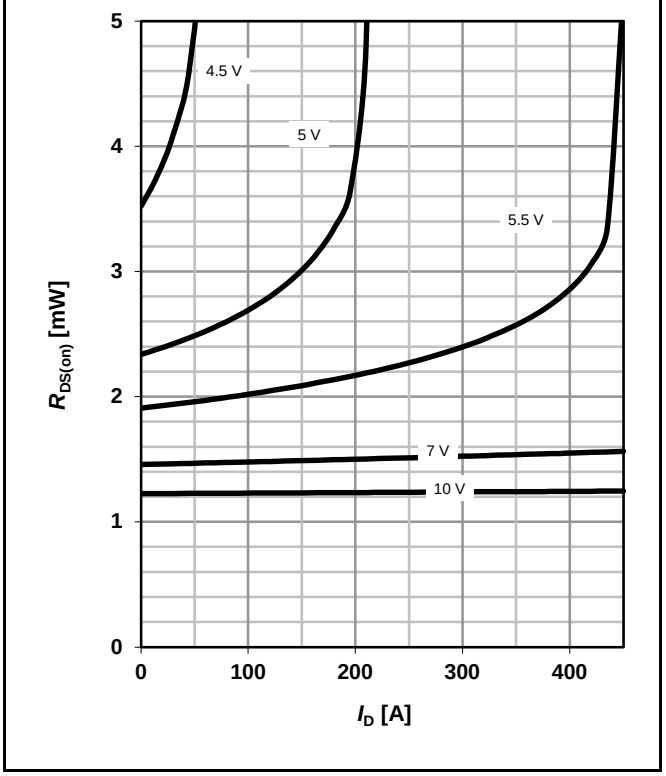
5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C; parameter: V_{GS}



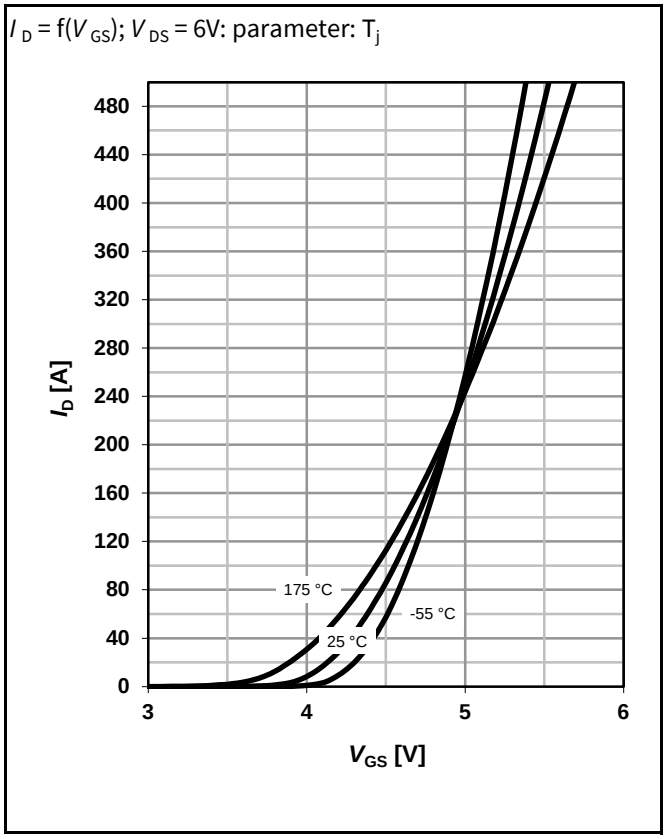
6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C; parameter: V_{GS}



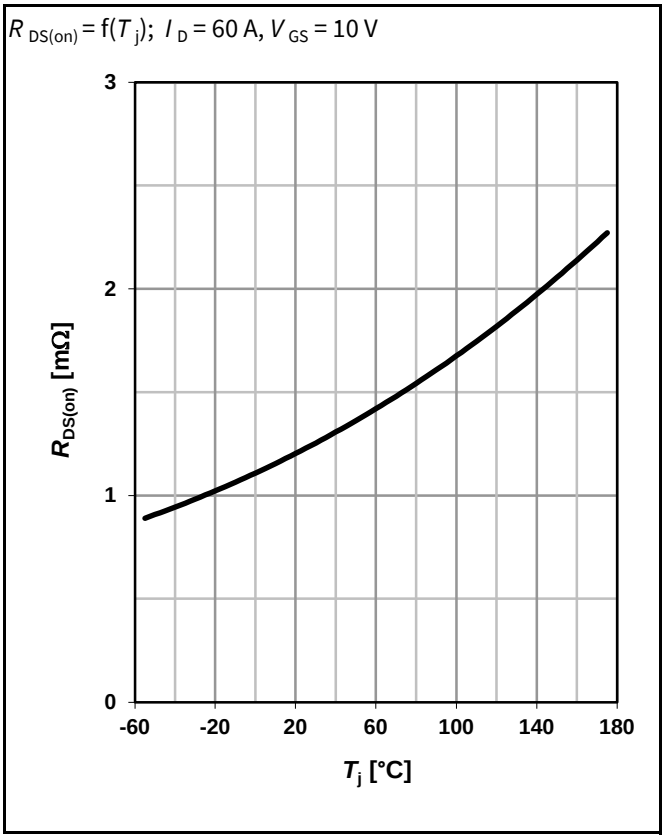
7 Typ. transfer characteristics

$I_D = f(V_{GS})$; $V_{DS} = 6$V: parameter: T_j



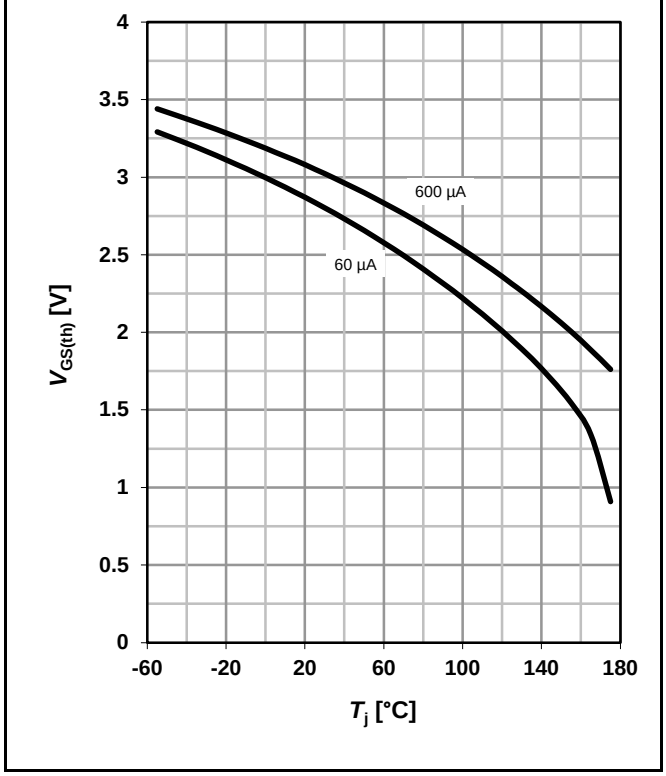
8 Typ. drain-source on-state resistance

$R_{DS(on)} = f(T_j)$; $I_D = 60$ A, $V_{GS} = 10$ V



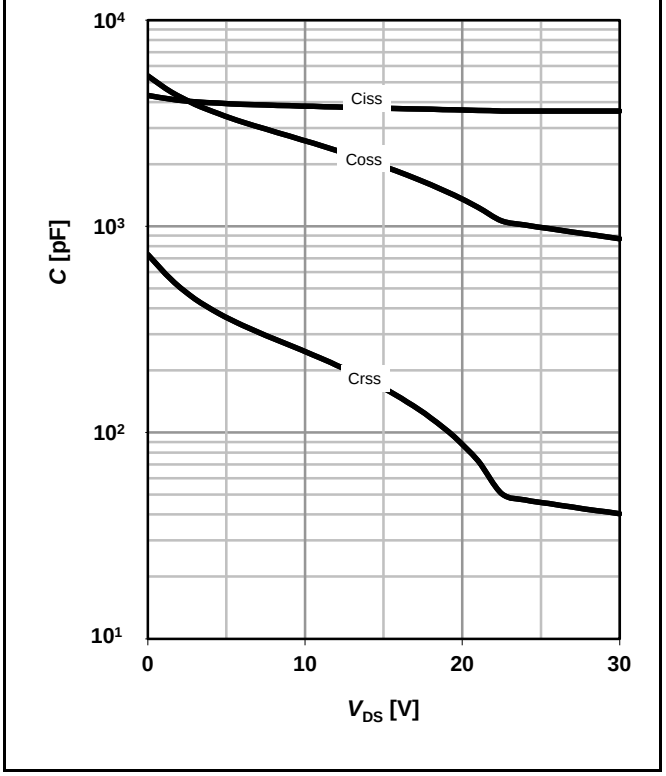
9 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$; parameter: I_D



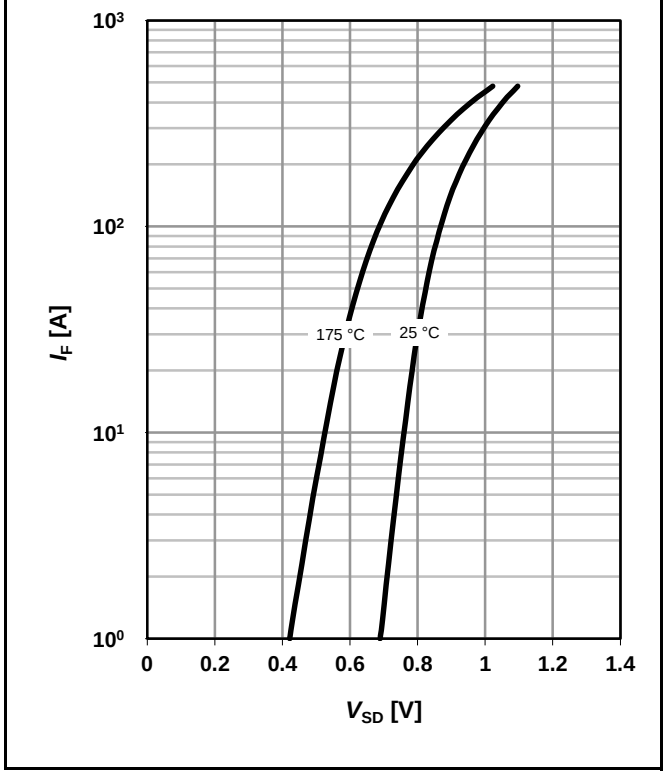
10 Typ. capacitances

$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



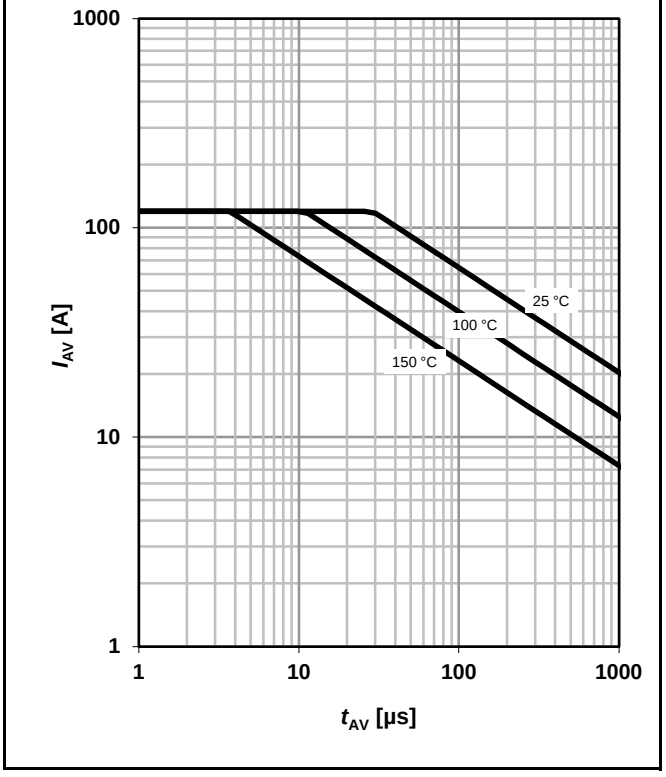
11 Typical forward diode characteristics

$I_F = f(V_{SD})$; parameter: T_j



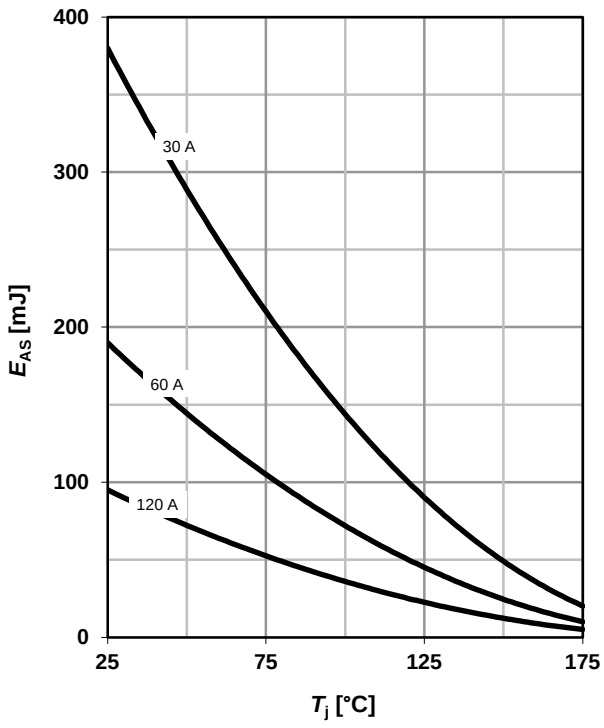
12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$; parameter: $T_{j(start)}$



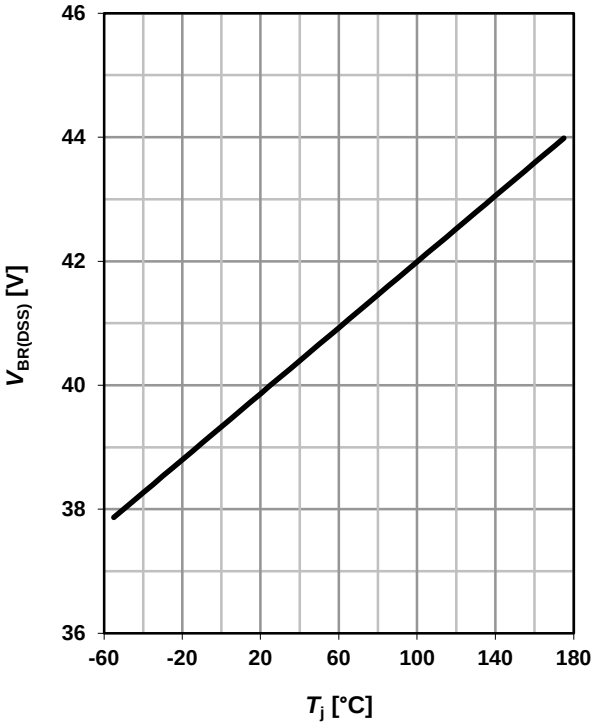
13 Typical avalanche energy

$E_{AS} = f(T_j)$; parameter: ID



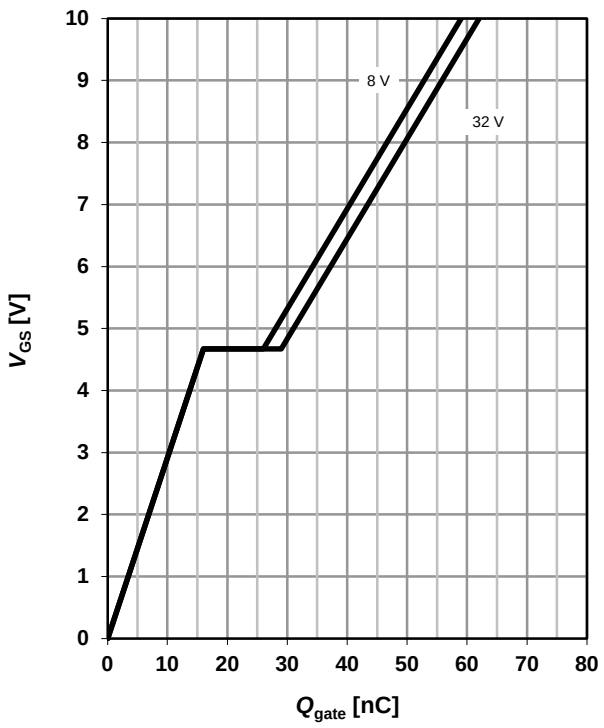
14 Drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j)$; I_{D_typ} = 1 mA

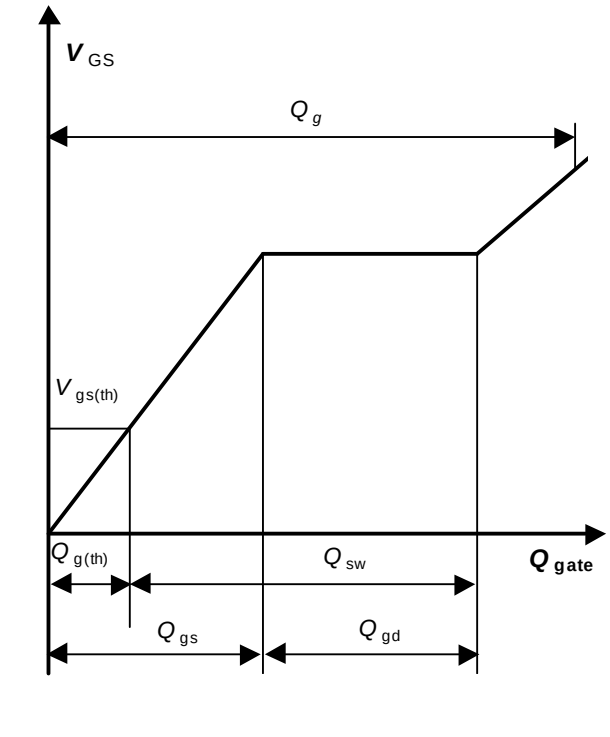


15 Typ. gate charge

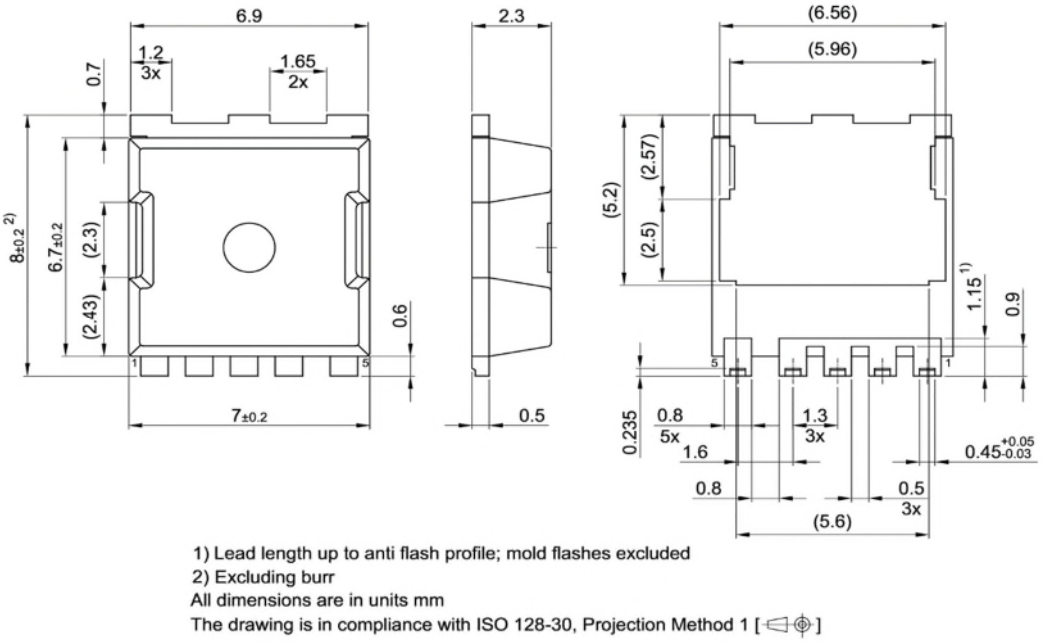
$V_{GS} = f(Q_{gate})$; I_D = 120 A pulsed; parameter: V_{DD}



16 Gate charge waveforms

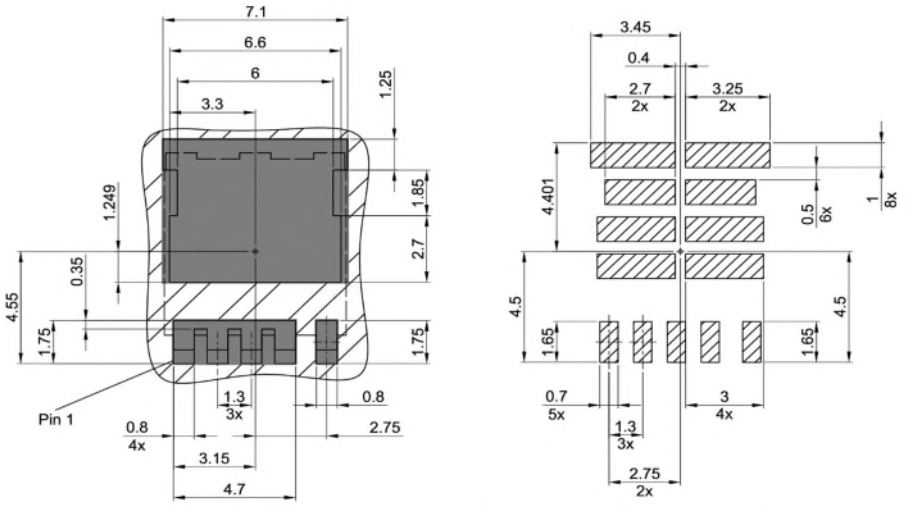


Package Outline



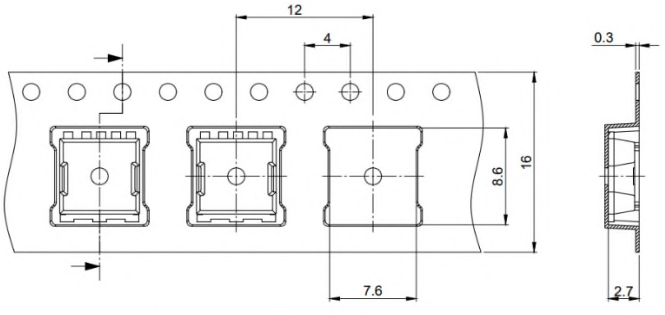
1) Lead length up to anti flash profile; mold flashes excluded
2) Excluding burr
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]

Footprint



All dimensions are in units mm

Packaging



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊲⊕]

Revision History

Revision	Date	Changes
Revision 1.0	11.04.2019	Final Data Sheet
Revision 1.1	24.01.2022	Editorial changes, package drawing added
Revision 1.2	11.09.2023	SOA diagram and I_D condition in figures 8 and 15 updated

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