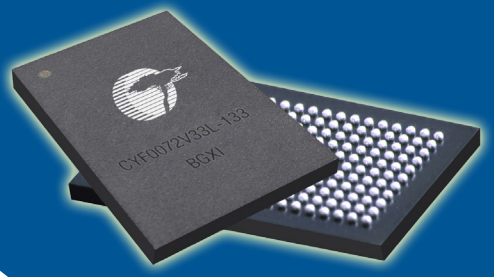
CYPRESS

HIGH-DENSITY FIFO



PRODUCT OVERVIEW

HIGH-DENSITY FIFOS WITH PROGRAMMABLE FEATURES

The Cypress programmable first in first out (FIFO) family offers the industry's highest density programmable FIFO memory device. In addition to densities up to 144 Mb, it has best-in-class speed of 133 MHz in addition to segment-specific, value-added features such as multiqueueing and selectable memory organizations. All of this helps customers design faster and more efficiently making it ideal for a wide range of applications. Based on SRAM technology, high-density (HD) FIFO offers high data reliability and low latency. The easy-to-use bus interface reduces implementation and debugging efforts. It is an off-the-shelf solution that accelerates time-to-market and reduces associated engineering efforts. The device also offers width expansion options.

It suits the video broadcasting, military, medical imaging, and basestation (networking) segments and caters to a host of applications such as:

- Frame buffers for common HD formats (720p, 1080i, 1080p): stores up to four frames of 1080p resolution
- HDTV/SDTV frame synchronization
- Switcher or format converter box
- High-end digital video camera
- High-density buffering in military radars
- Medical imaging
- Basestations - 3G, 4G, and networking

KEY SPECIFICATIONS

DENSITY: 18 Mb, 36 Mb, 72 Mb, 144 Mb

SPEED: 133 MHz

THROUGHPUT: UP TO 4.8 Gbps

BUS WIDTH: USER SELECTABLE x9, x12, x16, x18, x20, x24, x32, x36

CORE VOLTAGE: 1.5 V, 1.8 V

PACKAGE: 209-BALL BGA (14 mm X 22 mm)

INDUSTRIAL TEMPERATURE RANGE: -40 °C TO +85 °C

KEY FEATURES

DIFFERENT DEVICES OFFERED FOR MULTI-QUEUEING

- Single queue (up to 133 MHz)
- Two queues (up to 100 MHz)
- Eight queues (up to 100 MHz)

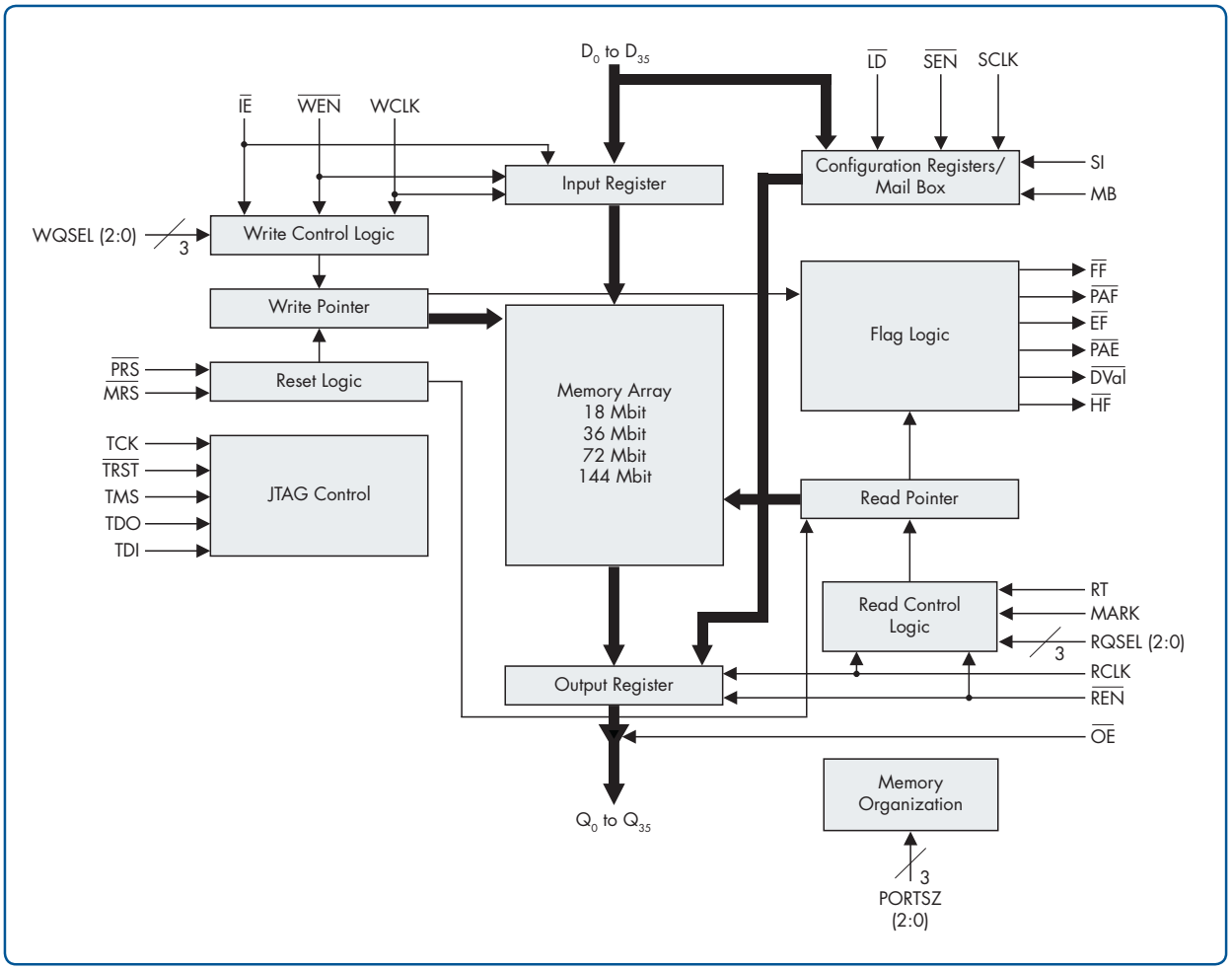
I/O VOLTAGE OPTIONS

- Supports 1.8 V and 3.3 V
- Available in LVCMOS

CYPRESS PERFORM

KEY FEATURES

- Multi-queue feature: Divide the FIFO into queues and switch randomly between queues. Useful for picture in picture and interlacing/ de-interlacing
- Unidirectional operation with independent read/write ports - supports simultaneous read/write operations
- Input and output enable control for write mask and read skip operations
- Mark and retransmit feature resets read pointer to user marked position
- A mail box register to send data from input to output port bypassing the FIFO sequence
- Separate SCLK input for serial programming of the configuration register
- Empty, full, half-full, and programmable almost-empty and almost-full status flags
- Programmable flags can be programmed either through serial or parallel means
- A partial reset to clear data but retain programmable settings
- JTAG port for boundary scan function



HD FIFO Functional Block Diagram

KEY ADVANTAGES

Simplified System Architecture - HD FIFO versus Other Discrete FIFOs

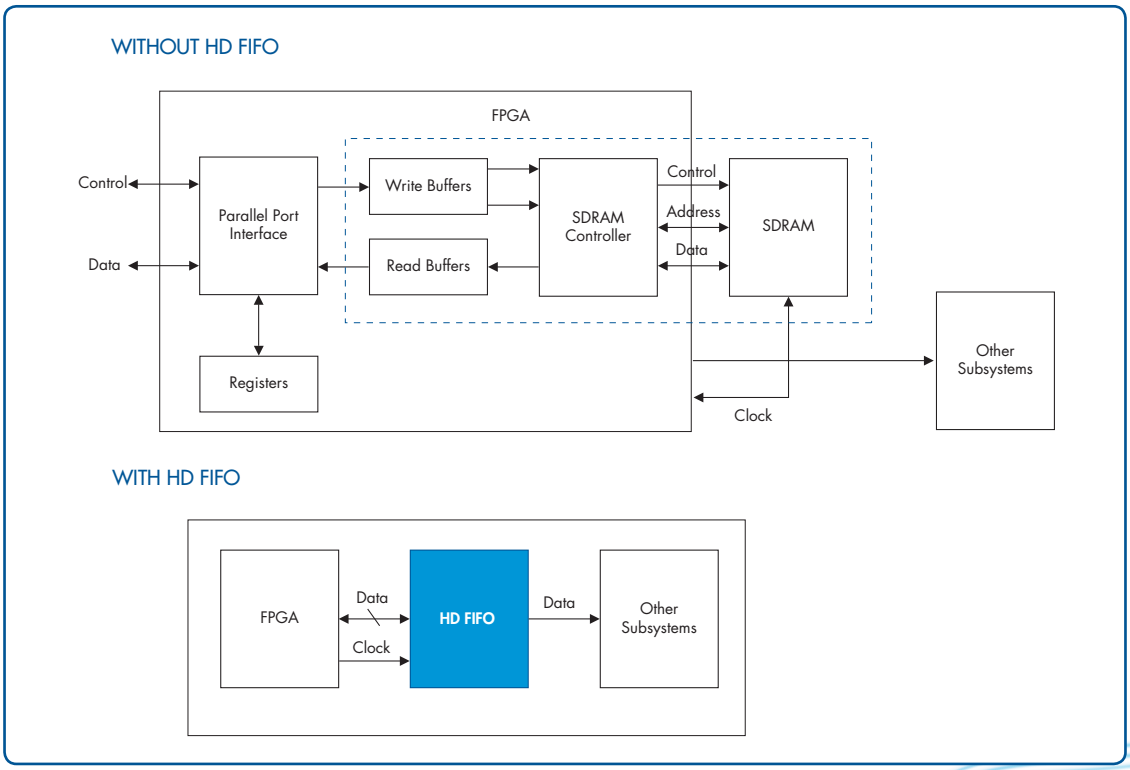
Discrete FIFOs in today's market are constrained by the densities they offer and high costs per megabit. The multi-queueing feature in Cypress's HD FIFO provides a much-needed tool that simplifies the system architecture of high performance imaging, video processing, and networking systems. This allows customers to design solutions quickly and more cost effectively than other discrete solutions.

FPGA/DSP Integrated Memory - HD FIFO and FPGA versus SDRAM and FPGA Solution

Image processing systems require very high amounts of data buffering that is handled by an FPGA. To achieve this high-density memory buffering, FPGAs are often coupled with an external SDRAM. By implementing FIFO controller logic inside the FPGA, the external SDRAM functions like a FIFO. To compensate for the latency of the external DRAM, a small memory buffer is created inside the FPGA. However, this has some drawbacks, which force customers to use higher-range FPGAs:

- Valuable logic resources in the FPGA used, making the design complicated and reducing efficiency
- Valuable FPGA I/Os used as the controller implemented in the FPGA needs to send address signals to the external SDRAM memory
- FPGA's internal memory space required (scratch pad memory), eliminating availability for other purposes
- Increased system complexity reduces performance

With Cypress's programmable HD FIFO, customers can choose to use a lower density FPGA resulting in reduced system costs. The diagram below shows the comparison between two such systems. HD FIFO also enables various combinations of part offerings to meet customer requirements and feature priorities.



Block Diagram Comparing Systems with and without HD FIFO

ORDERING INFORMATION

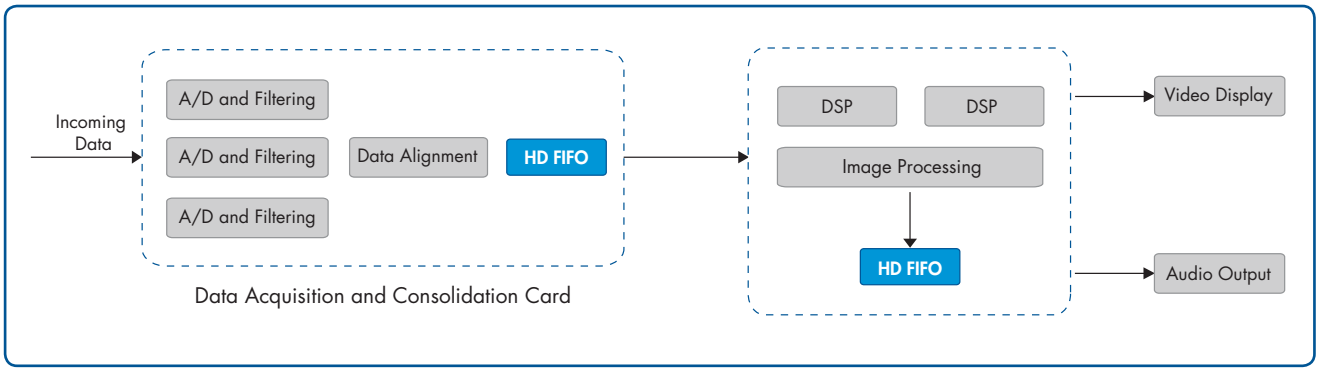
Density (Mb)	Organization	V_{DD} (V)	Temperature (°C)	Frequency (MHz)	Queues	I/O Voltage Standards (V)	Package	Availability
18	User selectable x9, x12, x16, x18, x20, x24, x32, x36	1.5, 1.8	-40 to +85	133	Single, double, 8	1.8, 3.3	209-ball BGA	Production parts available - order now!
36								
72								
144								Engineering samples available in Q1 2014. Production in Q2 2014.

HD FIFO IN AN IMAGING SYSTEM - AN EXAMPLE

The diagram below illustrates the working of an imaging system with HD FIFO. A typical imaging system comprises two sets of cards:

Data Acquisition and Consolidation Cards - Data acquisition cards filter incoming data. A diagnostic imaging system may comprise multiple data acquisition cards. Data consolidation cards buffer and align the acquired data. For CT and PET scanners, detectors rotate around the body and the data is serialized and sent across a slip ring electromechanical subassembly.

Image/Data Processing Cards - These cards perform heavy duty filtering and the most algorithm-intensive image reconstruction.



Example Application Bock Diagram with the Cards

GET STARTED NOW

For more information on HD FIFOs, visit www.cypress.com/go/HDFIFO or contact spcm_mktg@cypress.com.

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