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AN220270

Hardware Design Guide for the Traveo II Family

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Associated Part Family: CYT2B, CYT4B, CYT3D, CYT4D Series

Related Application Notes: Click here

This application note describes how to set up a hardware environment for Traveo™ II MCU family.

Contents

1 Introduction

This document describes how to set up a hardware environment for the Cypress Traveo II MCU family.

Design restrictions and recommendations regarding signal wiring and the electrical power system of the MCU are considered. For more details on the device features and its relevant settings, see the Traveo II Architecture Technical Reference Manual (TRM) and the dedicated device datasheet.

This application note answers most of frequent questions. It is not intended to replace the designer's responsibility.

2 Package Selection

First, decide the package you want to use for your design. Several considerations drive this decision, including number of I/O pins required, PCB and product size, PCB design rules, and thermal and mechanical stresses.

The Cypress device families have a very large selection of devices to help match your exact needs in any situation with an efficient and cost-effective solution. Packaging solutions range from the ultra-small Wafer Scale Packages to high pin count Ball Grid Array packages. Easier to layout on lower layer counts and lower cost PCBs are the Leaded Quad Flat Pack (LQFP). LQFP packaging options range from 48-pin devices to 176-pin devices for example.

Following are some package selection criteria:

LQFP

- Easier to route signals due to large pitch and the open area below the part
- Less mechanical rigidity for more protection against vibration and mechanical stress
- Disadvantages include larger package and lower thermal conduction (θ_{JA})

BGA and PBGA

- Small-scale packages offering high pin counts in larger lead pitches, which significantly reduce the manufacturing complexities for high I/O devices. BGA packages are used in applications requiring:
  - Faster circuitry speed because the terminations are much shorter and therefore less inductive and resistive.
  - Better heat dissipation.
- Conventional surface mount technology (SMT) production technologies such as stencil printing and component mounting can be used.
- Robust reflow processing, due to higher pitch (1.27 mm, 0.050", typical), better lead rigidity, and self-alignment characteristics. Self-alignment during reflow is very beneficial and opens the process window considerably.
- Disadvantage: X-ray is needed for solder joint inspection.

3 Power Supply

3.1 Power Domains

The MCU power system is based on separate analog and digital supplies as listed in Table 1.

Table 2 describes the functionality of each power supply pin.

Table 1. Power Domains

Power Domain	Associated Pins	
	CYT2B/4B Series	CYT4D Series
Analog	VDDA, VSSA	VDDA_ADC, VSSA_ADC, VDDA_DAC, VSSA_DAC, VDDPLL_FPD, VDDHA_FPD, VDDA_FPD, VSSA_FPD, VDDA_MIPI, VSSA_MIPI
Digital	VCCD, VSS	VCCD, VSSD
I/O	VDDIO, VSSIO	VDDIO_GPIO, VDDIO_SMC, VDDIO_HSIO, VDDIO_SMIF, VDDIO_SMIF_HV
Shared digital and I/O	VDDD	VDDD

Table 2. Power Supply Pin Description

Pin Name	Function	Nominal Power Domain Voltage Range
VDDD/VSSD	Shared power supply pins for internal voltage regulator, internal logic, I/O domain with GPIO_STD cells and debug IF.	3.3 V – 5.0 V
VSSD_1	Only BGA package: Silent ground connection	-
VDDIO_1/VSSIO_1	Power pins for I/O domain with GPIO_STD I/O cells grid.	3.3 V – 5.0 V
VDDIO_2/VSSIO_2	I/O power pins for GPIO_STD I/O cells.	3.3 V – 5.0 V
VDDIO_3/VSSIO_3	I/O power pins for HSIO_STD I/O cells for memory interfaces, but also slow signal shared on that domain. **Note**: Only BGA packages	3.3 V
VDDIO_4/VSSIO_4	I/O power pins for HSIO_STD I/O cells for Gigabit Ethernet shared with slow signals. **Note**: Only BGA packages	3.3 V
VDDA/VSSA	Power supply pin pair for analog part of the MCU.	Same as VDDIO_2, VDDD, or both depending on the deployed analog pins belonging to the domain.
VREFH/VREFL	Reference voltage pins for the AD-converter.	Same as VDDA

Pin Name	Function	Nominal Power Domain Voltage Range
VCCD	Internal core supply case: Dedicated power supply pin to internal voltage regulator output, to buffer the core voltage with an external smoothing capacitor. External core supply case: Depending on the device and the power dissipation of an application these pins are deployed for connecting external voltage source to the core supply. General: If a device package has several VCCD pins, then all VCCD pins must be shorted with each other. Therefore, the connections must have low impedance. For a BGA design, a common power island for VCCD is recommended to keep the EMI reduced.	1.1 V
VDDIO_GPIO	Power supply pin for GPIO	3.3 V – 5.0 V
VDDIO_SMC	Power supply pin for Stepper Motor Control I/O	3.3 V – 5.0 V
VDDIO_HSIO	Power supply pin for High-Speed I/O	3.3 V
VDDIO_SMIF	Power supply pin for HSIO_ENH IO 1.8V Serial Memory Interface	1.8 V
VDDIO_SMIF_HV	Power supply pin for HSIO_STD IO 3.3V Serial Memory Interface	3.3 V
VDDPLL_FPD	Power supply pin for FPD-Link PLL	1.1 V
VDDHA_FPD	Power supply pin for FPD-Link line drivers	3.3 V
VDDA_FPD / VSSA_FPD	Power supply pin pair for FPD-Link core	1.1 V
VDDA_MIPI / VSSA_MIPI	Power supply pin pair for D-PHY	1.1 V
VDDA_ADC / VSSA_ADC	Power supply pin pair for analog part of the MCU	3.3 V – 5.0 V
VDDA_DAC / VSSA_DAC	Power supply pin pair for Audio digital-analog convertor	3.3 V

To define a single supply rail, all power supplies should be connected to voltages between 3.3 V and 5.0 V. If you need to apply different power supply voltages, such as 5 V to the analog system (i.e., $V_{DDA} = V_{REFH}$) and 3.3 V to V_{DDIO} of the MCU port pins, see the operating conditions in the datasheet of the dedicated device. Table 1 lists the available power domains on the MCU.

Devices designed for applications with higher power dissipation require an external core supply source, which is controlled by dedicated MCU pins.

3.2 Analog Digital Converter Supply Pins

To avoid additional leakage current, connect the analog converter supply pins (VDDA, VSSA, VREFH, and optionally VREFL), even if the ADC is not used.

3.3 Power Supply Variants

Although separate power supplies are provided in the MCU, dependencies between each other must be considered. The power domains are independent of each other.

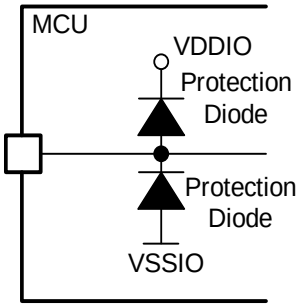
ADC

The enabled analog inputs belong to dedicated I/O domains, which means that the applied voltage level of an analog sensor is limited to the I/O domain supply level and the protection diode structure. That means, the analog supplies and the I/O domains of the selected analog inputs must have the same voltage supply level.

Debug Connection

You must select a power supply, on which both the debug HW tool and the MCU can communicate with each other. For more information on the HW connection, see Debug Interface.

Figure 1. Protection Diode Structure for All I/O Pins



3.4 Power ON/Power OFF Sequence of Power Supply Domains

Different voltage levels can be supplied to the power rails of the MCU. Therefore, power ON/OFF sequence is not required for power supplies of many devices. When there is no supply voltage at V_{DDD}, but the analog supply V_{DDA} is powered, a leakage current inside the MCU can occur. However, no port output will be driven. If a device needs a power sequence, see the device datasheet.

General

- Disable monitoring features (for example, LVD, BOD, internal supply monitoring via ADC) before disabling related power domains. Otherwise, an unintended reset or fault might occur.
- Disable or tie to low output pins before disabling the power domains
- Disable input buffers before disabling the power domains
- Power sequencing requirements and power domain dependencies can differ between power modes. So, when domains need to be switched OFF to reduce the leakage current in power save modes, carefully consider the transition phase for entering and leaving the modes.
- ECU peripherals must be in proper states during the power mode transitions.

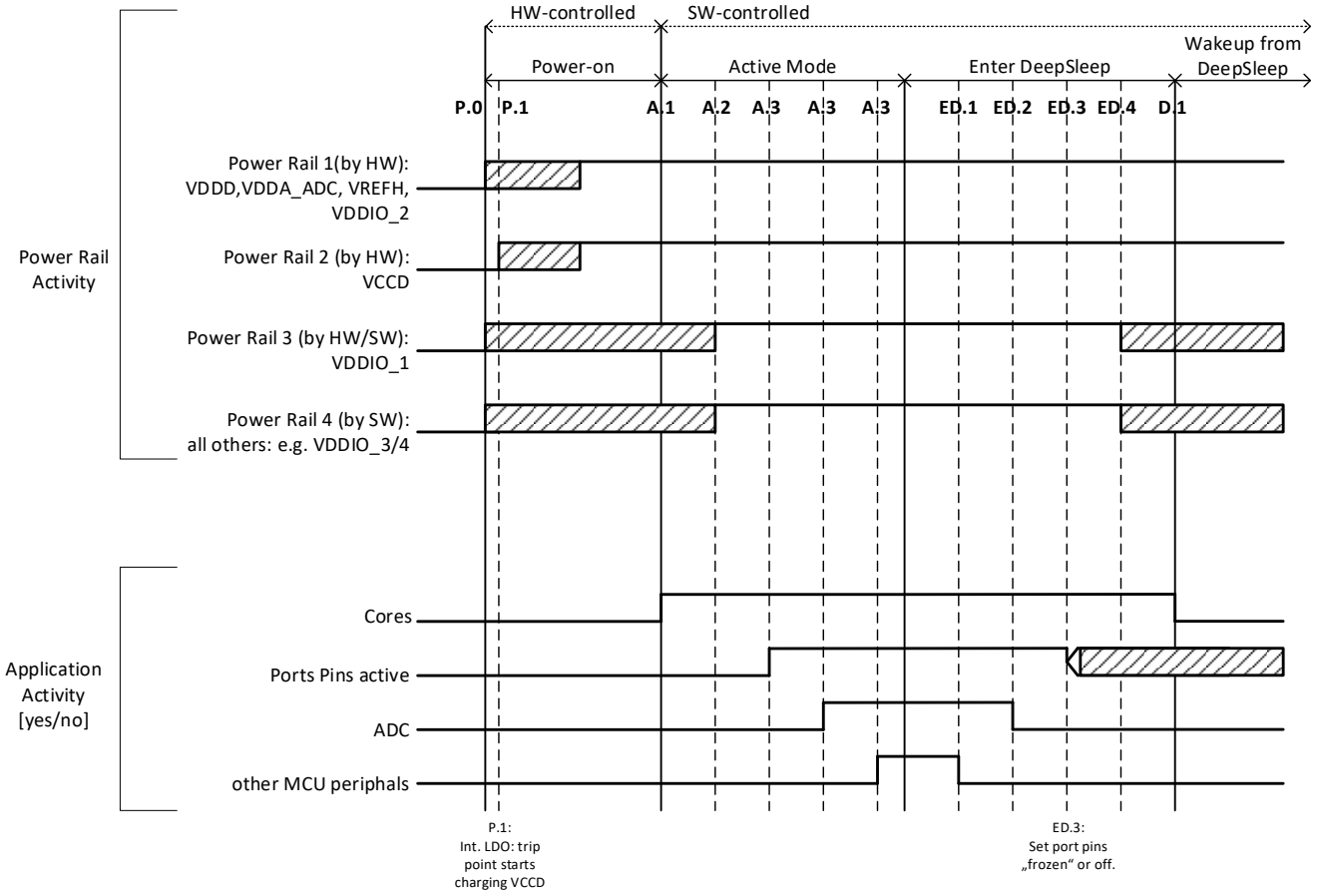
External core supply

- Devices running with external core supply have the same power ON/OFF sequence, because the MCU is starting in the internal supply mode and the external core supply must be enabled by the application. In power off transition, the external core supply is disabled by the MCU.

ADC

- In Active mode, leakage current occurs only when $V_{CCD} > V_{DDA\_ADC}$.
- Many I/O domains with shared analog/digital inputs can be ramped up after VDDA_ADC, as long as the ADC does not start the sampling operation of these domains.
- When the I/O domain is deployed only for digital signaling, many I/O domains can also have voltage operation range different from that of the ADC. See Clamping Structure of I/O Pins with Shared Analog Function.
- Do not address analog multiplexing bus (AMUXBUS) to unpowered domains.

Figure 2. Power Sequencing Example on CYT4B Series



Note:
VDDA_ADC: Leakage, when VCCD > VDDA_ADC in Active mode
ED.3: When I/O Domain Is OFF in Power Save Mode, then I/O Pins must be set to OFF state.
: Power Rail flexibility in sequencing according to power domain requirements

3.5 Power Supply Circuit

To meet EMC requirements for the target board, a noise efficient supply buffering concept is needed. Therefore, the supply should be filtered. To have a minimum noise on the analog supply, it is recommended to use a separate analog and digital power supply.

Power supply concept proposal for different devices are discussed in Appendix A Power Supply Concept.

3.6 External Core Supply Control

The power supply concept description is not part of this documentation. See the application note corresponding to your device in Related Documents.

3.7 Unused Power Domains

Unused power domain is usually considered as a permanent OFF state related to power domain in the full application lifecycle. However, a temporary state of unused domain is also possible, when some not-always-on power domains stay on in power save modes. For details on how to handle the I/O port pins of dedicated domain, see Port Input/Unused Pins.

In general, the following are the main classes of unused domain:

- Permanent unused domain: Not required in application
- Temporary unused domain: Disabled in power save mode

For details on different devices, see Unused Power Domain Handling.

Note: If you do not find information on unused power domains in the device datasheet, contact the technical support.

4 Clock Sources

The MCU provides several clock sources depending on the system requirements. Table 3 lists the available clock sources for the MCU system and shows how the clock sources are connected to the MCU internal clock system.

Table 3. Clock Sources

Clock Source	Oscillator	Int/ Ext	Port Pin Name (ext. only)	Frequency	Trimmable	Use Case
Internal Main Oscillator (IMO)	Yes	Int	-	8 MHz	Yes	LIN
Internal Low-Speed Oscillator (ILO)	Yes	Int		32 kHz	Yes	
External Crystal Oscillator (ECO)	Yes	Ext	ECO_IN ECO_OUT	~4 MHz to 33.33 MHz	Yes	CAN communication
Watch Crystal (WCO)	Yes	Ext	WCO_IN WCO_OUT	32.768 kHz	No	Watch
Low Power External Crystal Oscillator (LPECO) [1]	Yes	Ext	LPECO_IN LPECO_OUT	~4 MHz to 8 MHz	No	Watch
EXT_CLK pin[2]	No	Ext	Optional on several pins	Note[3]	-	Test
Reference clock for Ethernet PHY and MAC	Yes	Ext	ETHn_REF_CLK	50 MHz	-	Ethernet: RMII
				125 MHz	-	Ethernet: GMII, RGMII

5 Reset Circuit

To make sure that a MCU operates within the specifications, an external reset signal via the reset input pin (XRES pin) or an internal reset signal can be generated. The implementation of the internal reset circuits has several advantages over the hardware design:

- Reduced bill of material (BOM) cost as the external monitoring ICs are removed
- Detection of MCU internal out-of-range operations, which cannot be monitored externally (for example, MCU internal voltage drops)

Note that external monitoring or resetting ICs might still be needed based on the application requirements.

5.1 Reset Pin (XRES)

A switch connects the reset input pin to VSSIO (Ground). An internal pull-up resistor and an internal noise filter of minimum 100 ns are available, to reduce the BOM cost. If an external capacitor is applied for additional filtering, then

[1] LPECO is available only for CYT4D series.

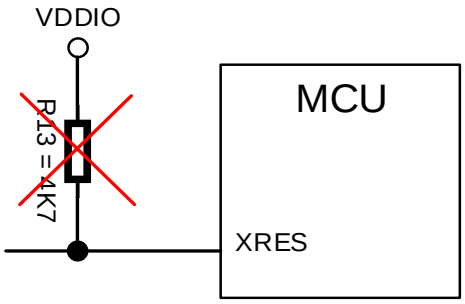
[2] This port pin is bi-directional and can be used as an external clock source for the device and as a clock observation for internal clock signals.

[3] See External Clock Input Specifications in the device datasheet.

make sure that the EMC requirements are fulfilled. Otherwise, the ESD test pulses might destroy the ESD protection structure inside the MCU.

For details on the reset pin, see the datasheet.

Figure 3. External Reset Input (XRES)



5.2 Power Supply Monitoring

To make sure that the MCU is not running out of the operating conditions, a broad range of power monitor circuits is provided by the MCU. See the device Architecture TRM and datasheet for more details.

Power-on Reset (POR)

Power-on reset (POR) circuits provide a reset pulse during the initial power ramp. Here, only the V_{DDD} power supply rail is observed.

Brown-out Detection (BOD)

The brown-out Detection (BOD) circuit protects the operating or retaining logic from possibly unsafe supply conditions by applying reset to the device. BOD circuits for the power supply rails VDDD, VDDA, and VCCD are provided. A reset is generated when one of the monitored operating ranges is undercut. This circuit is required to detect a sneaking voltage drop of the battery power supply.

Low-voltage Detection (LVD) and High-voltage Detection (HVD)

Before the BOD level threshold generates a reset, you might be warned by the configurable circuit for low-voltage detection (LVD) and high-voltage detection (HVD) use case. You can configure the trip point (detection level), which creates an interrupt for possible safety measures. This circuit can oversee faster transitions.

Over-voltage Detection (OVD)

Over-voltage detection (OVD) circuit applies a device reset when V_{CCD}, V_{DDD}, or V_{DDA} supply goes above the maximum allowed voltage. This concept is a reverse of BOD circuit.

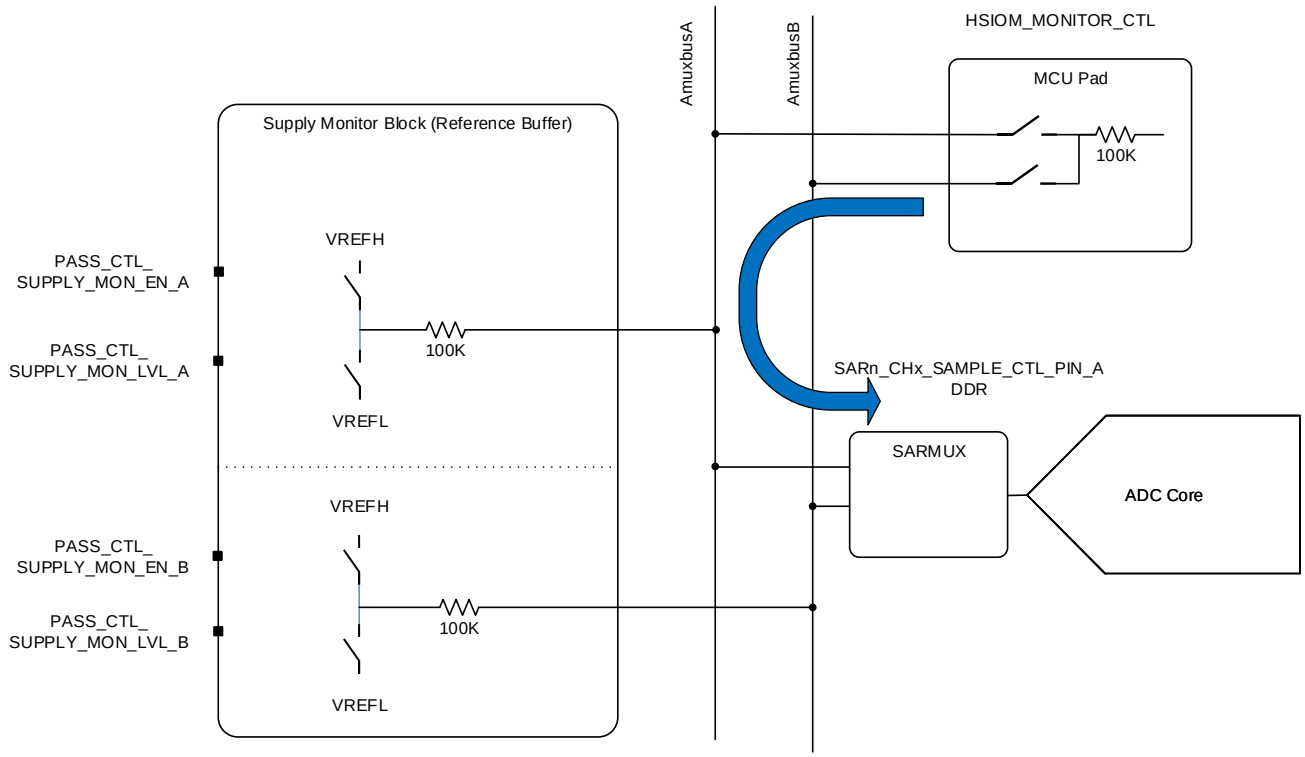
Over-current Detection (OCD)

The over-current detection circuit monitors the current of the power supply rail V_{CCD} and detects whether the load current of a regulator is higher than expected. If the current is over the regulator limit, the OCD circuit generates a reset to protect the device.

Power Domain Voltage Monitoring by the ADC

The ADC provides the opportunity to monitor several power supply and ground pads. Instead of a reset, an interrupt is solely generated by the corresponding ADC unit. To keep the CPU load low, the range detection feature can be enabled to generate only an interrupt when a critical range is entered. The pads can be selected by a complex multiplexer structure as shown in Figure 4. For more details on this feature, see chapters *Analog Subsystem* > *SAR ADC* > *Reference Buffer* and *Resources Subsystem (SRSS)* > *Voltage Monitoring* > *Voltage Monitoring by ADC* in the Architecture TRM.

Figure 4. Block Diagram of Voltage Monitoring by ADC



5.3 Watchdog Reset

An internal watchdog timer (WDT) within the MCU supports a wide range of capabilities. This WDT circuit can also run in the Hibernate power mode (see Device Power Modes in the Architecture TRM).

6 Ports and Non-Power Pins

6.1 Port Input/Unused Pins

6.1.1 General Consideration

This section explains the different methods to handle unused pins and the advantages and disadvantages with respect to the MCU operation. In general, the risk of unused pins is floating inputs and a latch-up effect within the pin structure.

Open Pin Connection

During and after POR, by default, the I/O pins are in a high-impedance (high-Z) analog state with disabled input buffers. The advantage of this method is that the current consumption of the MCU is lower when compared to the use of a terminal resistor; and the BOM cost is reduced. The disadvantage is that during an assembly option, a long signal trace is routed to the pin, and the signal trace can take effect as an antenna and a captured noise can cause a latch-up at the pin.

Direct Connection to GND or Power Supply

The I/O pins should not be connected directly to GND or to power supply as the power supply traces can take effect as an antenna to the pin and the captured noise can cause a latch-up effect.

Internal Pull-up/Down Resistor as Termination

When there is a risk of a latch-up effect at an unused pin due to the board design (long traces of optional features), terminate the input pin using internal pull-up or pull-down resistance.

The advantage is low current consumption and BOM cost reduction in place to external termination resistors. Disadvantage is that you must configure the port pin state after the reset. Therefore, during reset caused by any

disturbance (supply, clock issues, and so on), the internal termination is not available anymore and the system is again vulnerable against a latch-up effect. You can choose this method, if there are unused pins without long trace. In general, it must be considered that the pin state (enabled pull-up or pull-down resistor) must be unchanged when a Low Power mode is entered. The reason is that for an external resistor the internal termination must be available all the time.

External Pull Up/Down Resistor as Termination

An external termination resistor can be placed next to the unused I/O pin instead of using the internal ones. In case of an open signal line routed to the pin, any injected noise can be safely terminated even during the device reset. A resistor value between 2.2 kΩ and 10 kΩ can be used. But you should not connect several unused pins to one common termination resistor, because if unused I/O pins unintentionally drive different output levels against each other, the I/O pins might be permanently damaged.

6.1.2 Dedicated Port Pins

For dedicated MCU peripherals the unused I/O handling is explicitly considered. In most of these cases, the entire MCU peripheral including the power domain pins must be considered to avoid the risk of latch-up (LU). For more details on power domain pins, see Unused Power Domains.

Table 4. Handling of unused dedicated I/O Pins

MCU Peripheral	Power Domain	I/O Pin	I/O Function [IN/OUT]	Pin Handling (Connect to …)
MIPI	VDDA_MIPI	MIPI_DPx x: 0/1/2/3	IN	Open Pin Connection
	VDDA_MIPI	MIPI_DNx x: 0/1/2/3	IN	Open Pin Connection
	VDDA_MIPI	REXT	IN	Open Pin Connection (ext 15 kΩ removed)
FPD	VDDA_FPD	FPD_TxP x: A/B/C/D	OUT	Open Pin Connection
	VDDA_FPD	FPD_TxN x: A/B/C/D	OUT	Open Pin Connection
Audio DAC	VDDA_DAC	C_L, C_R	IN	GND (when Mono sound: Open Pin Connection of unused part)
		DAC_L, DAC_R	OUT	

6.2 Pins in Lower Power Mode

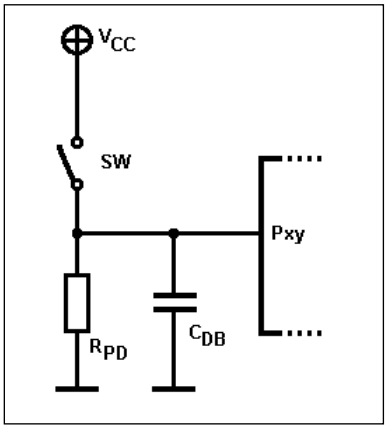
To achieve the lowest possible quiescent current in a low power mode, the current consumption of I/O pins must be considered. Depending on the low power mode, the configuration state and the last output state are frozen. In case of input pins, it is forbidden to have floating input levels, because the quiescent current of the MCU increases dramatically. When an input pin is used as a wake-up pin, do not change the configuration under the assumption that the pin has an internal or external pull-up or pull-down resistor for termination. When an input pin is not required in a low power mode, then it can be configured to high-z input with disabled input buffer. For details on different low power modes, see the architecture TRM and the corresponding application note listed in Related Documents.

6.3 Latch-up Consideration (Switch)

Pressed switches usually cause a bouncing signal. This can damage the MCU port pin. As a countermeasure debounce capacitors are deployed. Exercise caution with external switches to V_{CC} or ground together with debounce capacitors connected to port pins.

A usual configuration is shown in Figure 5.

Figure 5. Principle Switch Circuit

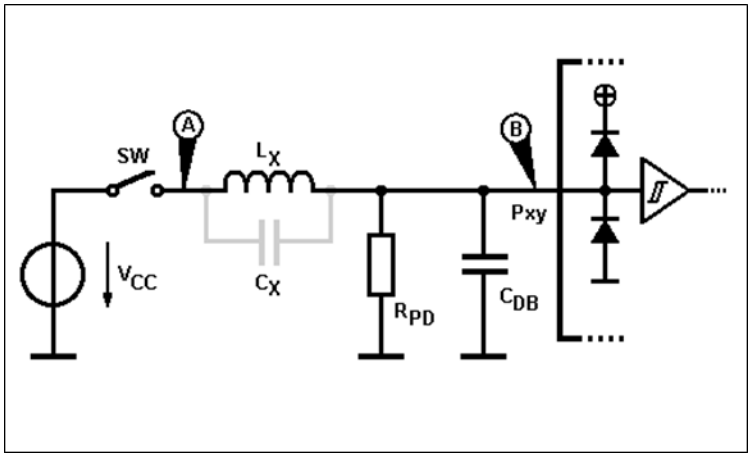


R_{PD} is a pull-down resistor and C_{DB} a debounce capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. When the switch is closed, the input changes to “1”.

From the physical aspect, it needs to be considered that the switch is often placed at a distance from the MCU by cable, wire, or circuit path. The longer the circuit path is, the higher will be its inductivity LX (and capacity CX).

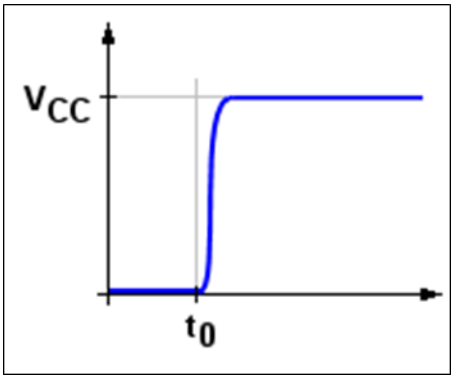
An equivalent circuit diagram is shown in Figure 6.

Figure 6. Equivalent Circuit of the Principle Switch Circuit



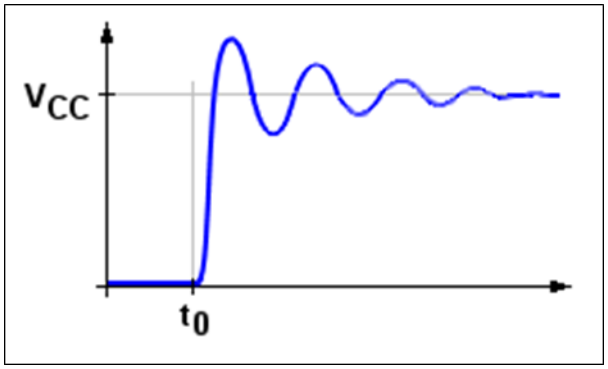
By closing the switch SW at time t_0, as shown in Figure 7 the voltage can be measured at point (A).

Figure 7. Signal Rise after Closing the Switch at Point (A).



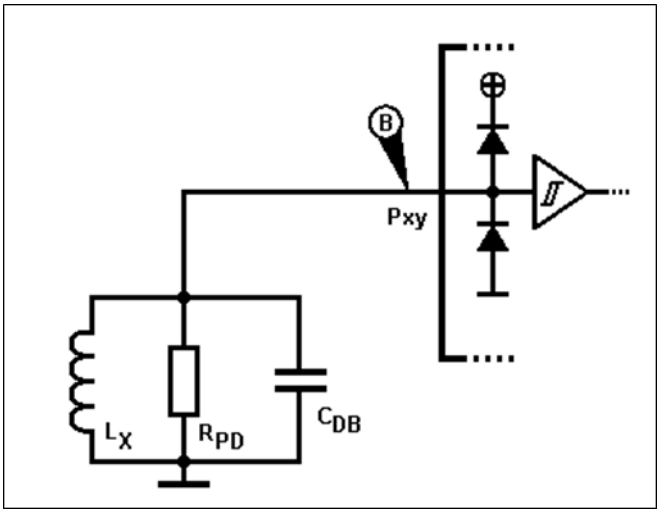
But, at the port pin Pxy on point (B), as shown Figure 8, voltage can be measured.

Figure 8. Signal Rise after Closing the Switch at Point (B)



By closing the switch SW, the circuit becomes a parallel oscillator with the wire-inductivity L_X, the debounce capacity C_X, and the damping R_{PD} of the pull-down resistor (It is assumed that it is an ideal power supply, that is, it has no internal resistance).

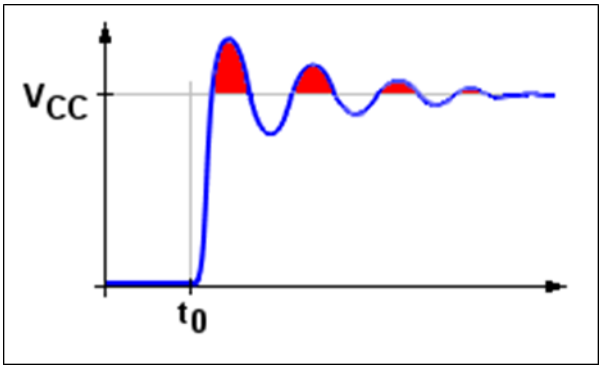
Figure 9. Equivalent Circuit during Closed Switch



R_{PD} is often chosen high (> 50 kΩ), and so its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin (point (B)), as shown in red in Figure 10.

Figure 10. Signal Overshoots on Port Pin after Closing the Switch



These overshoots may cause an internal latch-up on the port pin, as the internal clamping diode connected to internal power supply becomes conductive. Similar is the effect, if the switch SW is opened. In this case, there are under shoots on the port pin.

The frequency of the oscillation can be calculated by Equation 1.

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}}$$ Equation 1

The inductivity LX is an unknown value and depends on the PCB, its routing, and the wire length.

There are two counter measurements to prevent from latch-up.

Solution A:

One solution is to decrease the capacity of the debounce capacitor. This increases the oscillation frequency and the over-all energy of the overshoots is smaller.

Figure 11. Bounce Signal on the Pin with a Large Capacitance

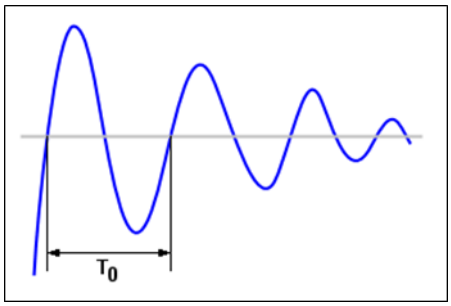
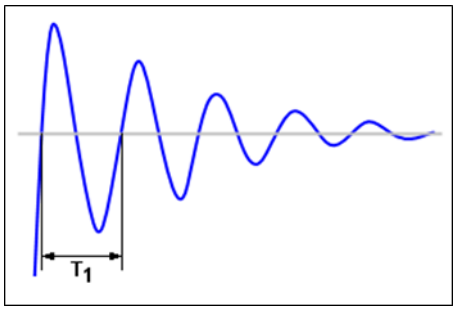


Figure 12. Bounce Signal on the Pin with a Small Capacitance

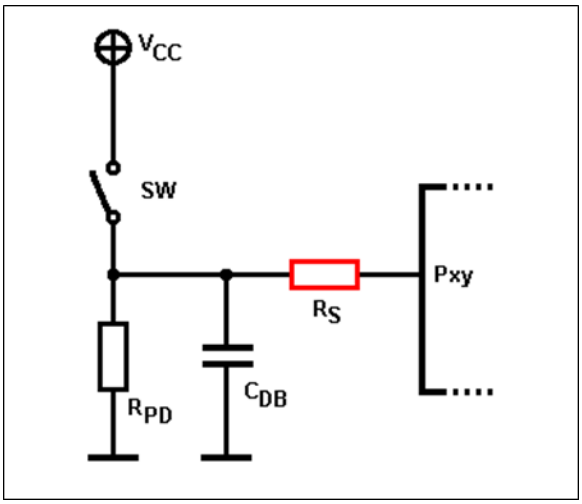


This solution has two disadvantages: the debounce effect decreases and there is no guarantee that the latch-up condition is eliminated.

Solution B: (recommended)

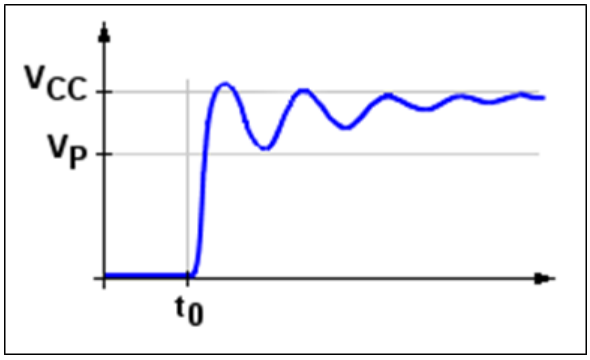
A recommended solution is to use a series resistor (R_S) at the port pin as shown Figure 13.

Figure 13. Recommended Switch Circuit with Series Resistor



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. Do not choose a too high resistor. Otherwise, the port pin input voltage (V_P) will be below the high input level threshold of the dedicated port pin (for example, CMOS/TTL/Automotive level).

Figure 14. Reduction of the Signal Bouncing on the Pin due to the Series Resistor



6.4 5 V Tolerant Input Pins

The MCU does not have 5 V tolerant input pins, if the corresponding I/O domain has a smaller voltage supply (for example, 3.3 V). In case of the deployment of an I^2C bus system with 5 V, and if V_{DDIO} is supplied with 3.3 V, an external level shifter needs to be added to avoid latch-up effect on the MCU pin.

6.5 Reset Behavior of IO Port Pins

During and after the power-on reset (POR), all GPIOs are in high-impedance analog state and the input buffers are disabled. During runtime, GPIOs can be configured by writing to the associated registers. The DAP connection can be disabled or reconfigured for general-purpose use only after the code execution starts.

6.6 Glitch Filtering

The MCU provides the option of internal glitch filtering. As the glitch filters are not available on every port pin, the assignment of wakeup pins needs to be done with caution. Before assigning the wakeup pins, check the number of available glitch filters in the device datasheet.

Analog Filter

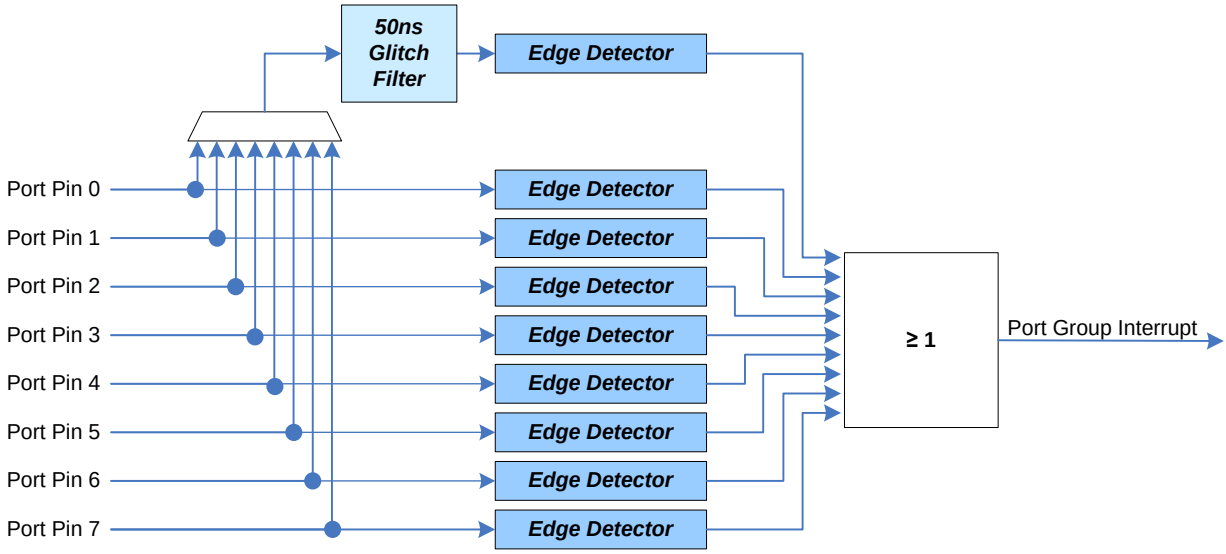
Every port group has one analog filter, which also works in Deep Sleep mode. For details on AC characteristics, see the device datasheet.

Digital Based Filter

The Smart I/O module in the IO system can implement one digital-based filter in dedicated ports. In the DeepSleep mode, either the internal low-speed oscillator (ILO) or the external crystal oscillator (ECO) clock can be selected as the clock source. (see Clock Sources). This means that the minimum filter period is ~30 µs. Additionally, the current consumption increases because a clock is running. For more information, see Smart I/O, I/O System in the Architecture Technical Reference Manual (TRM).

See Latch-up Consideration (Switch) for the latch-up considerations regarding deployed external filters.

Figure 15. Port Glitch Filter and Interrupt Structure



6.7 Mode Pin

A dedicated Mode pin is not required to enter the MCU into programming or normal run mode.

6.8 External Interrupt Input Pins

In general, an external interrupt can be captured by edge detection on every general-purpose I/O (GPIO) port pin. See Glitch Filtering on how to use glitch filtering.

Table 5 lists the wakeup sources in the different power modes. For more details on the power modes, see System Resources Subsystem (SRSS), Device Power Modes in the corresponding TRM.

Table 5. External Interrupt/Wakeup Support in Power Modes

	External Interrupt/Wakeup in Power Mode			
Port Pin Function	**Active**	**Sleep**	**Deep Sleep**	**Hibernate**
GPIO	X	X	X	-
Dedicated peripherals[4]	X	X	X	X
WAKEUP[5]	-	-	-	X

6.9 Clamping Structure of I/O Pins with Shared Analog Function

It is important to identify the power supply domains that must have common supply level in each application. Figure 16 and Table 6 provide the overview of the clamping structure and the consequences when analog input function is used on dedicated power domains. When any port pin of a dedicated power domain (PD) is applied as an analog input, the domain must have the same or lesser voltage level than the analog supply VDDA_ADC. Table 6 lists the special use cases.

General

- Usually the I/O domain, PD_1, deployed is also the same as PD_2, but in some case there are exceptions for PD_2.
- The power domain dependency PD_1 ≤ PD_2 is especially relevant, when PD_1 is a different power domain when compared to PD_2.
- When VDDA_ADC is only on PD_3 and as long as the pin input has **not** started to operate as analog input, PD_1 and PD_2 can be greater than VDDA_ADC. See also Power ON/Power OFF Sequence of Power Supply Domains.

[4] See the Architecture TRM, device datasheet, or both.

[5] The WAKEUP function is supported only on a few pins.

Figure 16. Clamping Structure of I/O Pins with Shared Analog Functions

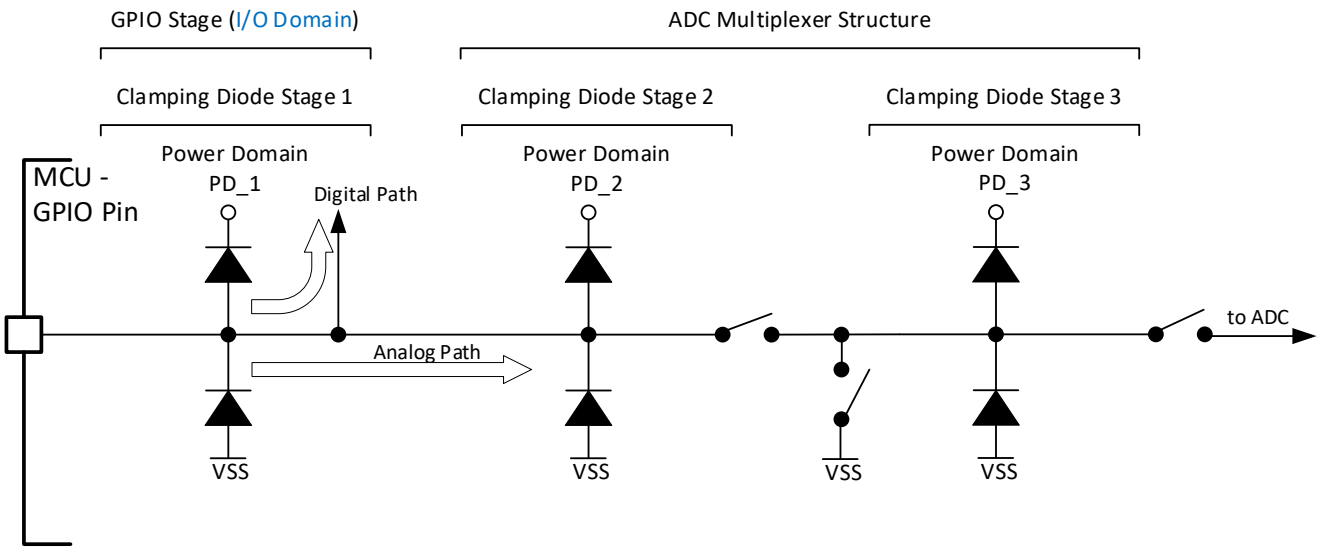


Table 6. Clamping Structure of I/O Pins with Shared Analog Function within CYT2B and CYT4B

PD_1 Port Pins used also as Analog Inputs	Clamping Diode Stages			Required Voltage Level of Power Domain PD_1/2 ≤ VDDA (Same as VDDA)
	Power Domain PD_1 (GPIO Stage)	Power Domain PD_2 (ADC MUX Stage)	Power Domain PD_3 (SAR MUX Stage)	
No (only digital)	VDDIO_1	VDDIO_1	VDDA	No
Yes	VDDIO_1	VDDIO_1	VDDA	Yes
No and Port P11 is **not** in use	VDDIO_2	VDDIO_2	VDDA	No
Yes	VDDIO_2	VDDIO_2	VDDA	No
Not on Port P11, but P11 is in use	VDDIO_2	VDDA	VDDA	Yes
Yes on Port P11, but P11 is in usel	VDDIO_2	VDDA	VDDA	Yes
No (digital only)	VDDD	VDDD	VDDA	No
Yes	VDDD	VDDD	VDDA	Yes

Table 7. Clamping Structure of I/O Pins with Shared Analog Function within CYT3D

PD_1 Port Pins used also as Analog Inputs	Clamping Diode Stages of of I/O Domain (= PD 1)			Required Voltage Level of Power Domain PD_1/2 ≤ VDDA_ADC (Same as VDDA_ADC)
	Power Domain PD_1 (GPIO Stage)	Power Domain PD_2 (ADC MUX Stage)	Power Domain PD_3 (SAR MUX Stage)	
No (digital only)	VDDIO_GPIO1	VDDIO_GPIO1	VDDA	No
Yes	VDDIO_GPIO1	VDDIO_GPIO1	VDDA	Yes
No (digital only)	VDDIO_GPIO2	VDDIO_GPIO1	VDDA	No
Yes	VDDIO_GPIO2	VDDIO_GPIO1	VDDA	Yes
Yes	VDDIO_SMC	VDDIO_SMC	VDDA	Yes

6.10 FPD-Link

The FPD differential data output signal pairs FPDx_TyP/N can be freely configured. This gives the advantage of avoiding signal pair crossing via changing the PCB layers for the signal routing to the display connector. However, the FPD clock signal pair is on fixed pinning.

7 Flash Programming Connection

The Flash programming can be done with the JTAG/SWD connection. Due to this fact, no mode pins are available to switch the device into a programming mode after power-on reset. See Debug Interface.

for information on the debug connections. There is also the option to use dedicated LIN and the CAN channels for the mass production programming.

8 Debug Interface

There are several options to connect the debug system to the MCU depending on the debug requirements and the tool chain support. The following are the debug connectors:

- Legacy 20-pin IDC JTAG Connector
- 10-pin Cortex Debug Connector
- 20-pin Cortex Debug+ETM Connector

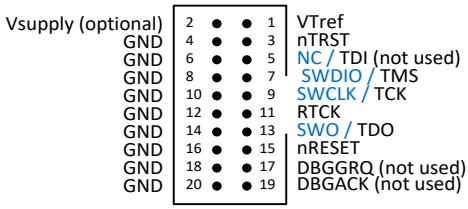
In all these connectors, the JTAG and SWD signals are shared. The differences are indicated by marking the Serial Wire Debug (SWD) protocol signals in blue. For more information on the interface signals, see Chapter 11 of the CoreSight Components Technical Reference Manual.

Legacy 20-pin IDC JTAG Connector

The legacy JTAG Interface is used for Flash programming and debugging. The JTAG signal RTCK is not available on the MCU. Additionally, the SWD signals can be shared.

Note: The JTAG interface terminates in a 20-way, 2.54 mm pitch IDC-connector (for example, Hirose HIF3FC-20PA-2.54DSA).

Figure 17. Legacy 20-pin IDC JTAG Connector



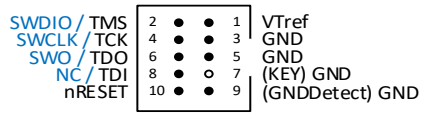
10-pin Cortex Debug Connector

To use the SWD debug interface, a 10-pin MIPI connector is defined with the minimum number of signals, which are required for debugging. The JTAG interface signals are replaced by the bidirectional data signal (SWDIO) and the clock signal (SWCLK). The freed up TDO signal can be re-used as a system trace data output serial wire output (SWO).

Note:

- For the SWD debugging a 10-way connector with 1.27 mm pitch is applied (for example, Samtech FTSH-105-01-L-DV-K).
- Position 7 (KEY) has no pin and serves only as a key to properly orient the connector.

Figure 18. 10-pin Cortex Debug Connector



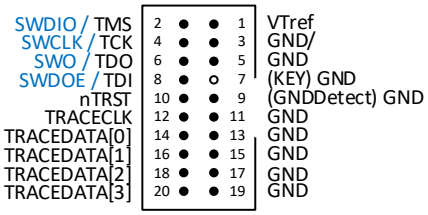
20-pin Cortex Debug+ETM Connector

Besides JTAG debugging and SWD debugging, this connector is used to connect a signal trace probe for the Embedded Trace Macrocell (ETM) instruction trace operations.

Note:

- As a connector, a 20-way 1.27mm pitch IDC-connector is applied (for example, Samtech FTSH-110-01-L-DV-K).
- Position 7 (KEY) has no pin and serves only as a key to properly orient the connector.

Figure 19. 20-pin Cortex Debug+ETM Connector



Termination Resistors

In general, the debug connection needs termination resistors for a proper communication. External termination resistors should not be required for this MCU, because after power-on reset per default JTAG IF is enabled in the boot ROM. If externals are applied on the board, then each external signal termination must in the same direction, as it is done in the device implementation. Although the JTAG IF is enabled by after reset, the SWD mode can be enabled afterwards by establishing the SWD connection.

Table 8. Termination Resistor for Debug IF

JTAG Mode	SWD Mode	Signal	Required Termination Resistor (If N/A in the MCU)	MCU Implementation
TCK	SWCLK	Clock into debug core	10 k – 100 kΩ pull-down resistor to GND	Pull-down resistor
TDI	-	JTAG Test Data Input	10 k – 100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
TDO	SWO	JTAG Test Data Output, SWV Trace Data Output	10 k – 100 kΩ pull-up resistor to V_{DDIO}	None. Termination, push-pull driver implemented.
TMS	SWDIO	JTAG Test Mode Select, SWD Data In / Out	10 k – 100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
nTRST	-	JTAG TAP reset (low active)	10 k – 100 kΩ pull-up resistor to V_{DDIO}	Pull-up resistor
GND	GND	Connection to system ground	-	-

Figure 20 and Figure 21 show how to connect the debug connector to the MCU. In general, it is recommended to place a series resistor R16 closer to the connector to avoid reflections and ringing of the debug clock signal. Otherwise, with strong oscillations during the level settlement, the debug I/F can interpret wrong data. It must be considered that due to the internal termination resistor, a possible voltage divider in the debug clock signal might be created.

Figure 20. JTAG Debug Connection to the MCU with 20-pin IDC Connector

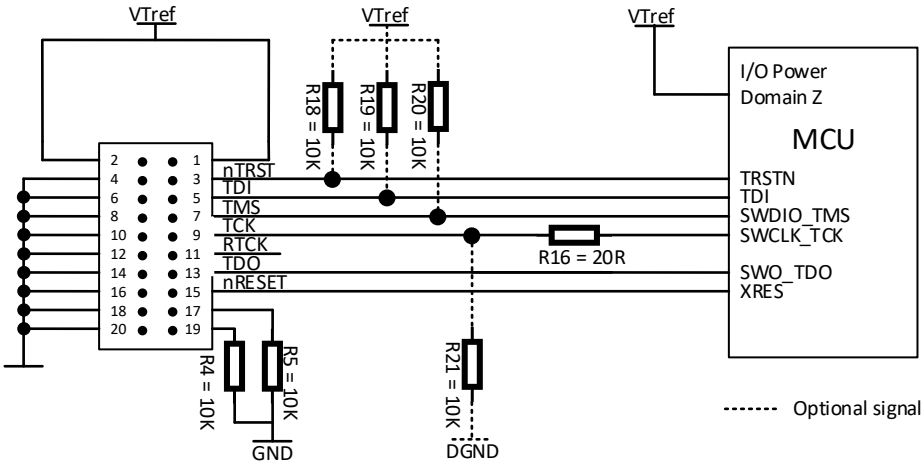
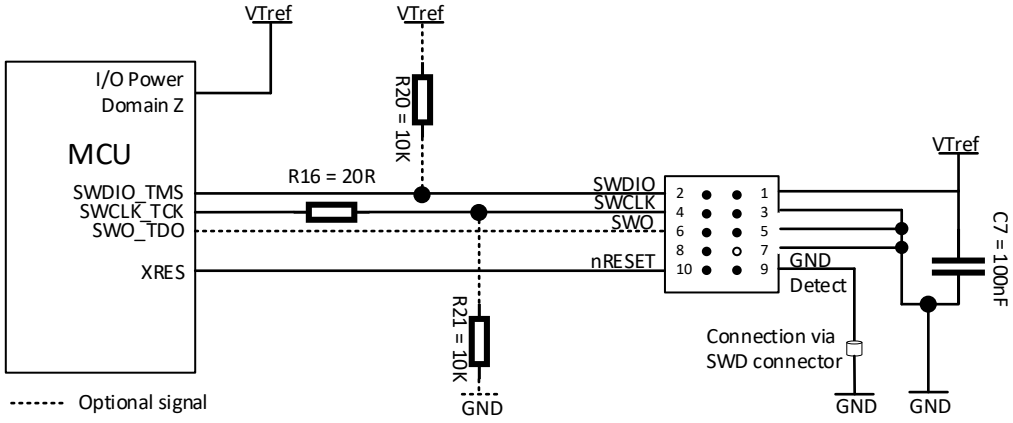


Figure 21. SWD Debug Connection to the MCU with 10-pin MIPI SWD Debug Connector



Note:

- When SWD is used as debug IF instead of JTAG, there is time slot after reset and in between boot ROM and user pin configuration, in which the unused JTAG pins are configured according to the JTAG communication. When these unused JTAGs pins are used in an application, make sure that the peripherals on the ECU are not negatively affected.
- It is recommended to check the debug connection. that is supported by the vendors for Flash programming and debugging. Also, check for the target board supply and the supported power supply level of the vendor's hardware. In case of a power supply mismatch, an adapter is required.
- Boundary-scan is only supported on JTAG IF, not on SWD.

9 Clock Output Function

You might need to cross-check the MCU internal clock signals for evaluation purposes. You can cross-check with the following options:

- EXT_CLK port pin
- Alternate output function pin

EXT_CLK Port Pin

Internal clocks can be routed through a divider to the alternate function port pin EXT_CLK as clock output function. It must be taken into consideration that the macro Event Generator (EVTGEN) and EXT_CLK are driven by the same internal clock signal CLK_HF1. So, when the divided ECO signal should be observed at the EXT_CLK pin, then the EVTGEN is also driven with the ECO clock accordingly and this might have impact to the application. The EXT_CLK pin is a bi-directional pin and can be also used as external clock source. See Clock Sources for more information about this pin.

As the MCU clock output functionality drives fast digital signal, this signal must be routed far away from the analog input and the analog voltage reference signals.

Alternate Function Pin

The system clocks can be implicitly observed by using a PWM signal coming from a TCPWM output channel for instance. It must be taken into consideration that each TCPWM channel input clock is derived by a dedicated clock divider of the peripheral clock. See Clocking System in the TRM for more details on the clock tree.

10 Layout and Electromagnetic Compatibility

10.1 General

To avoid ESD problems and noise emission of the system, consider some rules for the layout design.

The most critical point is the VCCD pin, as this is the connection to the internal supply for the MCU core. The required decoupling capacitors (DeCaps) must be placed as close as possible to this pin. Usually a bigger buffer or bypass capacitor of µF range is added to the dedicated power domain to bypass the period of time until the capacitors are recharged again. Otherwise DeCaps and finally the system fall below the power supply operating range.

As the MCU has different digital supply rails, the routing of power supply traces must be done carefully. The supply traces should be routed in a star shape or as digital plane in the middle layer. A digital ground plane in the middle layer or on the mounting side just under the MCU is recommended. Decoupling capacitors should be assembled as near as possible to the related pins. If these capacitors are placed too far away, their functionality becomes useless.

If possible, all decoupling capacitors should be placed on the same mounting side as the MCU. Alternatively, the DeCaps could be placed on the bottom layer below the paired power supply pins (for example, VDD/VSS pair).

The analog supply should be decoupled from the digital supply and a common ground star point should be as far as possible from the MCU. In the hardware design, make sure that no latch up effect between the digital and analog supply or between analog and digital ground can occur. Therefore, the impedance between the different VSS pins and between analog ground and analog reference input need to be as low as possible.

10.2 Power Supply Pins

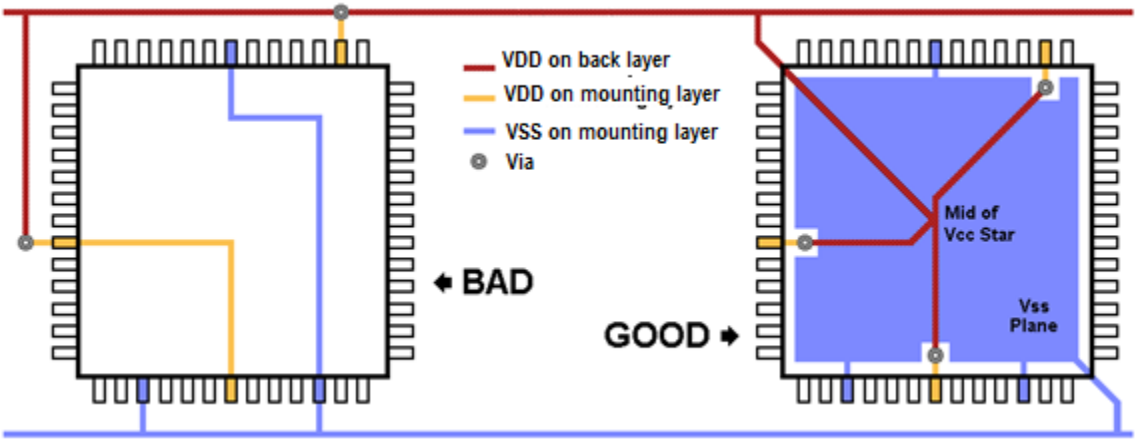
All power supply pins, listed in Table 2, are EMC critical pins and DeCaps are required to ensure the correct operation of the MCU. See General regarding recommendations about the placement of the DeCaps.

10.3 Ground and Power Supply

In general, the corresponding VDD and VSS lines should not be routed in chains, but in star shape.

Figure 22 is a principal example of a bad and a good power line routing.

Figure 22. Generic Example of Bad vs. Good Power Line Routing



For a multi-layer PCB, the VDD and VSSD should be routed as a plane in the inner layers of PCB. Considering a layer stack with several power supply planes, these planes should not overlap to avoid noise coupling.

Here are some recommendations for good EMC behavior:

- Use a multi-layer PCB
- Use power supply planes (ground and power) in the inner-layer of PCB layer stack.
- Place one or two decoupling capacitors close to each corresponding supply pin pair to reduce the possible radiation.
- Use capacitor groups to match frequency behavior of power supply decoupling. The decoupling capacitors can have values between 1 nF and 10 µF.
- Make sure that only one common star point connects analog and digital ground planes to each other. To have less noise on the analog part, the star point should be placed as far as possible from the MCU and as close as possible to the voltage regulator capacitor resp. to the Electronic Control Unit (ECU) connector.
- Make sure that the digital and analog planes do not overlap and interfere. Furthermore, there should be no signal plane between these planes.
- Shield the analog input signals by the analog ground as much as possible.
- Avoid ground loops.
- Make sure that the supply traces with a layer changeover have at least two vias.

Figure 23 shows an example of a bad PCB Layer Stack, as there might be crosstalk between different power supply planes. However, Figure 24 is an example of well-designed PCB layer stack in which the analog and digital supply planes are separated in the common layer. Thus, the EMC behavior of the board is already improved.

Figure 23. Example of a Bad PCB Layer Stack

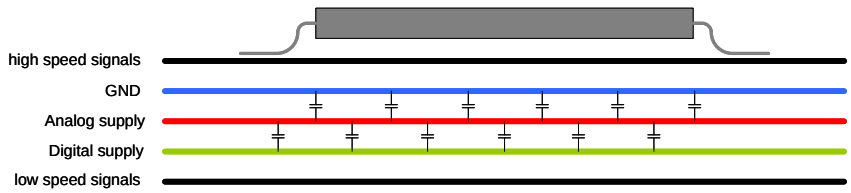
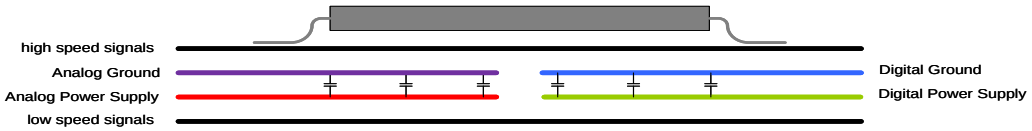


Figure 24. Example of a Good PCB Layer Stack



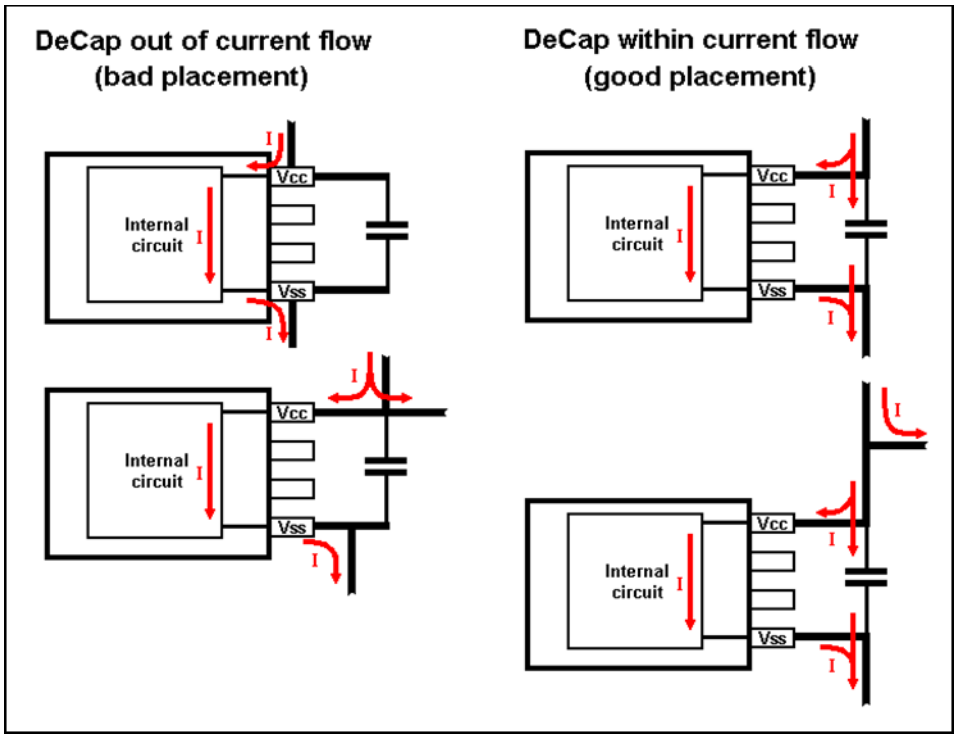
10.4 Power Supply Decoupling

10.4.1 Placement

In general, the DeCaps should be placed as close as possible to MCU. When a small ceramic capacitor is used together with a large electrolytic capacitor for decoupling, then place the ceramic capacitor closer to the MCU power supply rail than the electrolytic capacitor.

DeCaps for power supply must be placed within the current flow. If not, they are useless as their function becomes less efficient as shown in Figure 25. As the description is valid for generic use, as shown in Figure 25 to Figure 27, the generic naming convention for power supply pins is VCC and for ground pins is VSS.

Figure 25. Power Supply Decoupling Capacitor Placement



Usually the noise current should flow through the soldering pad of decoupling capacitor CB. Figure 26 shows the recommended routing and placement on the boards.

Figure 26. Recommended Power Supply Decoupling on Boards

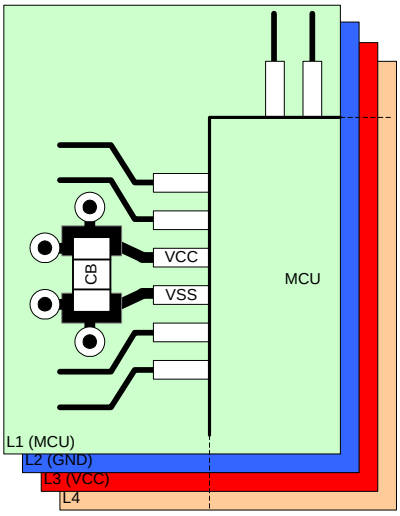
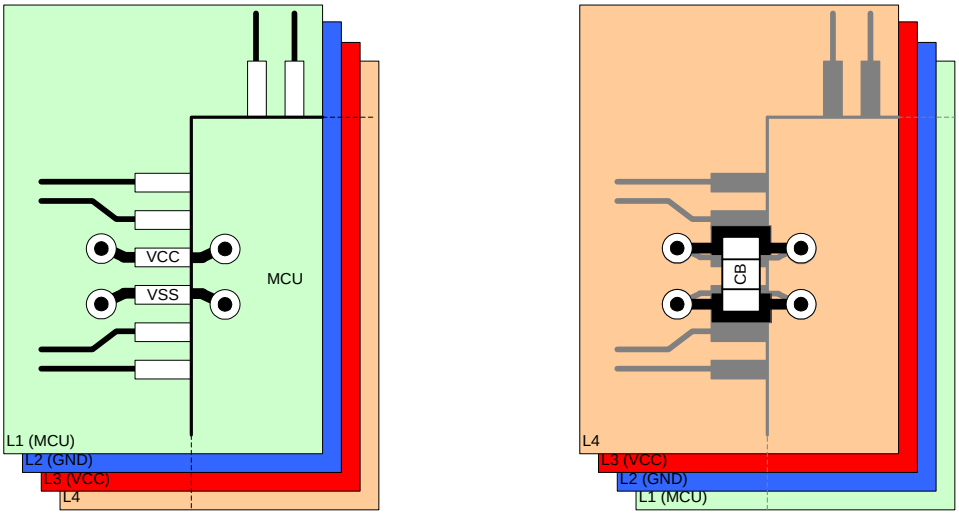


Figure 27 shows an alternate, but not recommended routing and placement. Note that the capacitor is placed on the opposite PCB side like the MCU. This solution is the best for high-density board assembly.

Figure 27. Alternate Power Supply Decoupling on Boards



10.4.2 I/O Domains

The dimensioning of the DeCaps and Bypass capacitors for the I/O domain is application specific. The following are some points to be considered while dimensioning:

- How is the switching behavior (periodic or random) of the output stages and what is the transition requirement?
- How many outputs have the same transition at the same time during the running operation or after any wake up or reset?
- How big is the capacitive load at one output pin?
- Which driver strength configuration is selected?
- Is there any DC current caused by resistors, which might be also buffered by big bypass capacitor?

It is strongly recommended to make either a Power Distribution Network (PDN) analysis with an according model (IBIS or lumped model) or test on the PCB. A simplified consideration about the decoupling is provided in the document SRAM Board Design Guidelines.

10.5 Quartz Crystal Placement and Signal Routing

The MCU provides two pierce oscillators implementations with an embedded feedback resistor (Rf) for the ECO and external watch oscillator (WCO). You can enable both oscillators by software. That means the MCU starts the boot process from an internal clock source.

Note: Figure 28 to Figure 31 showing the implementation of oscillator implementations in the family and the trimming features discussed in this application note might differ from the dedicated device architecture TRM. Due to different trimming features in the external BOM cost can be reduced in the ECU design.

Setup

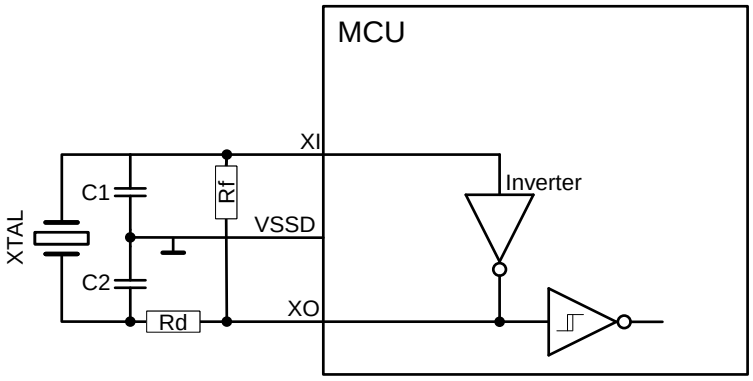
Figure 28 shows the principle of an external oscillator circuit. The feedback resistor (Rf) is required to act the inverter as an amplifier. Optionally, a damping resistor (Rd) is required for drivel level (DL) reduction. If the DL is too strong, the crystal can be damaged over life time. The load capacitance C_L is the terminal capacitance and is connected to the crystal. Thereby, C_L includes the external capacitors C1 and C2 and the stray capacitance C_S. C_S comes from the PCB layout, the manufacturing tolerances, and the oscillator MCU pins. As the stray capacitance is usually ~4 pF for each signal line, C1 and C2 should have 8 pF or more to stabilize the frequency. The value of both load capacitors (C1 and C2) should be determined with a crystal matching test. The crystal matching test must always be done by the crystal manufacturer when there is any change on the target board affecting the oscillator circuit.

Load Capacitance C_L

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_S$$

Equation 2

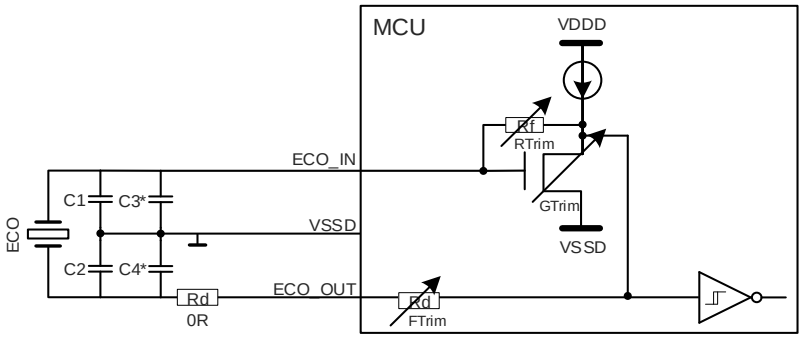
Figure 28. Principle Setup of an External Oscillator Circuit



XI: Oscillator Input Pin
XO: Oscillator Output Pin
C1, C2: Load Capacitors
C_S: Stray Capacitance of the PCB and the connections

The ECO design is optimized for BOM costs reduction (see Figure 29). This is realized by a scalable DL and an embedded Rf implementation. By trimming features, a broad crystal frequency range can be supported. For more details, see Clock Sources in the Architecture TRM.

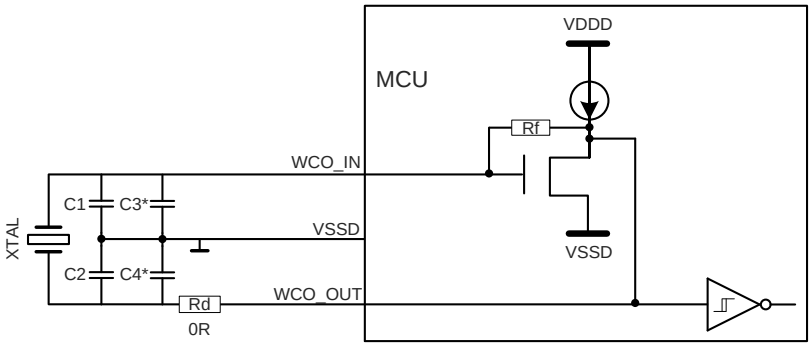
Figure 29. ECO Circuit Scheme[6]



ECO_IN: External crystal oscillator input pin
ECO_OUT: External crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB

The WCO implementation scheme is shown in Figure 30. Like in the ECO, Rf is embedded to reduce the external BOM costs. An external Rd might be required, to avoid a damage of the external watch crystal.

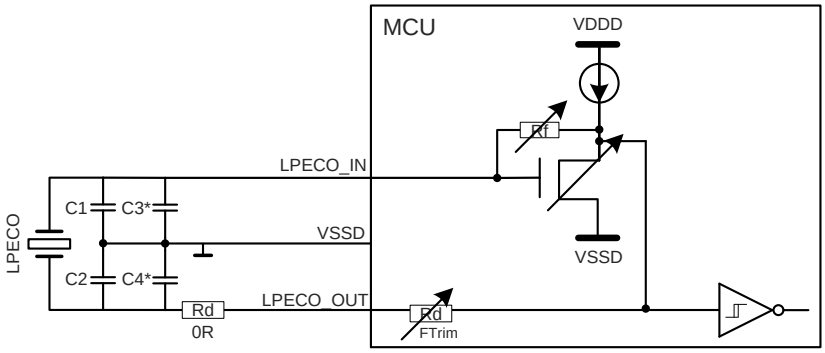
Figure 30. WCO Circuit Scheme[6]



WCO_IN: Watch crystal oscillator input pin
WCO_OUT: Watch crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB

The LPECO design is optimized for BOM costs reduction (see Figure 31). This is realized by a scalable DL and an embedded Rf implementation.

Figure 31. LPECO Circuit Scheme[6]



LPECO_IN: External crystal oscillator input pin
LPECO_OUT: External crystal oscillator output pin
C1, C2: Load Capacitors
C3*, C4*: Stray Capacitance of the PCB

[6] Figure might differ from dedicated Architecture TRM. Trimming features are not covered 100%.

PCB Design

To reduce the impact of the EMI effects, the placement of the external oscillator components and the signal routing must be done carefully. The following items should be consideration during the PCB layouts. Due to design constraints it might be required, to make a tradeoff between the items.

- Stable Frequency
  - Place the external oscillator components on the MCU layer.
  - Place the external oscillator components as close as possible to the MCU.
  - Make sure that the connection of the load capacitors C1 and C2 to the oscillator ground should be in a common star point.
  - Make sure that there is no signal line between both capacitor ground connections.
  - Do not use vias for ground signal routing.
- Noise Injection
  - Use a ground layer directly below the MCU.
  - Use a ground shield in the MCU layer and use the neighbor layer as ground layer.
  - Shield the area of the oscillator bonding wires.
  - Do not use the ground shield as oscillator ground signal.
  - Avoid ground loops. The oscillator ground signal must be connected at first to VSSD before connecting to the system ground.
  - Make sure that the routing of the oscillator ground to VSSD is as short as possible.
  - Do not route signals with strong pulses close to the oscillator. This is also valid for the neighbor layer.
- Noise Emission
  - Do not route sensitive signals close to the oscillator signals (example: analog sensor signals).

10.6 Component Placement

- The placement of analog components should be done in a way that the ground connection is on a common partition area. The same should be also done for digital components. The analog voltage reference regulator should be placed over the analog plane and the digital voltage regulator accordingly over the digital plane.
- Components with a common power supply should be located as centrally as possible to each other.
- The MCU and other mixed signal components should accordingly be placed on the PCB as bridge between the analog and digital partitions.

10.7 Signal Routing

- Digital power and signal traces should be routed over the digital ground planes and analog power and signal traces should be routed over the analog ground plane.
- To isolate analog signals traces, areas around the traces should be filled with copper, which are connected to analog ground plane. Accordingly, the same recommendation is also valid for areas with digital signal traces.
- Do not route traces near to or parallel to other noisy and sensitive traces.
- Keep the trace lengths as short as possible.

Furthermore, when designing an application, the following areas should be closely studied to improve the EMC performance:

- Noisy signals, for example, signals with fast edge times
- Sensitive and high-impedance signals
- Signals that capture events, such as interrupts and strobe signals

11 Thermal Considerations

Once an indication of the MCU total power requirement is known, it is very important to understand, if the system design can properly dissipate this power into the ambient air efficiently enough, to require no further action or if significant heat sinking and PCB design choices might be required. The Cypress MCUs cover a wide range of products from devices capable of very low power to MCUs with very fast complex logic requiring higher power needs. Under certain conditions, MCUs may dissipate more than 1 Watt of power including the core, peripheral, and I/O currents. With a lot of power in a device, necessary steps must be considered to avoid it from overheating. Before a design is finalized, a complete thermal review should be done. Items such as the amount of airflow through the system, nearby heat sources, and PCB construction should be reviewed. The examples given below are first steps to determine, whether the preliminary design objectives can be met by taking the equation.

Calculation of Junction Temperature

$$T_J = T_A + \Theta_{JA} \times P_D \qquad \text{Equation 3}$$

T_J: Junction Temperature

T_A: Ambient Temperature

Θ_{JA}: Thermal Resistance from Junction to Ambient

P_D: Power Dissipation

For a first order approximation, first check the datasheet for the thermal resistance from junction to ambient (θ_{JA}) for the target device package. θ_{JA} is expressed in units of °C/watt. For example, the θ_{JA} for an LQFP 120-pin is 38 °C/watt. For the same device in an LQFP 120-pin package with an exposed pad on the bottom side correctly mounted, the θ_{JA} is reduced to 18 °C/watt, allowing a much higher total device power usage or a higher ambient operating temperature.

The maximum temperature difference between the device junction and the ambient air surrounding the device is θ_{JA} times the maximum power, or as in the first case above 38 °C/watt x 1.0 watt = 38 °C. Because the specified maximum operating junction temperature of the device is 125°C, the maximum allowable ambient air temperature is 125 – 38 = 87 °C. If you use the exposed pad version of package, which has a lower thermal resistance θ_{JA} of 18°C/watt if implemented with proper PCB to pad design, then the maximum allowable ambient air temperature is 125 °C – 18 °C = 107 °C. This allows a 20 °C increase in ambient operating temperature or the possibility to drive more power from the device I/O or core.

Each datasheet for a device series contains a table showing package thermal resistance and maximum permissible power. This allows you to quickly see the amount of power, that can practically be consumed by a device in a given package. In the DS recommended minimal PCB construction might be given. So, for instance a four-layer PCB has a better power dissipation characteristic than a two-layer PCB, because inner plane layers help to dissipate the heat.

Note: The datasheet specifications for θJA are typical. The ambient air temperature should be much less than the allowable maximum for the product design.

Note: With the above calculation, if the θJA or the power dissipated is high, the maximum allowable ambient air temperature could theoretically approach the 125°C junction temperature limit. However, the product's commercial-range ambient air temperature limit of 85°C or the industrial-range ambient air temperature limit of 105°C still applies. In the example above, the first example would be unacceptable for operating a consumer grade (85°C) device. In the second example, a consumer grade or industrial grade device would be well suited depending on the choice of operating conditions of the final product.

MCU offered in BGA or QFN packages have a reduced available surface area for thermal conduction due to the small package size, these packages must be thoroughly reviewed for power applications.

Detailed information is provided in the application notes AN72845, AN202751, and AN79938 listed in Related Documents.

12 ADC

This section considers ADC and its analog input (AN) circuit for high accurate sampling of the analog sensor level and protentional other issues.

12.1 Filter Design Consideration for Analog Inputs

12.1.1 Principle of the Acquisition

The full period of sampling the analog value and then the conversion into a digital value is called acquisition time (t_{ACQ}). The voltage level of analog input is sampled by an internal sample capacitor (C_{VIN}) within a configurable sample time (t_S), the conversion time (t_{CNV}) is implicitly configurable by the ADC clock input.

Figure 32 shows a principle circuit between the sensor, the analog source V_0, and the analog input.

$$t_{ACQ} = t_S + t_{CNV}$$ Equation 4

Figure 32. Analog with Optional External Buffer Capacitor

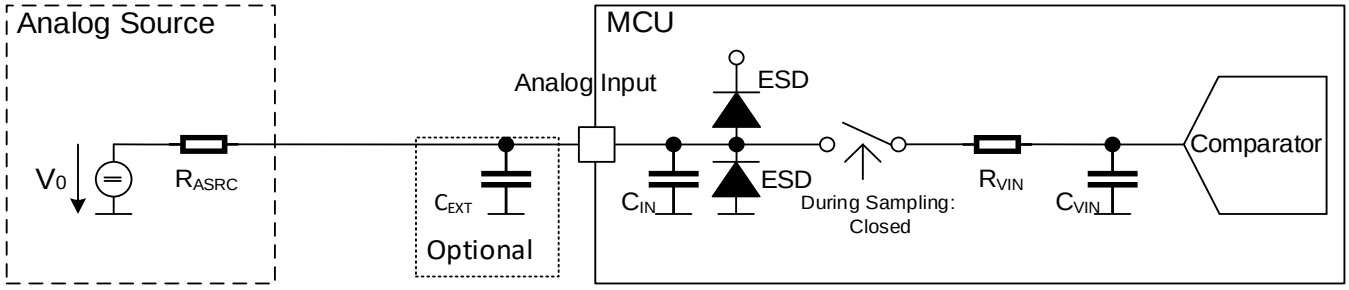
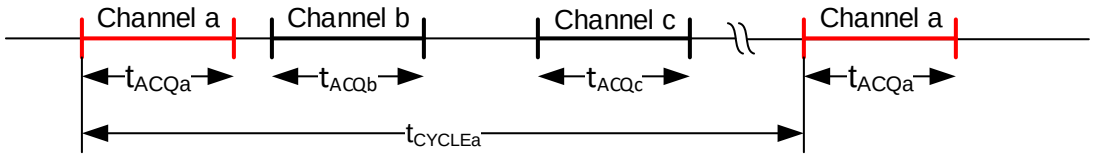


Figure 33. Cycle Time of Analog Channels



t_{ACQ} : Acquisition Time [sample time (t_S) + conversion time (t_{CNV})
t_{CYCLE} : Cycle time of one analog input/channel

12.1.2 Accuracy at Sample Time

The sample time (t_S) must be long enough for charging C_{VIN} on the same level as the analog source, which means that that the internal resistance of the analog source (R_{ASRC}) should be usually small enough. When the R_{ASRC} is too high, either the sample time must be longer which has an impact on the total sample rate of all channels or the cycle time (t_{CYCLE}), the period between two acquisitions of a channel, must be longer accordingly (see Figure 32). After the cycle time, there should be either no or a neglectable voltage difference between the analog source V_0 and the analog input AN before the next acquisition. When a channel is sampled twice or more directly one after the other, the following equation must be fulfilled: $t_{CYCLE} \leq t_{ACQ}$.

The following are the assumptions to be considered while calculating the cycle time t_{CYCLE}:

- The analog input must be reloaded to a new source level V_0 with a remaining voltage difference V_R depending on the required resolution 2^r. V_R should be smaller than the sampled error.
- The reloading from the external capacitor C_{EXT} to internal sample capacitor C_{VIN} during the sample time extends the cycle time.

$$t_{CYCLE} = t_S + k \times \tau = t_S + \ln\left(\frac{2^r}{V_{R,LSB}}\right) \times \left(R_{ASRC} \times (C_{EXT} + C_{IN})\right)$$ Equation 5

Example:

Resolution: 12-bit

$V_{R,LSB}$: 0.25 LSB = 0.25 x ($1/2^{12}$)

$$t_{CYCLE} = t_S + k \times \tau = t_S + \ln\left(\frac{2^{12}}{0.25}\right) \times \left(R_{ASRC} \times (C_{EXT} + C_{IN})\right) = t_S + 9.7 \times \tau$$ Equation 6

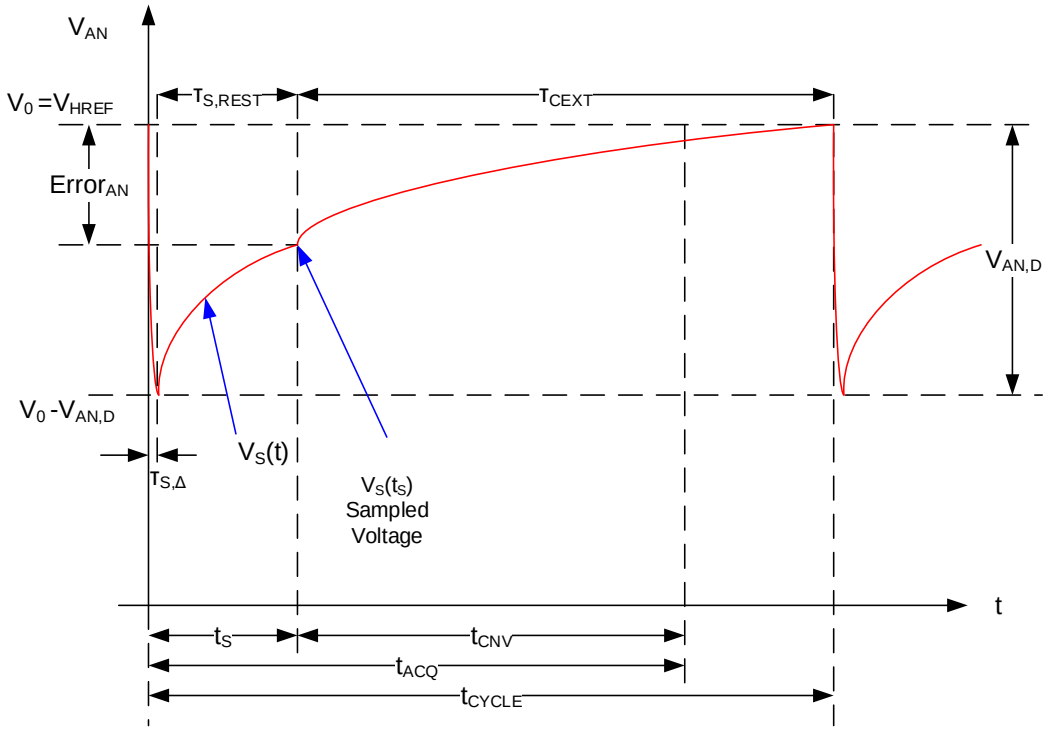
12.1.3 Sample Time Charging Process

During the sample phase, the sample capacitor C_{VIN} is charged by the external capacitor C_{EXT} until both reach a common voltage (charge balancing). After that both capacitors are charged to analog source level V_0 via the source resistance.

So, different time constants must be considered:

- $T_{S,\Delta}$: Time constant at the beginning of the sample time for the charge balancing between C_{EXT} and C_{VIN}.
- $T_{S,REST}$: Time constant during sample time, after the charge balancing, to charge closely to V_0 with an acceptable error.
- T_{CEXT}: Time constant, starting from the conversion time and ending with the next sample phase of the analog input.

Figure 34. Charging Curve of Analog Input during Acquisition Time



t_s : Sample time (t_S)
t_{ACQ} : Acquisition time
t_{CYCLE} : Cycle time of one analog input/channel
$\tau_{S,D}$: Time constant for the charge balancing between C_{EXT} and C_{VIN} causing a voltage drop during sample time
$\tau_{S,REST}$: Time constant for charging C_{EXT} and C_{VIN} by analog source V_0 for the rest of the sample time
τ_{CEXT} : Time constant for C_{EXT} only after sample time
V_0 : Voltage of the analog source
$V_S(t)$: Voltage level at analog input during sample time
t_{CNV} : Conversion time
$V_{AN,D}$: Voltage drop caused at analog input due to the charge balancing during the sample time
$Error_{AN}$: Voltage error between sample voltage and analog source voltage level

12.1.4 Charge Balancing between C_{EXT} and C_{VIN}

Depending on the ADC macro implementation, the sample capacitor can be precharged to a target level ($C_{VIN, PRE}$) before starting the sample phase. If this feature is not deployed, C_{VIN} will have the voltage level of the previous acquisition, which means that in the worst case, the maximum voltage difference ($\Delta V_{CVIN, PRE}$) between C_{VIN} and the external capacitor C_{EXT}

corresponds to the analog reference voltage V_{REFH}. When the sample switch is closed, the charge balancing between the external capacitor C_{EXT} and the sample capacitor C_{VIN} causes a voltage drop at the analog input $V_{AN, D}$.

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times (V_0 - V_{VIN,PRE})}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times \Delta V_{VIN,PRE}}{(C_{IN} + C_{EXT}) + C_{VIN}}$$

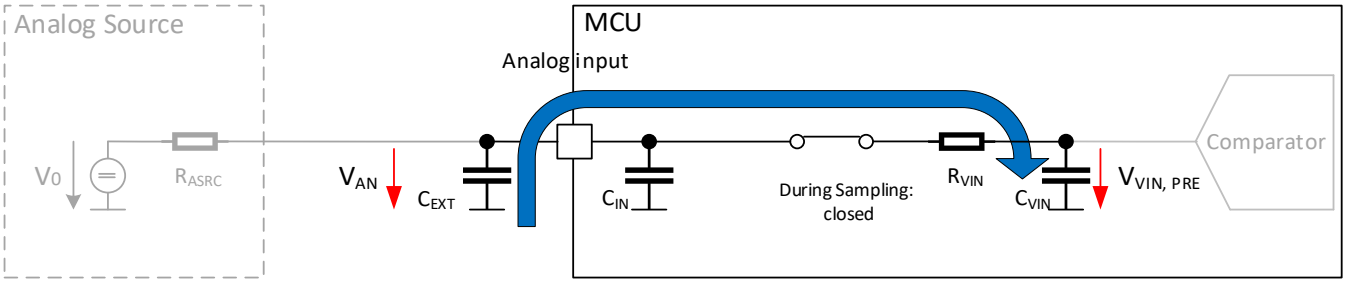
Equation 7

In simplified consideration of Equation 7, the analog input and the analog source have the same voltage level $V_{AN} = V_0$, resulting in Equation 8.

$$V_{AN,D} = \frac{Q_{VIN}}{(C_{IN} + C_{EXT}) + C_{VIN}} = \frac{C_{VIN} \times (V_0 - V_{VIN,PRE})}{(C_{IN} + C_{EXT}) + C_{VIN}}$$

Equation 8

Figure 35. Charge Balancing during ADC Sample Time



While this charge balancing happens, it is assumed that $R_{ASRC} >> R_{VIN,}$ and therefore R_{ASRC} has no impact during that phase. This results in the following time constant $\tau_{S,\Delta}$ for charging the capacitor:

$$\tau_{S,D} = R_{VIN} \times C_{SUM} = R_{VIN} \times \left(\frac{1}{1/(C_{EXT} + C_{IN}) + 1/C_{VIN}} \right)$$

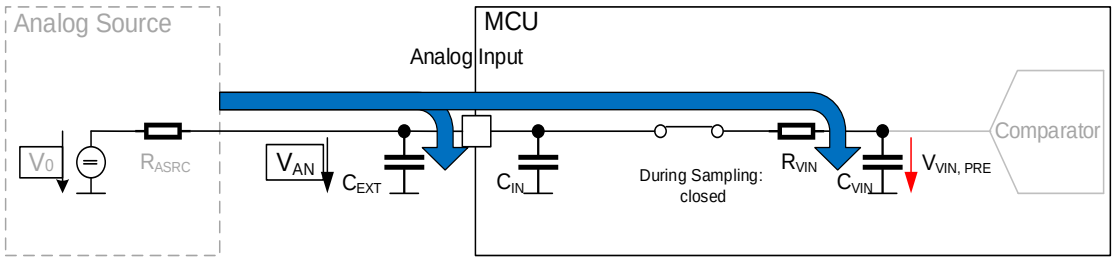
Equation 9

So in the worst scenario regarding the maximum voltage difference between analog input and the sample capacitor after $9.7 * \tau_{S,\Delta}$, the voltage error of the analog input is less than 0.25 LSB_{12}.

12.1.5 Charging Analog Input by Analog Source V_0

Depending on the dimensioning of the external capacitor C_{EXT}, the charge balancing between C_{EXT} and C_{VIN} causes a huge voltage difference in the analog input in relation to the analog source V_0, and the analog input must be charged by V_0 itself directly. In this case, the analog source resistance R_{ASRC} has a relevant influence for the charging curve.

Figure 36. Charging of Analog Input during Sample Time by the Analog Source V_0



So for the rest of the sample time, the time constant $\tau_{S,REST}$ is calculated as follows:

$$\tau_{S,REST} = \left(R_{VIN} + R_{ARSC}\right) \times C_{VIN} + R_{ARSC} \times \left(C_{EXT} + C_{IN}\right)$$

Equation 10

12.1.6 Filter Case: $C_{EXT} > 2^r * C_{VIN}$

When the analog source impedance is too high, the sampling period for analog voltages may be insufficient, especially when all analog input needs to be sampled with a common high sample rate (for example, 1 MS/s). If the cyclic sampling of the dedicated analog input, the cycle time (t_{CYCLE}), can be much longer than a big external buffer capacitor C_{EXT} can be deployed. The dimensioning considers the maximal target error at the sampled analog input $Error_{AN}$.

Figure 37. Analog Input with Decoupling Capacitor against Internal Switching Noise

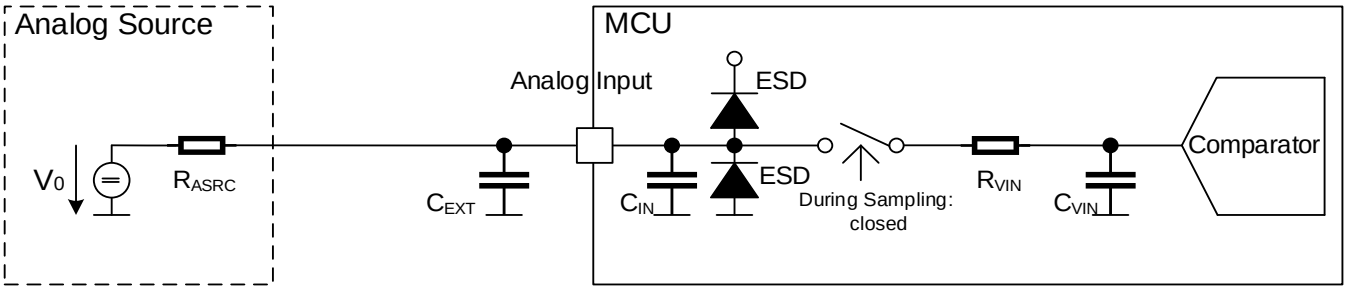
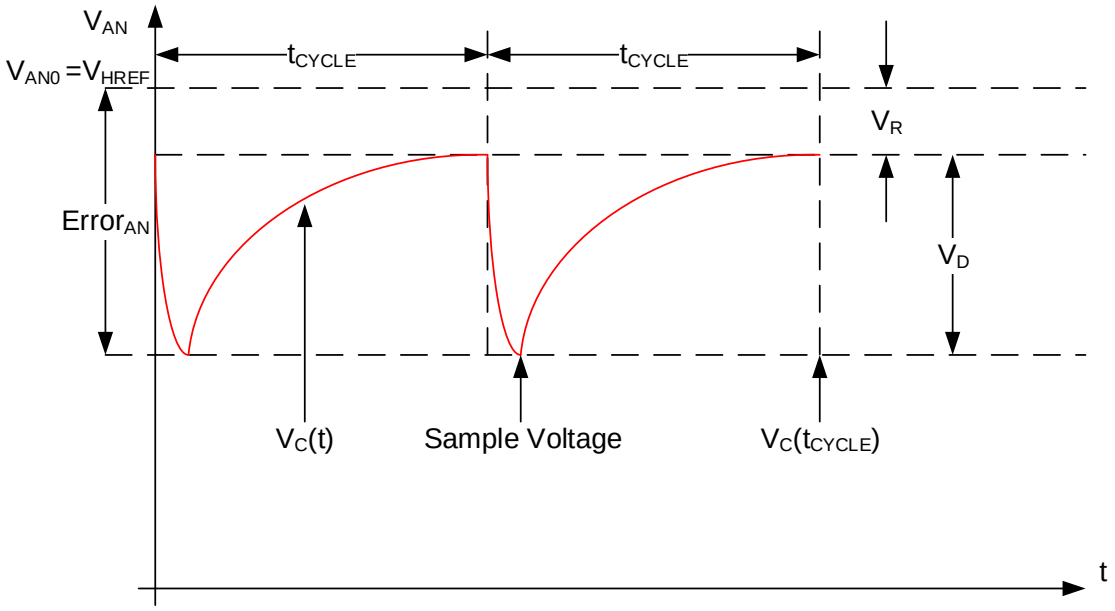


Figure 38. Simplified Cyclic Charge Curve of C_{EXT} for Use Case CEXT > 2r * CVIN



t_{CYCLE} : Cycle time of one analog input / channel
V_0 : Voltage of the analog source
V_R : Remaining voltage at the end of t_{CYCLE}
$V_C(t)$: Charge curve for C_{EXT}
V_D : Voltage drop at the beginning of the sample phase due to charging vom C_{EXT} to sample capacitor C_{VIN}
$Error_{AN}$: Voltage error between sample voltage and analog source voltage level

At first a maximum permitted error $Error_{AN}$ must be defined as shown in Equation 11.

$$Error_{AN} = 1/2^{E} \times LSB_r \qquad \text{Equation 11}$$

with:

r = 12: 12-bit resolution E = 0; ErrorAN = 1 LSBr

r = 12: 12-bit resolution E = 1; ErrorAN = LSBr / 2

r = 12: 12-bit resolution E = 2; ErrorAN = LSBr / 4

$$C_{EXT} = 2^{r+E} \times C_{VIN}$$ Equation 12

To achieve a sampling error of less than 0.25 LSB (E = 2) at 12-bit resolution (r = 12), the minimum external filter capacitor C_{EXT} is as shown in Equation 13.

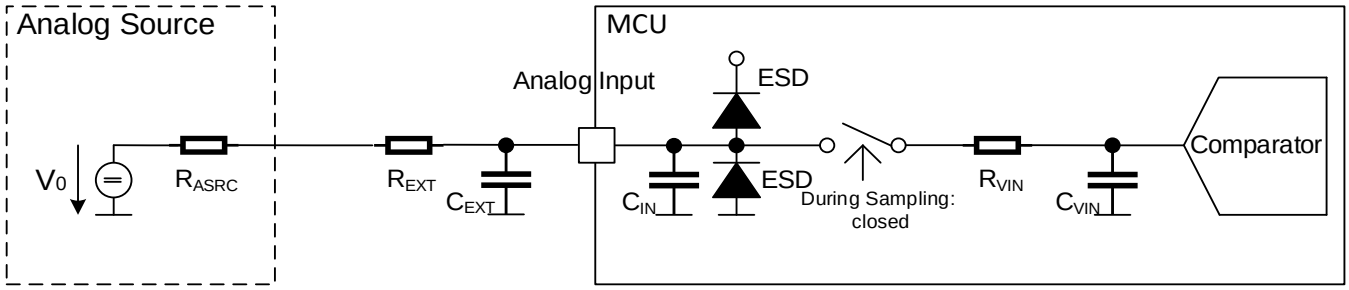
$$C_{EXT,0.25LSB} \geq 2^{r+E} \times C_{VIN} = 2^{r12+2} \times C_{VIN}$$ Equation 13

Due to the selection of $C_{EXT} > 2^r * C_{VIN}$, the sample time t_S can be selected independently of the analog source R_{ASRC}. Nevertheless, R_{ASRC} has a direct impact to the cycle time t_{CYCLE}.

12.1.7 Discrete RC Filter

If an extended sample time is insufficient to filter noise on the analog signal input, you can use an external low pass filter (RC filter) to the analog input pin (see Figure 39). Cross-check the possible sample period with the cut-off frequency of the RC filter. Furthermore, the voltage drop at R_{EXT} due to the complete leakage current of the analog input must not be higher than the required accuracy of the measured analog signal.

Figure 39. Analog Input with Low Pass Filter



13 Assembly and Package-related PCB Design

The application notes AN202751 and AN79938 provided guidelines on surface mount assembly for different BGA packages, related PCB design, surface mount process flow, and final joint inspection methods.

14 Summary

The application note described how to setup a minimum MCU system. The application note also provided hints on how to handle different uses cases at MCU pins and how to make a proper PCB layout design.

15 Abbreviations

Abbreviation	Description
ADC	A/D Converter
ALT	Alternate
AN	Analog Input
BOD	Brown-out-Detection
BOM	Bill of Material
DeCap	Decoupling capacitor
DDR	Double Data Rate. Data sampled twice within a clock cycle. fDATA = fCLK
DS	Data Sheet
DUT	Device under Test
ECU	Electronic Control Unit
ETM	Embedded Trace Macrocell™
Ext	external
GND	Electrical ground
GPIO	General Purpose I/O
HVD	High-Voltage-Detection
IC	Integrated Circuit
IF	Interface
Int	Internal
IO	Input Output
JTAG	Joint Test Action Group is the common name for the IEEE 1149.1 Standard Test Access Port, Boundary-Scan Architecture, and interface for debug tools for on-chip debug inside the target MCU
LVD	Low-Voltage-Detection
LU	Latch-up
MAC	Media Access Control. Component independent from communication medium.
MCU	Microcontroller
MCU	Microcontroller Unit
PDN	Power Distribution Network
PHY	PHYsical layer. Electrical component for data coding and decoding between pure digital and modulated channel
SDR	Single Data Rate. Data sampled only once within a clock cycle. fDATA = ½ x fCLK
S/s	Samples per second
NC	Not connected
OCD	Over-Current-Detection
OVD	Over-Voltage-Detection
PCB	Printed Circuit Board
POR	Power-On-Reset
Rd	Damping resistor
Rf	Feedback resistor

Abbreviation	Description
STP	Shielded Twisted-Pair
SWD	Serial Wire Debug
TRM	Technical Reference Manual
VCC	Generic naming convention for power supply pin
Voltage drop	Transient voltage drop
VSS	Generic naming convention for ground pin
WDT	Watchdog Timer

16 Related Documents

- AN224153 – Design and Layout Guide for Semper Flash Memory
- AN79938 – Design Guidelines for Cypress Ball Grid Array (BGA) Packaged Devices
- AN202751 – Surface Mount Assembly Recommendations for Cypress FBGA Packages
- AN213250 – Power Filter Options for FPD-Link Interfaces
- AN226698 – External Power Supply Design Guide for Traveo II Family CYT4BF000 Series
- AN220118 – Getting Started with the Traveo II Family
- AN72845 – Design Guidelines for QFN Packaged Devices
- AN89611 – PsoC 3 and PSoC 5LP Getting Started with Chip Scale Packages
- AN80994 – Design Considerations for Electrical Fast Transient (EFT) Immunity
- AN57821 – PsoC 3, PSoC 4, and PSoC 5LP Mixed Signal Circuit Board Layout Considerations
- AN220222 – Low power mode procedure in the Traveo II family
- ARM_Link_01 – CoreSight Components Technical Reference Manual (Cortex debug connector detailed specification in Appendix C)
- ARM_Link_02 – Cortex-M Debug Connectors
- SRAM Board Design Guidelines
- Device datasheet
  - CYT2B7 Datasheet 32-Bit Arm® Cortex®-M4F Microcontroller Traveo™ II Family
  - CYT2B9 Datasheet 32-Bit Arm® Cortex®-M4F Microcontroller Traveo™ II Family
  - CYT4BF Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller Traveo™ II Family
  - CYT4DN Datasheet 32-Bit Arm® Cortex®-M7 Microcontroller Traveo™ II Family
- CYT2B Series
  - Traveo™ II Automotive Body Controller Entry Family Architecture Technical Reference Manual (TRM)
  - Traveo™ II Automotive Body Controller Entry Registers Technical Reference Manual (TRM) for CYT2B7
  - Traveo™ II Automotive Body Controller Entry Registers Technical Reference Manual (TRM) for CYT2B9
- CYT4B Series
  - Traveo™ II Automotive Body Controller High Family Architecture Technical Reference Manual (TRM)
  - Traveo™ II Automotive Body Controller High Registers Technical Reference Manual (TRM)
- CYT4D Series
  - Traveo™ II Automotive Cluster 2D Family Architecture Technical Reference Manual (TRM)
  - Traveo™ II Automotive Cluster 2D Registers Technical Reference Manual (TRM)

Contact Technical Support to obtain Traveo II family series datasheets and Technical Reference Manuals.

About the Author

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Appendix A. Power Supply Concept

The appendix provides the MCU-specific proposals for a power supply concept including decoupling capacitors for the MCU power supply.

Note: The deployment of decoupling caps and the Bypass capacitors depend on the application, this is especially valid for the I/O supplies. For more information, see I/O Domains.

Definitions

- fCLK: Clock signal frequency
- fDATA: Data signal frequency
- SDR: Single Data Rate. Data sampled only once within a clock cycle. f_{DATA} = ½ x f_{CLK}
- DDR: Double Data Rate. Data sampled twice within a clock cycle. f_{DATA} = f_{CLK}
- 'Pin': Synonym for the original pin name
- Domain: Power Domain. One power domain can have one or more power pins (for example, VDDD has several pins)
- Voltage drop: Transient voltage drop

A.1 CYT2B Series

Figure 40. Power Supply Concept Example for CYT2B Series

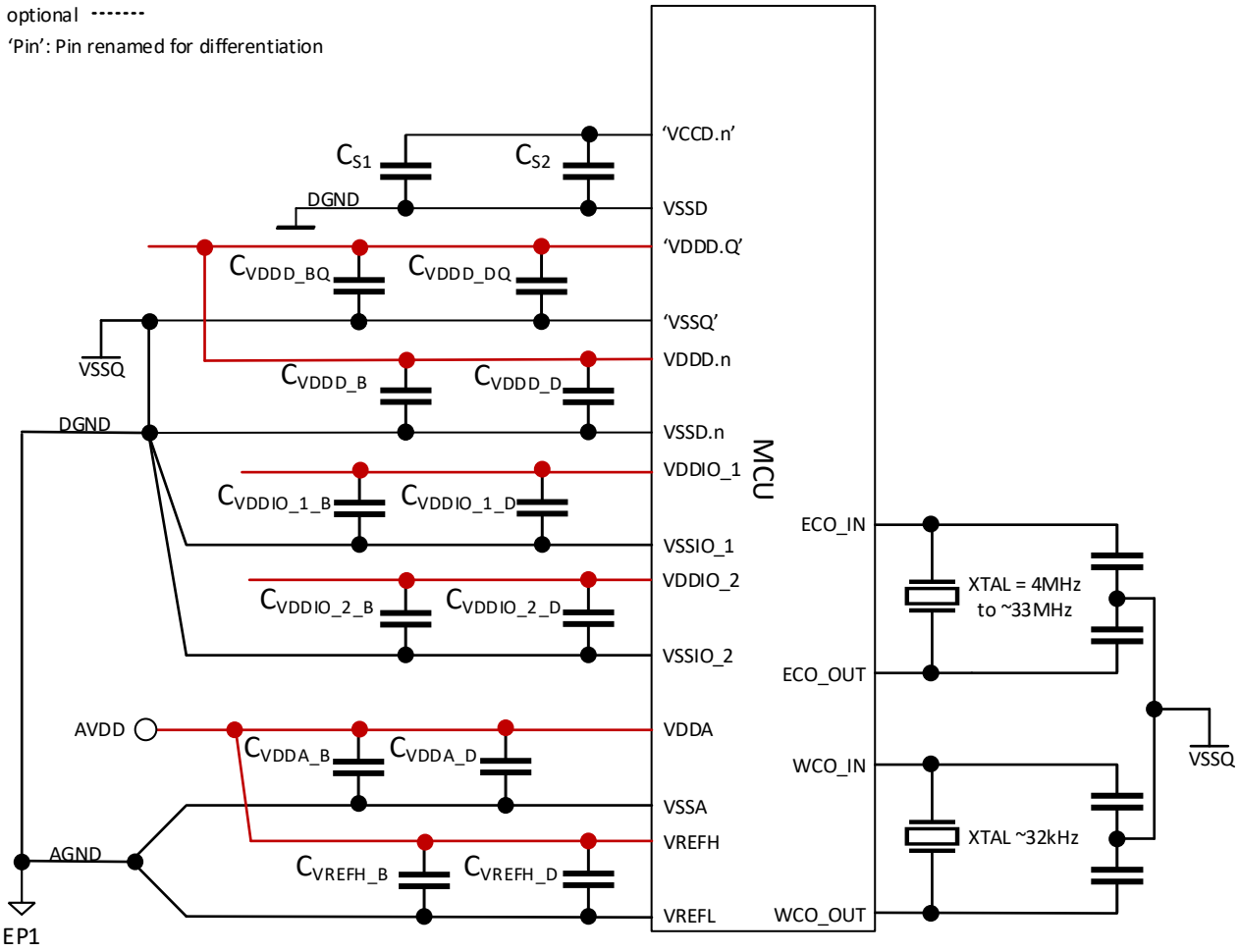


Table 9. External Component Integration Example for CYT2B Series

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass / Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet. Close to Pin Pair according to Device DS specification resp. to 'VCCD.CS1'. 1 capacitor per power domain. ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor and including board track to all VCCD pins with priority on pin 'VCCD.CS1' with I_{DD}[7] ≤ 150mA by Active Regulator
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT:	1 capacitor per power domain pin. Only required if more pins are available

[7] I_{DD}: input current definition of VDDD in CYT2B datasheet

Symbol	Parameter	Package	
		Value	Remark
		47 nF X7R	
C_{VDDD_BQ}	Bypass capacitor for VDDD domain IPs	4.7 uF X7R	Also, used for low frequency decoupling and MCU inrush current. For PCB specific Capacitor Dimensioning, consider the inrush current from Active Regulator in spec ID SID603 mentioned in datasheet Figure 48. ESR ≤ 100 mΩ, ESL ≤ 4 nH including board track
C_{VDDD_DQ}	Decoupling capacitor for VDDD domain IPs	100 nF X7R	Voltage drop greater than 300 mV must be avoided to keep stability of internal LDO. Pin 'VDDD.Q' (Quiet Supply) not shared with I/O Domain, but for oscillator among others.
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	-	Only required if C_{VDDD_BQ} is not sufficient for bypassing power rail supply.
C_{VDDD_D}[8,9]	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin Decoupling conditions is valid per pin and all toggling groups should toggle asynchronously to each other.
$C_{VDDIO\_1\_B}$	Bypass capacitor for IO domain VDDIO_1	TBD	Optional. Depending on the power supply inductance
$C_{VDDIO\_1\_D}$[10,11]	Decoupling capacitor for IO domain VDDIO_1	100 nF X7R	1 capacitor per power domain pin Decoupling condition is valid for the whole domain.
$C_{VDDIO\_2\_B}$	Bypass capacitor for IO domain VDDIO_2	-	
$C_{VDDIO\_2\_D}$[12]	Decoupling capacitor for IO domain VDDIO_2	100 nF X7R	1 capacitor per power domain pin Decoupling condition is valid for the whole domain. Note: Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA
C_{VDDA_B}[13]	Bypass capacitor for ADC VDDA	2.2 µF X7R	-
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Only required, if separate analog reference supply is used.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	

[8] VDDD: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[9] VDDD: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[10] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 5x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[11] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 5x parallel transition: 100 ns, C_L/pin: 47 pF, asynchronous to footnote 10, no consideration of device internal impedance

[12] VDDIO_2: 5 V, 4% voltage drop, f_{CLK}: 2 MHz, SDR, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[13] Connection of C_{VDDA_B} to both ADC DeCaps for low noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed following values according to Figure 45: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1nH

Table 10. Special Power Domain Pins for CYT2B Series

Name	Package Pin Number (Original Pin Name)					Comment
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP	
'VDDD.Q'	55 (VDDD)	69 (VDDD)	86 (VDDD)	124 (VDDD)	153 (VDDD)	Quiet Supply. Not shared with I/O Domain.
'VSSQ'	56 (VSSD)	70 (VSSD)	87 (VSSD)	125 (VSSD)	154 (VSSD)	Quiet Ground for Oscillator.
'VCCD.CS1'	58 (VCCD)	72 (VCCD)	89 (VCCD)	127 (VCCD)	156 (VCCD)	

A.2 CYT4B Series with TEQFP Package

Figure 41. Power Supply Concept Example for CYT4B Series with TEQFP Package

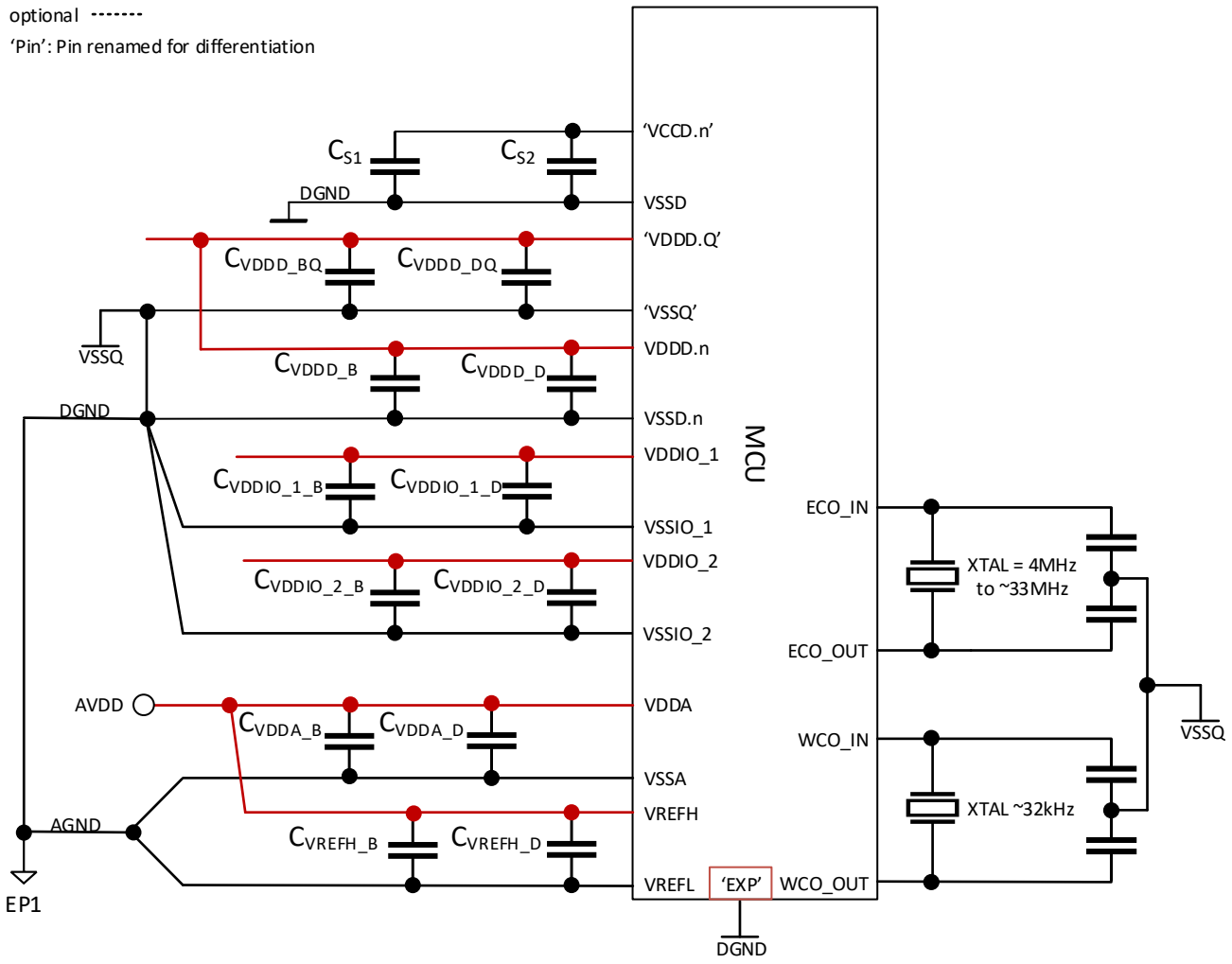


Table 11. External Component Integration Example for CYT4B Series with TEQFP Package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet. Close to Pin Pair according to Device DS specification respective to 'VCCD.CS1'. 2 capacitors per power domain. ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including board track to all VCCD pins with priority on pin 'VCCD.CS1' with I_{DD_VDDD}[14] ≤ 150mA by Active Regulator.

[14] I_{DD_VDDD}: input current definition of VDDD in internal supply mode in CYT4B datasheet

Symbol	Parameter	Package	
		Value	Remark
			Values do not cover higher load transition cases like Wakeup from DeepSleep with permanent supply from external. PMIC.
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per power domain pin group. For VCCD pin group definition, see Table 12.
C_{VDDD_BQ}	Bypass capacitor for VDDD domain IPs	4.7 µF X7R	Also, used for low frequency decoupling and MCU inrush current. For PCB specific Capacitor Dimensioning consider the inrush current from Active Regulator in spec ID SID603 mentioned in datasheet Figure 48. 2 capacitors per power domain. ESR ≤ 100 mΩ, ESL ≤ 4 nH in total per capacitor including board track.
C_{VDDD_DQ}	Decoupling capacitor for VDDD domain IPs	100 nF X7R	Voltage drop greater than 300 mV must be avoided to keep stability of internal LDO. Pin 'VDDD.Q' (Quiet Supply) is not shared with I/O Domain, but with oscillator among others.
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	-	Only required if C_{VDDD_BQ} is not sufficient for bypassing power rail supply.
C_{VDDD_D}[15,16]	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin Decoupling conditions is valid per pin and all toggling groups should toggle asynchronously with each other.
$C_{VDDIO\_1\_B}$	Bypass capacitor for IO domain VDDIO_1	TBD	Optional. Depending on the power supply inductance
$C_{VDDIO\_1\_D}$[17,18]	Decoupling capacitor for IO domain VDDIO_1	100 nF X7R	1 capacitor per power domain pin Decoupling condition is valid for the whole domain.
$C_{VDDIO\_2\_B}$	Bypass capacitor for IO domain VDDIO_2	-	
$C_{VDDIO\_2\_D}$[19]	Decoupling capacitor for IO domainVDDIO_2	100 nF X7R	1 capacitor per power domain pin Decoupling condition is valid for the whole domain. **Note**: Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA
C_{VDDA_B}[20]	Bypass capacitor for ADC VDDA	2.2 µF X7R	-
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Only required if separate analog reference supply is used.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	

[15] VDDD: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[16] VDDD: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 4x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[17] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 2 MHz, 5x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[18] VDDIO_1: 5V, 4% voltage drop, f_{DATA}: 0.1 MHz, 5x parallel transition: 100 ns, C_L/pin: 47 pF, asynchronous to footnote 17, no consideration of device internal impedance

[19] VDDIO_2: 5 V, 4% voltage drop, f_{CLK}: 2 MHz, SDR, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

[20] Connection of C_{VDDA_B} to both ADC DeCaps for low noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed following values according to Figure 45: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1nH

Table 12. Special Power Domain Pins for CYT4B Series with TEQFP Package

Name	Package Pin Number (Original Pin Name)					Comment
	64-TEQFP	80-TEQFP	100-TEQFP	144-TEQFP	176-TEQFP	
'VDDD.Q'	Package(s) not available		86 (VDDD)	124 (VDDD)	153 (VDDD)	Quiet Supply. Not shared with I/O Domain.
'VSSQ'			87 (VSSD)	125 (VSSD)	154 (VSSD)	Quiet Ground for Oscillator.
'VCCD.CS2.A'			27 (VCCD) 28 (VCCD)	38 (VCCD) 39 (VCCD)	46 (VCCD) 47 (VCCD)	One decap C_{S2} on pin group
'VCCD.CS2.B'			64 (VCCD) 65 (VCCD)	92 (VCCD) 93 (VCCD)	111 (VCCD) 112 (VCCD) 113 (VCCD)	One decap C_{S2} on pin group
'VCCD.CS2.C'			89 (VCCD)	127 (VCCD)	156 (VCCD)	One decap C_{S2} on pin group
'EXP'	N/A	N/A	yes	yes	yes	Exposed Pad

A.3 CYT4B Series with BGA Package

Figure 42. MCU Power Supply Concept Example for CYT4B Series with BGA Package

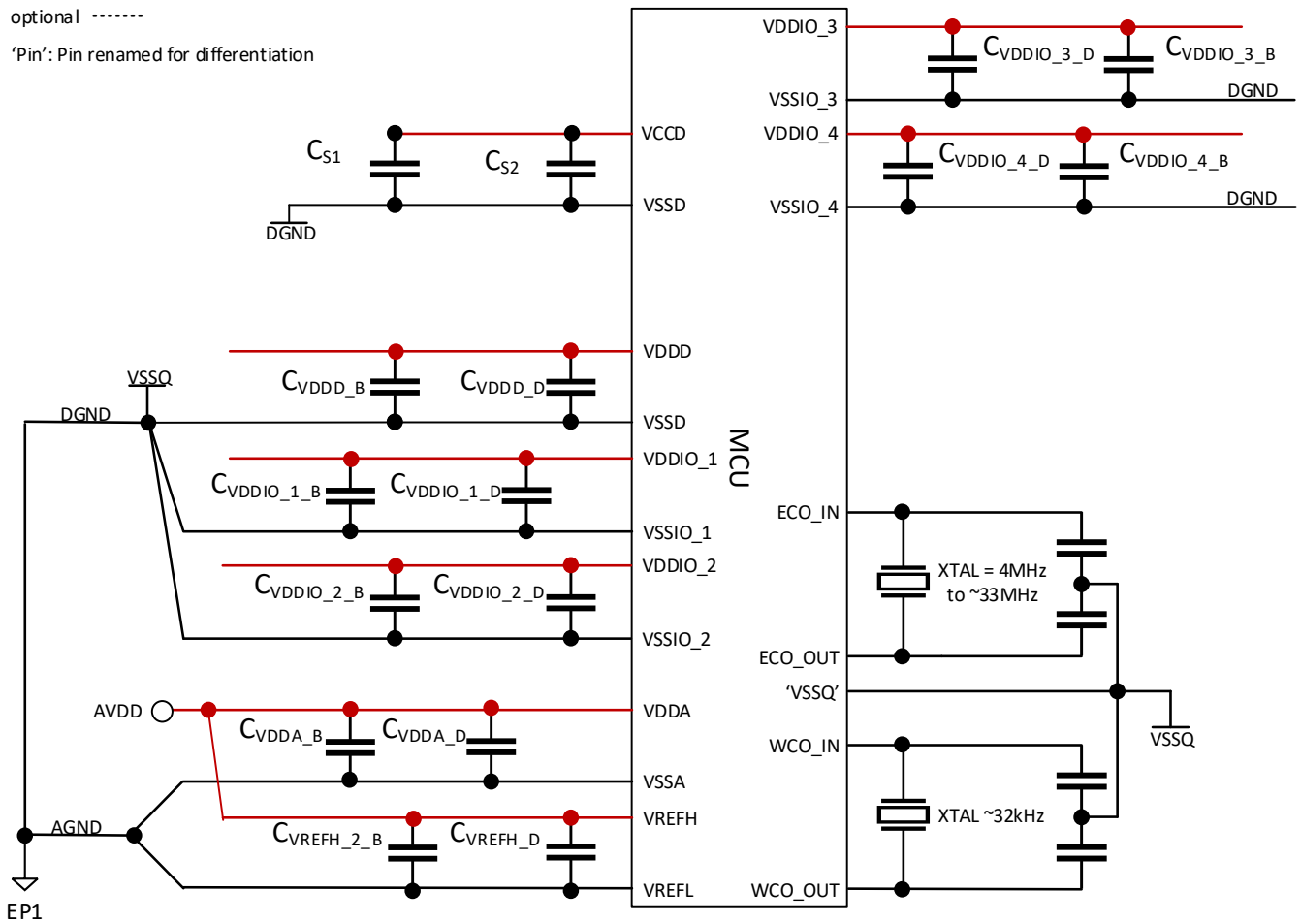


Table 13. External Component Integration Example for CYT4B Series BGA Package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet. Nominal value for power domain. Close to Pin Pair according to device datasheet specification. Check capacitor value and placement requirements between MCU and PMIC depending on core VCCD power rail concept.
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R ALT: 47 nF X7R	1 capacitor per power domain pin.
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	10 µF X7R	Required for internal LDO. For PCB specific Capacitor Dimensioning, consider the inrush current from Active Regulator in spec ID SID603 mentioned in datasheet Figure 48.
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO. Number of parallel transitions should be reduced as much as possible.
$C_{VDDIO\_1\_B}$[21]	Bypass capacitor for IO domain VDDIO_1	1 µF X7R	1 capacitor per power domain
$C_{VDDIO\_1\_D}$[19]	Decoupling capacitor for IO domain VDDIO_1	100 nF X7R	1 capacitor per power domain pin. Minimum two pieces are required.
$C_{VDDIO\_2\_B}$	Bypass capacitor for IO domain VDDIO_2	-	
$C_{VDDIO\_2\_D}$[22]	Decoupling capacitor for IO domain VDDIO_2	100 nF X7R	1 capacitor per power domain pin **Note**: Voltage drop at VDDIO_2 must fulfill the requirement VDDA – 0.3 V ≤ VDDIO_2 ≤ VDDA
$C_{VDDIO\_3\_B}$	Bypass capacitor for IO domain VDDIO_3	1 µF X7R	1 capacitor per power domain Equivalent power rail inductance: 20 nH
$C_{VDDIO\_3\_D}$[23]	Decoupling capacitor for IO domain VDDIO_3	100 nF X7R 10 nF X7R	1 capacitor for power domain 1 capacitor for power domain
$C_{VDDIO\_4\_B}$	Bypass capacitor for IO domain VDDIO_4	1 µF X7R	1 capacitor per power domain Equivalent power rail inductance: 20 nH
$C_{VDDIO\_4\_D}$[24]	Decoupling capacitor for IO domain VDDIO_4	100 nF X7R 10 nF X7R	1 capacitor for power domain 1 capacitor for power domain
C_{VDDA_B}[25]	Bypass capacitor for ADC VDDA	2.2 µF X7R	-

[21] VDDIO_1: 3.3 V, 5% voltage drop at capacitors(s), f_{CLK}: 25 MHz, DDR, 9 x parallel transition: 3 ns, C_L/pin: 20 pF, no consideration of device internal impedance

[22] VDDIO_2: 5 V, 4% voltage drop at capacitor(s), f_{DATA}: 2 MHz, 10 x parallel transition: 20 ns, C_L/pin: 47 pF, no consideration of device internal impedance

Conditions:

[23] VDDIO_3: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 100 MHz, DDR, 9 x parallel transition: 1.5 ns, C_L/pin: 15 pF, no consideration of device internal impedance

[24] VDDIO_4: 3.3 V, 7% voltage drop at capacitors, f_{CLK}: 125 MHz, SDR, 9 x parallel transition: 0.75 ns, C_L/pin: 10 pF, no consideration of device internal impedance

[25] Connection of C_{VDDA_B} to both ADC DeCaps for low noise environment. Three ADC units run simultaneously, not asynchronously and no use of the precondition feature. Power rails and ground parasitic for the analog supply should not exceed following values according to Figure 45: R_{AVDD} ≤ 100 mΩ, L_{AVDD} ≤ 15 nH, R_{AGND} ≤ 100 mΩ, L_{AGND} ≤ 15 nH, L1 ≤ 1 nH, L2 ≤ 1nH

Symbol	Parameter	Package	
		Value	Remark
C_{VDDA_D}	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
$C_{VREFH\_2\_B}$	Bypass capacitor for ADC VREFH	2.2 µF X7R	Optional. Only required, if separate analog reference supply is used.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	

Table 14. Special Power Domain Pins for CYT4B Series with BGA Package

Name	Package Pin Number (Original Pin Name)		Comment
	272-BGA	320-BGA	
'VSSQ'	L11 (VSSD_1)	N13 (VSSD_1)	Quiet Ground for Oscillator.

A.4 CYT4D Series with BGA Package

Note: This power concept is valid for all CYT4D, except CYT4DND Rev. A0 and CYT4DNJ Rev. A0.

Figure 43. MCU Power Supply Concept Example for CYT4D Series with BGA Package

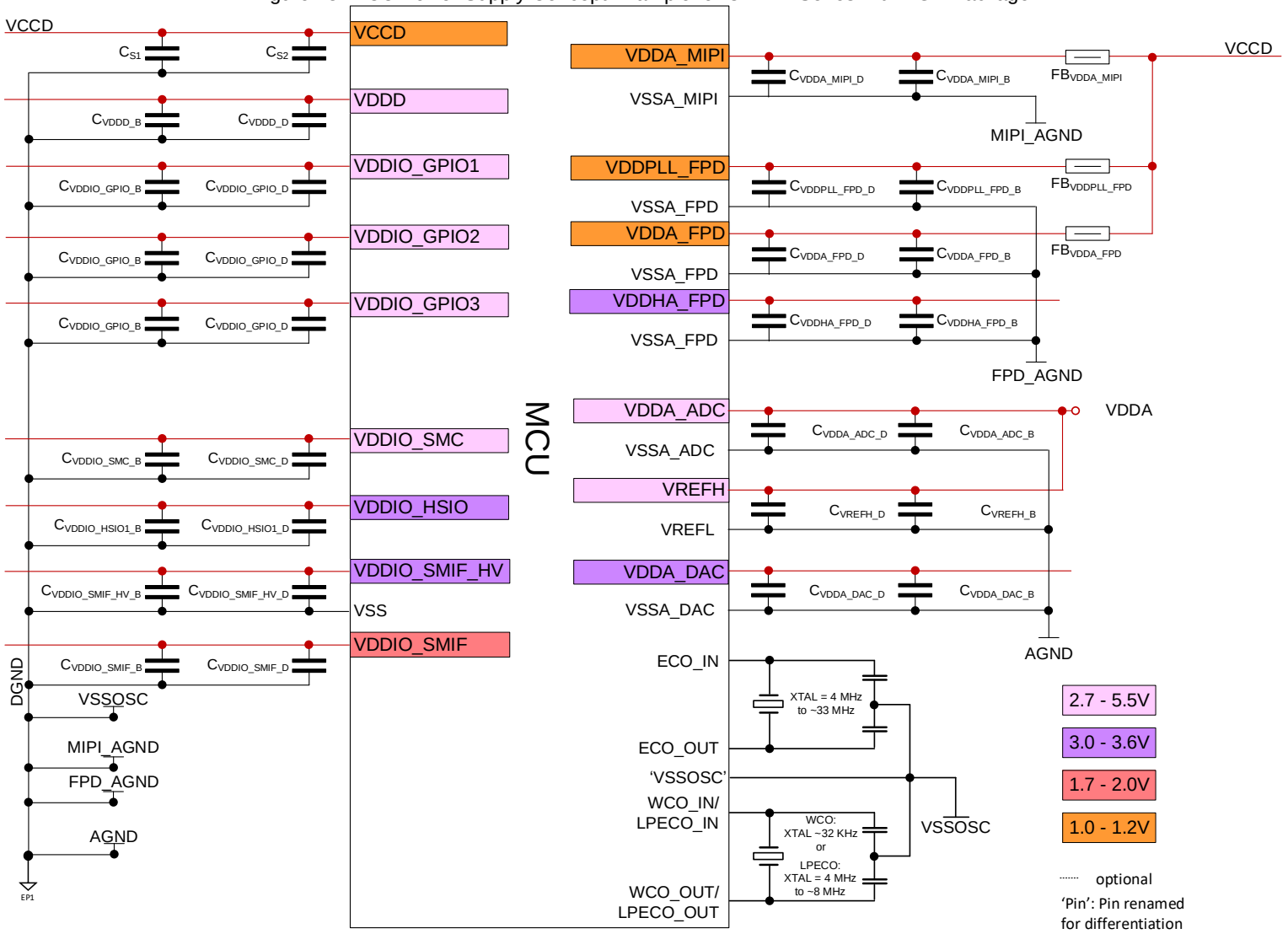


Table 15. External Component Integration Example for CYT4D Series with BGA Package

Symbol	Parameter	Package	
		Value	Remark
C_{S1}	Bypass/Smoothing capacitor for core power supply domain VCCD	X7R Type	Value in the datasheet. 2 capacitors for power domain. Close to Pin Pair according to device datasheet specification. Check capacitor value and placement requirements between MCU and PMIC depending on core VCCD power rail concept.
C_{S2}	Decoupling capacitor for core power supply domain VCCD	100 nF X7R	1 capacitor per power domain pin
C_{VDDD_B}	Bypass capacitor for VDDD domain IPs and I/O	44 µF X7R	Required for internal LDO For PCB specific Capacitor Dimensioning, consider the inrush current from Active Regulator in spec ID SID603 mentioned in datasheet Figure 48.
C_{VDDD_D}	Decoupling capacitor VDDD domain logic and I/O	100 nF X7R	1 capacitor per power domain pin Voltage drop greater than 300 mV must be avoided due to internal LDO. Number of parallel transitions should be reduced as much as possible.
$C_{VDDIO\_GPIO1\_B}$	Bypass capacitor for IO domain GPIO	1 µF X7R	1 capacitor for power domain
$C_{VDDIO\_GPIO1\_D}$	Decoupling capacitor for IO domain GPIO	100 nF X7R	1 capacitor per power domain pin
$C_{VDDIO\_GPIO2\_B}$	Bypass capacitor for IO domain GPIO	1 µF X7R	1 capacitor for power domain
$C_{VDDIO\_GPIO2\_D}$	Decoupling capacitor for IO domain GPIO	100 nF X7R	1 capacitor per power domain pin
$C_{VDDIO\_GPIO3\_B}$	Bypass capacitor for IO domain GPIO	1 µF X7R	1 capacitor for power domain
$C_{VDDIO\_GPIO3\_D}$	Decoupling capacitor for IO domain GPIO	100 nF X7R	1 capacitor per power domain pin
$C_{VDDIO\_SMC\_B}$	Bypass capacitor for IO domain SMC	2.2 µF X7R	1 capacitor per power domain
$C_{VDDIO\_SMC\_D}$	Decoupling capacitor for IO domain SMC	100 nF X7R	1 capacitor per 2 power domain pins
$C_{VDDIO\_HSIO1\_B}$	Bypass capacitor for IO domain HSIO1	2.2 µF X7R	1 capacitor per power domain
$C_{VFDIO\_HSIO1\_D}$	Decoupling capacitor for IO domain HSIO1	100 nF X7R	1 capacitor per 2 power domain pins
$C_{VDDIO\_SMIF\_B}$	Bypass capacitor for IO domain SMIF	2.2 µF X7R	1 capacitor per power domain
$C_{VDDIO\_SMIF\_D}$	Decoupling capacitor for IO domain SMIF	100 nF X7R	1 capacitor per 2 power domain pins
$C_{VDDIO\_SMIF\_HV\_B}$	Bypass capacitor for IO domain SMIF_HV	2.2 µF X7R	1 capacitor per power domain
$C_{VDDIO\_SMIF\_HV\_D}$	Decoupling capacitor for IO domain SMIF_HV	100 nF X7R	1 capacitor per 2 power domain pins
$C_{VDDA\_ADC\_B}$	Bypass capacitor for ADC VDDA	4.7 µF X7R	1 capacitor per power domain
$C_{VDDA\_ADC\_D}$	Decoupling capacitor for ADC VDDA	100 nF X7R	1 capacitor per power domain pin
$C_{VDDA\_DAC\_B}$	Bypass capacitor for DAC VDDA	2.2 µF X7R	1 capacitor per power domain
$C_{VDDA\_DAC\_D}$	Decoupling capacitor for DAC VDDA	100 nF X7R	
C_{VREFH_B}	Bypass capacitor for ADC VREFH	2.2 µF X7R	1 capacitor per power domain. Optional. Only required, if separate analog reference supply is used.
C_{VREFH_D}	Decoupling capacitor for ADC VREFH	100 nF X7R	1 capacitor per 2 power domain pins
$C_{VDDPLL\_FPD\_B}$	Bypass capacitor for FPD VDDPLL	4.7 µF X7R	1 capacitor per power domain
$C_{VDDPLL\_FPD\_D}$	Decoupling capacitor for FPD VDDPLL	100 nF X7R	1 capacitor per 2 power domain pins

Symbol	Parameter	Package	
		Value	Remark
$F_{BVDDPLL\_FPD}$	Ferrite bead for FPD VDDPLL	Tbd	1 ferrite bead per power domain. Silent supply must be ensured.
$C_{VDDA\_FPD\_B}$	Bypass capacitor for FPD VDDA	4.7 µF X7R	1 capacitor per power domain
$C_{VDDA\_FPD\_D}$	Decoupling capacitor for FPD VDDA	100 nF X7R	4 capacitors per power domain
F_{VDDA_FPD}	Ferrite bead for FPD VDDA	Tbd	1 ferrite bead per power domain. Silent supply must be ensured.
$C_{VDDA\_MIPI\_B}$	Bypass capacitor for MIPI VDDA	4.7 µF X7R	1 capacitor for power domain
$C_{VDDA\_MIPI\_D}$	Decoupling capacitor for MIPI VDDA	100 nF X7R	4 capacitors per power domain
F_{VDDA_MIPI}	Ferrite bead for MIPI VDDA	Tbd	1 ferrite bead per power domain. Silent supply must be ensured.
$C_{VDDHA\_FPD\_B}$	Bypass capacitor for FPD VDDHA	2.2 µF X7R	1 capacitor per power domain
$C_{VDDHA\_FPD\_D}$	Decoupling capacitor for FPD VDDHA	100 nF X7R	1 capacitor per 2 power domain pins

Table 16. Special Power Domain Pins for CYT4B Series with BGA Packages

Name	Package Pin Number (Original Pin Name)		Comment
	327-BGA rev. A0	500-BGA rev. A0	
VSSOSC	E20, F19, G20	H25, H26, K25, K26 (VSS)	Quiet ground for oscillator shielding

Appendix B. Analog Supply

Figure 44 and Figure 45 show the difference between an ideal analog supply without any parasitic elements and a real analog supply with the parasitic elements in the power rail and in the filter capacitors.

Figure 44. Ideal Analog Power Supply

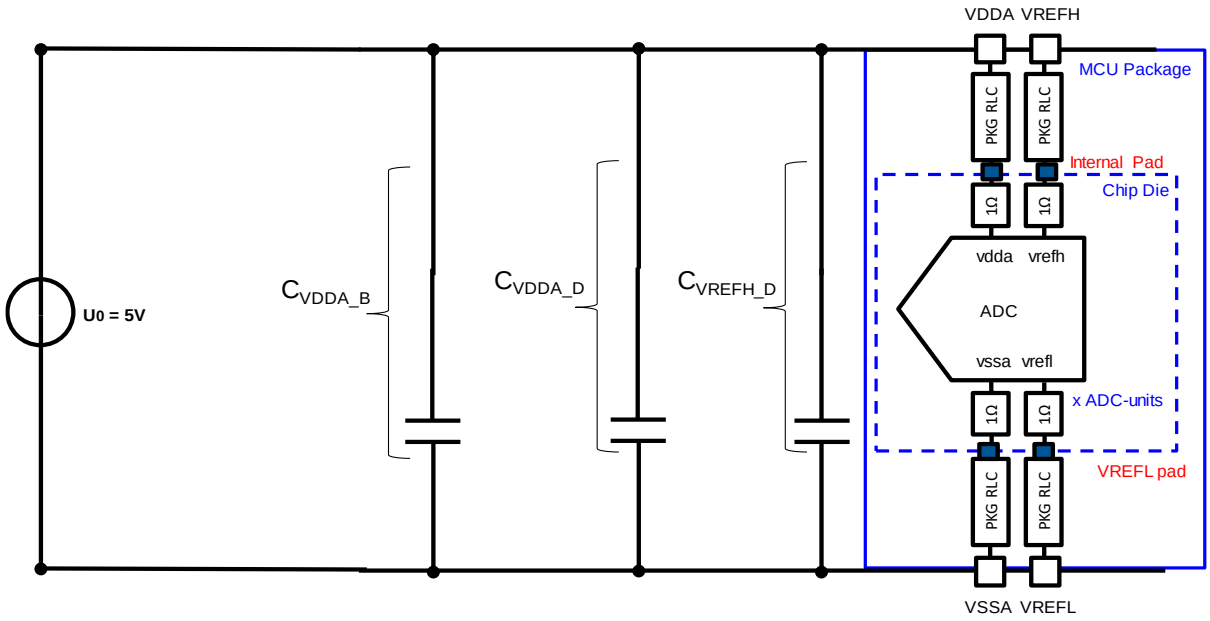
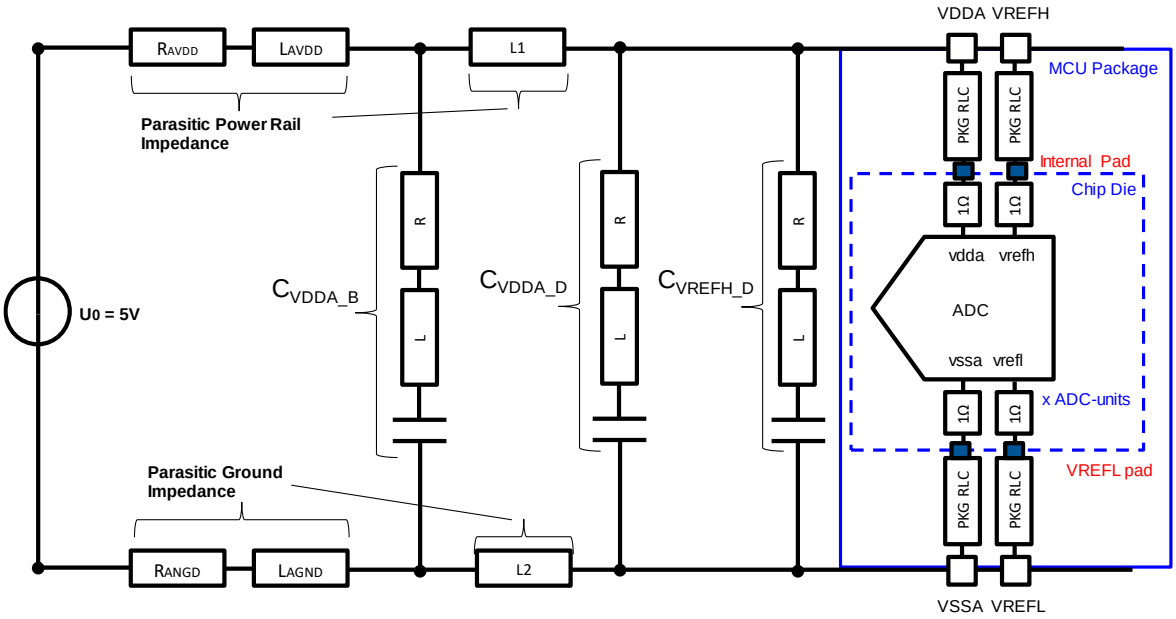


Figure 45. Real Analog Power Supply



Appendix C. Oscillator Layout

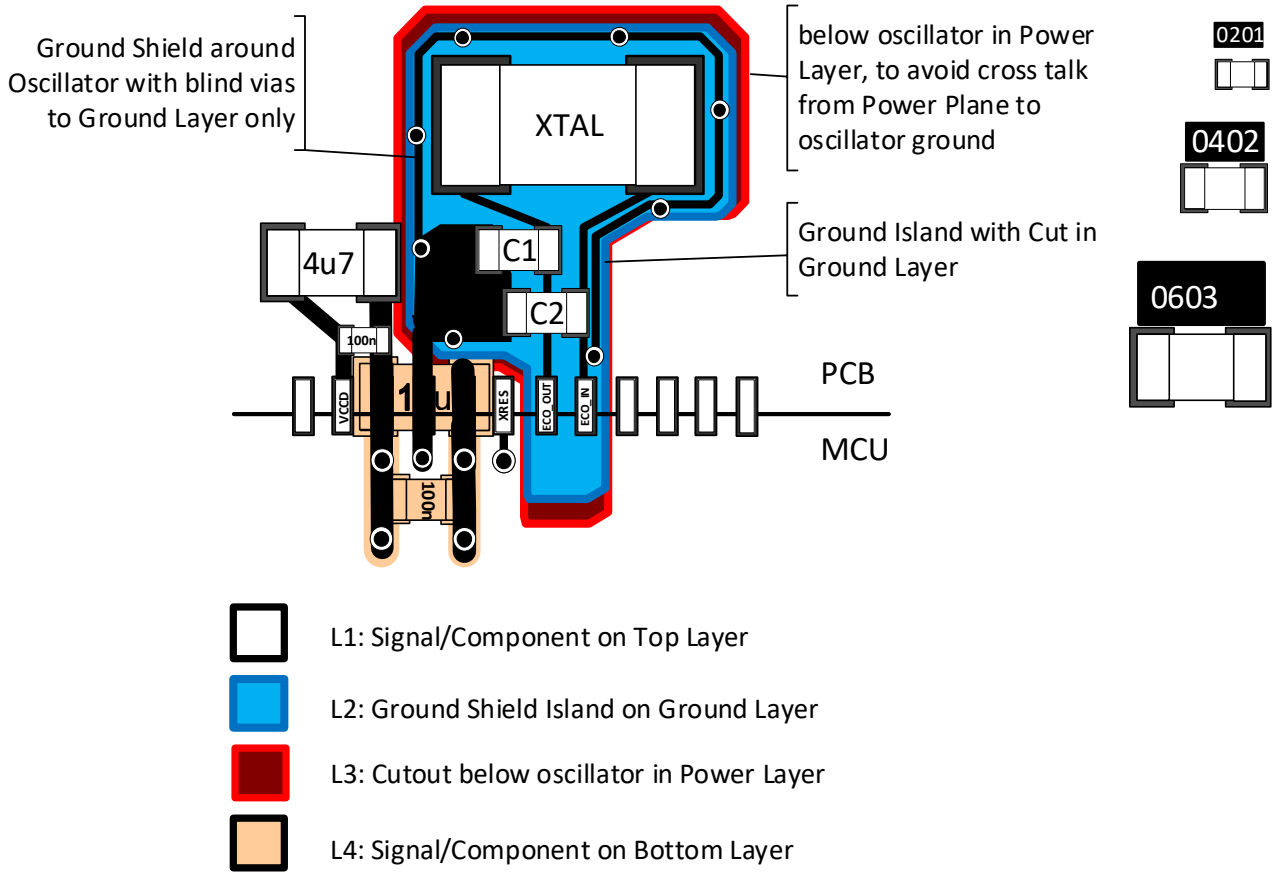
Generic Oscillator layout proposals are given for several packages.

Note: Layout design neither gives any warranty for correct component ratio nor does not follow any PCB design rules. Changes between different packages might be required.

C.1 QFP Packages

A generic proposal for an oscillator layout with the QFP packages is shown in Figure 46.

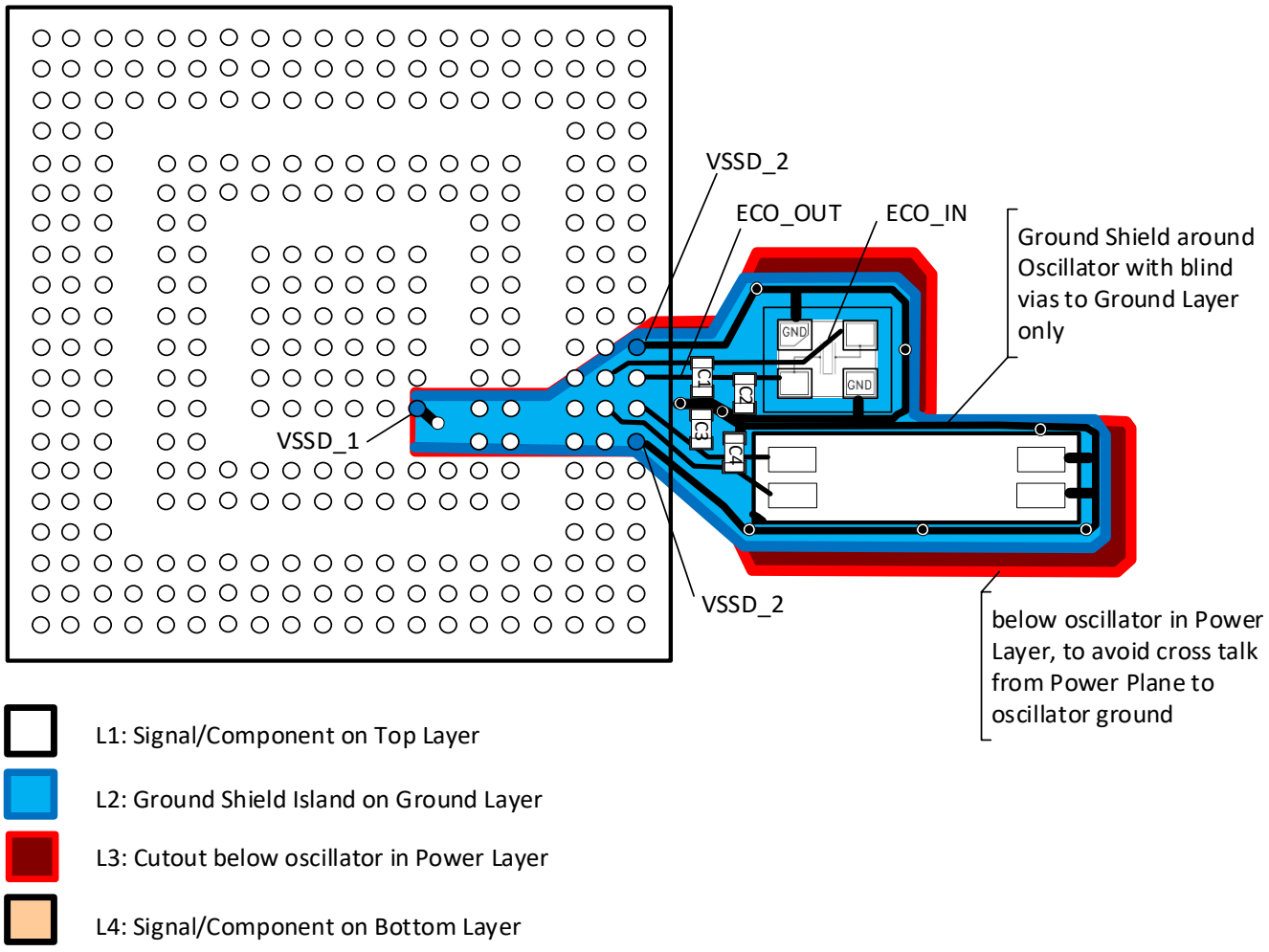
Figure 46. Oscillator Layout Proposal for CYT2B and CYT4B Series QFP Packages



C.2 BGA Packages

A principle proposal for an oscillator layout with the BGA packages is shown in Figure 47.

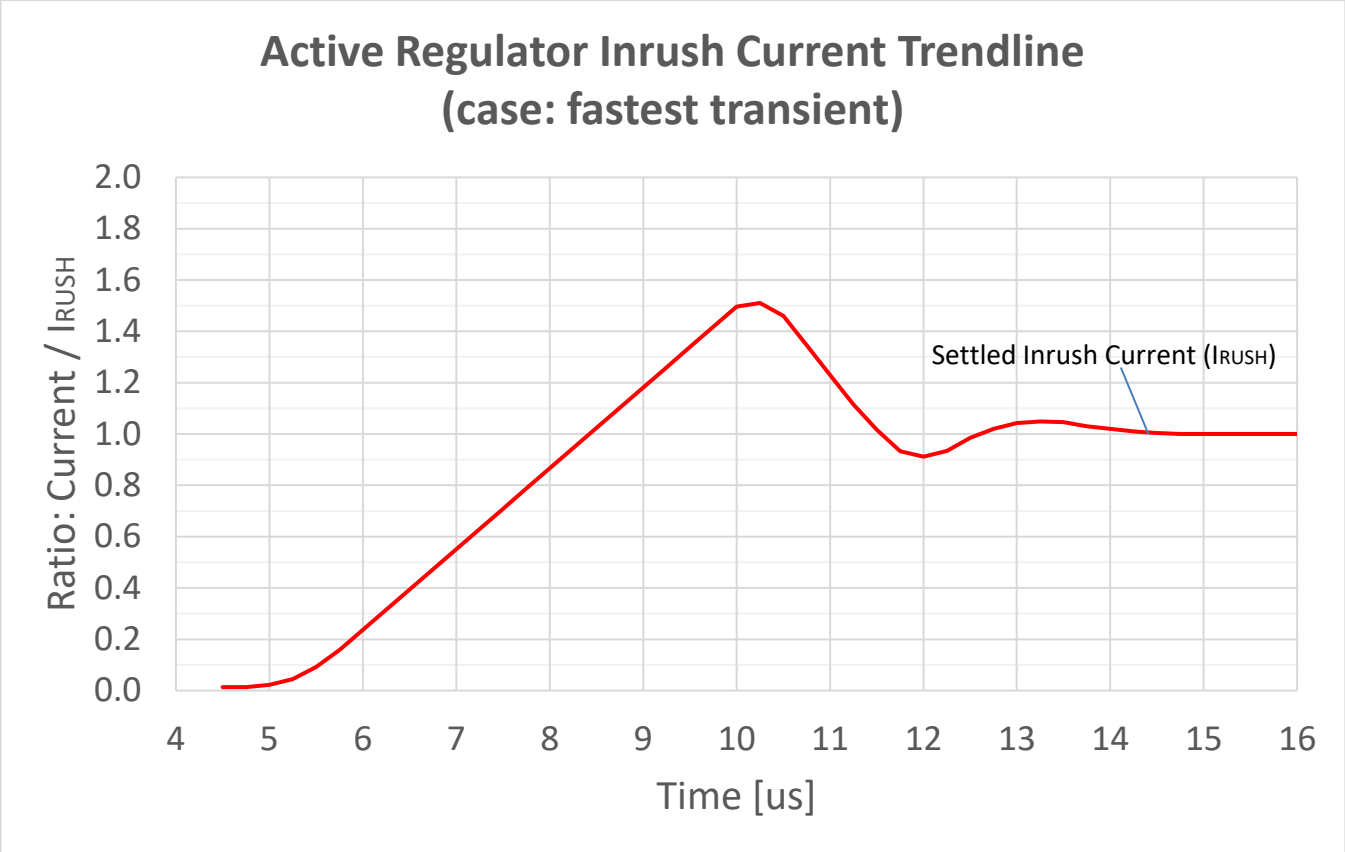
Figure 47. Oscillator Layout Proposal for BGA Packages (Based on CYT4B Series 320-BGA Package)



Appendix D. Active Regulator Inrush Current

As one part of dimensioning of the bypass capacitors at the VDDD domain, the external voltage regulator, the PCB parasitics (ESR and ESL) of that power rail, and the maximum current consumption of the Active Regulator (internal LDO) need to be considered. The fastest inrush current transient into the Active Regulator is shown in Figure 48. Here it is relative to the settled inrush current, specified as parameter I_{RUSH} in the datasheet.

Figure 48. Active Regulator Inrush Current in Worst Case Scenario



Appendix E. Unused Power Domain Handling

This section explains how to handle unused power domains and their I/O port pins. It does not consider the transition requirements for different power modes, that is, the power ON/OFF sequencing. With regard to I/O port pin handling, make sure that the ECU peripherals are in proper states during power mode transitions. These items are in the responsibility of the user.

E.1 CYT2B Series

Power Domain	Voltage Operation Range	Permanent Unused Domain (Active Mode)			DeepSleep Mode			Hibernate Mode		
		Can be switched OFF? [Yes, No]	I/O Pin Handling[26]	Remark	Can be switched OFF? [Yes, No]	I/O Pin Handling[26]	Remark	Can be switched OFF? [Yes, No]	I/O Pin Handling[26]	Remark
VDDD (always-ON)	2.7 - 5.5 V	No	-	-	No	-	-	No	-	-
VCCD	1.09 - 1.21 V	No	-	-	No	-	-	-	-	-
VDDA_ADC	2.7 - 5.5 V	No	-	-	Yes	-	Disable BOD Reset before DeepSleep	Yes	-	-
VDDA_VREFH	2.7 - 5.5 V	Yes	-	-	Yes	-	-	Yes	-	-
VDDIO_1	2.7 - 5.5 V	No	Tie to GND, Open pin	-	No	-	-	No	Disable	-
VDDIO_2	2.7 - 5.5 V	No	-	-	Yes	Disable	-	Yes	Disable	-

[26] Explanation on I/O Pin Handling (For details on unused I/O port pins, see Port Input/Unused Pins)

- Tie to GND: direct connection to GND. Floating levels must be avoided due to Latch-up (LU) risk
- Open pin: pin stays open, no wiring. Exception in power save modes.
- Disable: Disable input-buffer and disable output

E.2 CYT4B Series

Power Domain	Voltage Operation Range	Permanent Unused Domain (Active Mode)			DeepSleep Mode			Hibernate		
		Can be switched OFF? [Yes, No]	I/O Pin Handling[27]	Remark	Can be switched OFF? [Yes, No]	I/O Pin Handling[27]	Remark	Can be switched OFF? [Yes, No]	I/O Pin Handling[27]	Remark
VDDD (always-ON)	2.7 - 5.5 V	No	-	-	No	-	-	No	-	-
VCCD	1.09 - 1.21 V	No	-	-	No	-	-	-	-	-
VDDA_ADC	2.7 - 5.5 V	No	-	-	Yes	-	Disable BOD Reset before DeepSleep	Yes	-	-
VDDA_VREFH	2.7 - 5.5 V	Yes	-	-	Yes	-	-	Yes	-	-
VDDIO_1	2.7 - 5.5 V	Yes	Tie to GND, Open pin	-	Yes	Disable	-	Yes	Disable	-
VDDIO_2	2.7 - 5.5 V	No	-	-	Yes	Disable	-	Yes	Disable	-
VDDIO_3	2.7 - 5.5 V	Yes	Tie to GND, Open pin	-	Yes	Disable	-	Yes	Disable	-
VDDIO_4	2.7 - 5.5 V	Yes	Tie to GND, Open pin	N/A in all packages	Yes	Disable	-	Yes	Disable	-

[27] Explanation on I/O Pin Handling (For details on unused I/O port pins, see Port Input/Unused Pins)

- Tie to GND: direct connection to GND. Floating levels must be avoided due to Latch-up (LU) risk
- Open pin: pin stays open, no wiring. Exception in power save modes.
- Disable: Disable input-buffer and disable output

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Revision	ECN	Submission Date	Description of Change
**	5978183	11/27/2017	New application note.
*A	6653146	08/19/2019	■ Remove section Minimum System ■ Removed Figure 1 ■ Replaced Figure 24, Figure 25, and Figure 43 ■ Updated section 5.2 Power Supply Monitoring ■ Changed Appendix A from Minimum Device System to Power Supply Concept ■ Added Appendix B and Appendix C ■ Moved Oscillator Design Proposal to Appendix C ■ Add CYT4D series Parts Number ▫ Updated Table 1, Table 2, and Table 3 ▫ Updated Figure 28 to Figure 30 ▫ Added Figure 31 to Figure 43 ▫ Added Table 15 ■ Deleted CYT3B series Parts Number ■ Deleted 6.1 Analog Input Pins
*B	6755980	12/18/2019	■ Updated External Core Supply Control, 5 V Tolerant Input Pins, Related Documents ■ Updated Appendix A.2, A.1 ■ Corrected Table 13 ■ Updated Figure 29 ■ Added section 6.9 Clamping Structure of I/O Pins with Shared Analog Function ■ Added section 12 ADC
*C	6888932	05/28/2020	■ Updated Appendix: all “*External Component Integration*” tables, A.1 ■ New linked documents in Related Documents ■ Added section: Assembly and Package-related PCB Design, Active Regulator Inrush Current, Unused Power Domains ■ Updated section: Power ON/Power OFF Sequence of Power Supply Domains
*D	7048089	12/18/2020	■ Added section: Unused Power Domains, Unused Power Domain Handling, FPD-Link ■ Updated section: Power ON/Power OFF Sequence of Power Supply Domains, Debug Interface, Port Input/Unused Pins, Clamping Structure of I/O Pins with Shared Analog Function ■ Updated: Figure 20, Figure 21, Figure 43

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