Application Note

ANPS0031 -ICE1HS01G

Half Bridge LLC Resonant Converter Design using ICE1HS01G

Power Management & Supply

Never stop thinking.

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1 Introduction

This application note describes how to design half bridge LLC resonant converter using ICE1HS01G, which is an 8-pin LLC controller developed by Infineon Technologies. ICE1HS01G is specially designed for applications of switch mode power supplies used in LCD / PDP TV, AC/DC adapter and Audio system.

In this application note, an overview of half bridge LLC resonant converter will be given at first, followed by the introduction of ICE1HS01G functions and operations. A typical application example, 200W HB LLC resonant converter demoboard using ICE1HS01G, will be given in the last past of this document.

2 Overview of Half Bridge LLC Resonant Converter

The increasing requirements of lighter, smaller and more efficient electronic products demand the power supply designers to develop DC/DC converter with high power density and efficiency.

The conventional PWM power converters are widely used in low and medium power applications. However, due to the known limitations exhibited by PWM converters, such as drop in efficiency and deterioration of EMI problem at high-switching frequency and high-input voltage, the efficiency and power density can not be further improved easily. For this reason, the resonant converter is a good alternative because of its soft-switching characteristic. The resonant DC/DC converter can considerably reduce the switching loss and obtain low EMI emission, which has facilitated its adoption in a diverse range of applications [1,2].

A lot of advantages of the LLC resonant converter, such as zero-voltage switching (ZVS) capability of MOSFETs, load insensitive characteristic at normal operation point, output voltage regulation even at zero load condition and low EMI emission, have been investigated and verified in many literatures [3-5]. These features can fully meet the power supply's demands in many modern applications such as LCD/PDP TV, AC/DC adapter, audio system, etc.

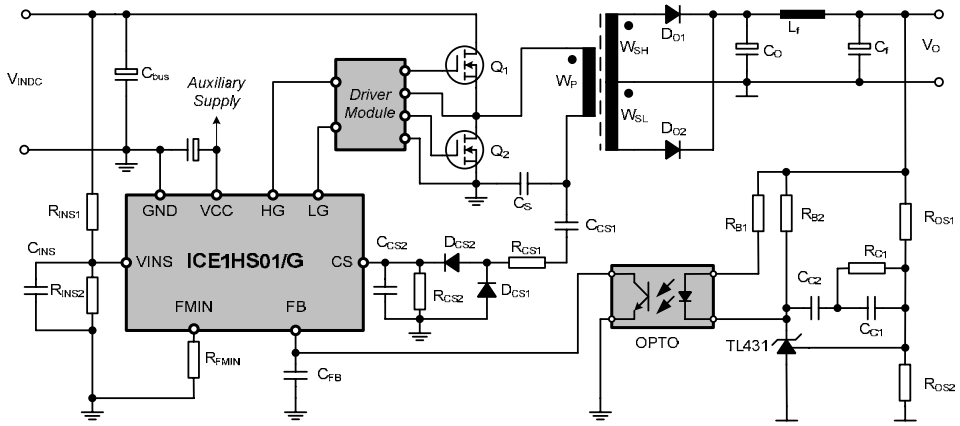


Figure 1 Typical application of 8-pin half bridge LLC controller ICE1HS01G

Figure 1 shows a typical application of ICE1HS01G in half bridge LLC resonant converter. The driver module can be implemented by either a pulse transformer or a high voltage driver IC. The mains input voltage is normally around 380Vdc delivered by the frontend PFC pre-regulator. The MOSFETs Q_1 and Q_2 are driven complementarily to generate a square waveform at the input of the resonant tank. The elements of the resonant tank are the resonant inductance L_r, the magnetising inductance L_m of the transformer and the resonant capacitor C_s. L_r is often realized with the leakage inductance of the transformer. During operation, the primary MOSFETs Q_1 and Q_2 are turned-on under ZVS condition, and the secondary rectifier diodes D_{O1} and D_{O2} are turned-on and turned-off under ZCS condition. Hence high switching frequency and high power density can be achieved. In addition, MOSFETs Q_1 and Q_2 and rectifier diodes D_{O1} and D_{O2} have low voltage stresses clamped by the input and output voltages, respectively. Hence, the devices with lower voltage rating can be used, and consequently lower conduction loss and lower cost can be further achieved.

3 IC Description

ICE1HS01G is an 8-pin controller IC; nevertheless, it includes all necessary protection features for HB LLC resonant converter. ICE1HS01G allows the designer to choose suitable operation frequency range by programming the oscillator with an external resistor. And the programmed soft-start function to limit both the inrush current and the overshoot of output voltage is also provided. In addition, ICE1HS01G performs all necessary protection functions in HB LLC resonant converters. All of these make ICE1HS01G an outstanding product for HB LLC resonant converter in the market.

3.1 Main Features

- Maximum 600kHz switching frequency
- Adjustable minimum switching frequency with high accuracy
- 50% duty cycle
- Mains input under voltage protection with adjustable hysteresis
- Two levels of overcurrent protection: frequency shift and latch off
- Open-loop/over load protection with adjustable blanking time
- Built-in digital and nonlinear softstart
- Adjustable restart time during over load protection

3.2 Pin Configuration

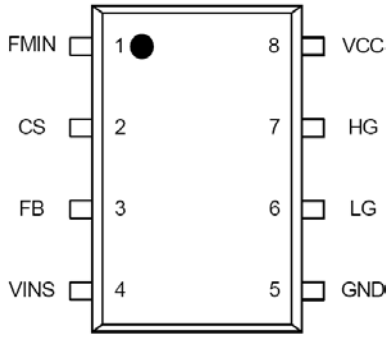


Figure 2 Pin configuration (top view)

3.3 Pin Functions

FMIN (Minimum Switching Frequency)

An external resistor R_{FMIN} is connected between this pin and the ground. The voltage of this pin is constant during operation and thus the resistance determines the current flowing out of this pin. The minimum switching frequency is determined by this current. The maximum switching frequency during normal operation and the maximum switching frequency during soft start are both related to the current flowing out of FMIN pin.

CS (Current Sense)

The current sense signal is fed to this pin. Inside the IC, two comparators are provided. If the voltage on CS pin is higher than the first threshold (0.8V typically), IC will increase the switching frequency to limit the maximum output power of the converter. If the voltage on this pin exceeds the second threshold(1.6V typically), IC will be latched off immediately.

FB (Feedback)

This pin is connected to the collector of the external optocoupler. Internally, during normal operation, this pin is connected to reference voltage source with a pull-up resistor (R_{FB}). The IC uses the voltage on this pin to adjust the switching frequency within the range of maximum and minimum frequency set by FMIN pin. If FB

voltage is higher than V_{FBH} for a certain internallyn fixed blanking time (20ms), an extended timer will be started. If over load/open loop protection exists longer than the extended blanking time, IC will enter auto-restart mode. Another off timer starts from the instant IC stops switching till IC starts another soft start. This off timer is determined by the resistors and capacitor connected to VINS pin. More details regarding this function are provided in section 4.6 and 4.7.

VINS (Mains Input Voltage Sense)

The mains input voltage is fed to this pin via a resistive voltage divider. If the voltage on VINS pin is higher than the threshold V_{INSon} (1.25V typically), IC will start to operate with softstart when VCC increases beyond turn on threshold (12V typically). During operation, if the voltage on this pin falls below the threshold V_{INSon}, IC will stop switching until the voltage at this pin increases again. When IC goes into over load protection mode, IC will stop switching and try to restart after a period of time. This period is adjustable by the RC network connected between VINS pin and ground. More details regarding this function are provided in section 4.7.

GND (Ground)

IC common ground.

LG (Low Side Gate Drive)

Low side power MOSFET driver.

HG (High Side Gate Drive)

High side power MOSFET driver.

VCC (IC Power Supply)

Supply voltage of this IC, VCC pin should be connected to an external auxiliary supply.

4 Application Information

4.1 Minimum switching frequency

The minimum switching frequency is a very important factor. ICE1HS01G allows the minimum switching frequency easily programmed by connecting an external resistor R_{FMIN} between FMIN pin and ground.

The IC internal circuit provides a regulated 1.5V voltage at FMIN pin. The resistor R_{FMIN} , connected from FMIN pin to GND, determines the current(I_{FMIN}) flowing out from FMIN pin. A certain current proportional to I_{FMIN} is defined as the minimum charging current(I_{chg_min}), which in turn defines the minimum switching frequency. The maximum switching frequency during normal operation and the switching frequency variation range during soft start and over current protection are all related to this current flowing out of FMIN pin, which will be discussed in the following section.

The relationship between minimum switching frequency and R_{FMIN} is shown in Figure 3.

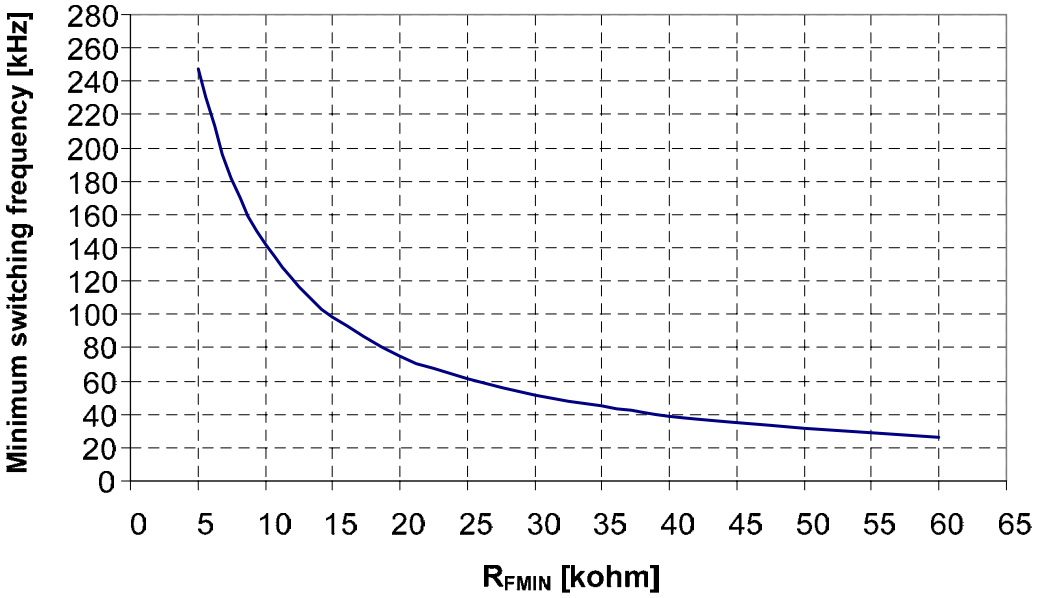


Figure 3 Minimum switching frequency VS R_{FMIN}

4.2 IC power supply and soft start

The controller ICE1HS01G is targetting at applications with auxiliary power supply. In most cases, a front-end PFC pre-regulator with a PFC controller is used in the same system.

The controller ICE1HS01G starts to operate when the supply voltage VCC reaches the on-threshold, typically 12V. The minimum operating voltage after turn-on, VCCoff, is typically 11V. The maximum supply voltage VCCmax is 18V. It is suggested that IC is supplied with a regulated dc power supply for stable operation. At the same time, a small bypass filter capacitor 100nF is suggested to be put between VCC and GND pins, as closely as possible.

After IC supply voltage is higher than 12V, and if the voltage on VINS pin is higher than 1.25V, IC will start switching with soft start. The soft start function is built inside the IC with a digital manner. During softstart, the switching frequency of the MOSFET is controlled internally by changing the current I_{SS} instead of by the feedback voltage. The charging current I_{SS} during soft start, which determines the switching frequency, is reduced step by step as shown in product datasheet [1]. The maximum duration of softstart is 32ms with 1ms for each step. Figure 4 illustrates the actual switching frequency VS start time when R_{FMIN}=22kohm. During softstart, the frequency starts from 250kHz, and step by step drops to normal operation point.

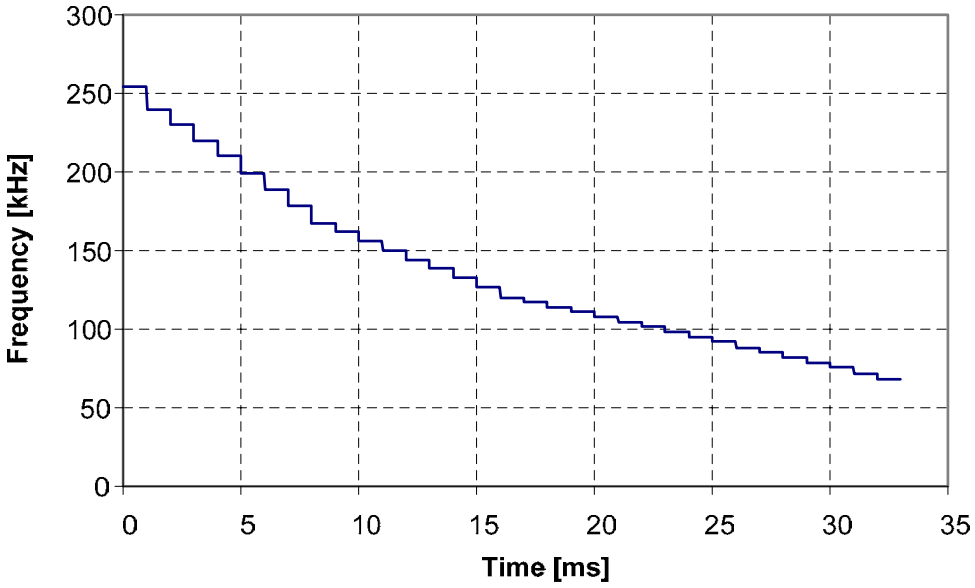


Figure 4 Switching frequency during softstart @ R_{Fmin}=22kohm

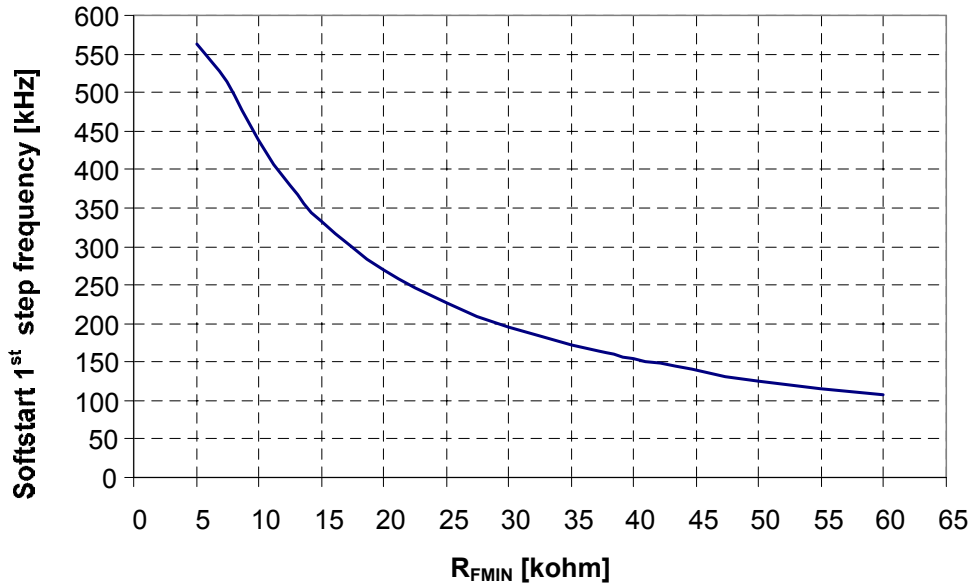


Figure 5 Soft start 1st step switching frequency VS R_{Fmin}

The soft start 1st step switching frequency, maximum frequency during softstart, is also closely related to the minimum switching frequency fixed by external R_{Fmin} resistance. Figure 5 illustrates the relationship between the 1st step frequency and R_{Fmin}.

During this 32ms soft start, the overload protection is disabled.

4.3 Over Current Protection

Current sense pin in ICE1HS01G is only for protection purpose. ICE1HS01G features two-level over current protection. In case of over-load condition, the lower OCP level，0.8V，will be triggerred, the switching frequency will be increased according to the duration and power of the over load. The higher OCP level，1.6V，is used to protect the converter if transformer winding is shorted. When V_{cs} reaches 1.6V, the IC will be latched immediately.

If V_{cs} is higher than 0.8V, IC will boost up the switching frequency. If V_{cs} is lower than 0.75V, IC will resume to normal operation gradually. If V_{cs} is always higher than 0.8V for 1.5ms, the frequency will rise to its maximum level, and vice versa.

To sum up, ICE1HS01G will increase the switching frequency to limit the resonant current in case of temporary over-load and will also decrease the switching frequency to its normal value after over-load condition goes away.

4.4 Feedback

The output load information is fed into the controller through feedback voltage V_{FB}. Inside the IC, the feedback (FB) pin is connected to the 5V voltage source through a pull-up resistor R_{FB}. Outside the IC, this pin is connected to the collector of opto-coupler. Normally, a ceramic capacitor C_{FB} can be put between this pin and ground for signal smoothing purpose, also C_{FB} is used to determine the extended blanking time for over load protection, which will be discussed in section 4.6

If the output load is increased, and consequently V_{FB} is higher, ICE1HS01G will reduce the switching frequency to regulate the output voltage and vice versa. The regulation of switching frequency is achieved by changing the charging current I_{FB}. The relationship between I_{FB} and V_{FB} can be found in product datasheet [1]. The effective range of feedback voltage V_{FB} is from 0.8V to 3.8V. Figure 6 graphs the relationship between the actual switching frequency and feedback voltage V_{FB} when R_{FMIN}=22kohm.

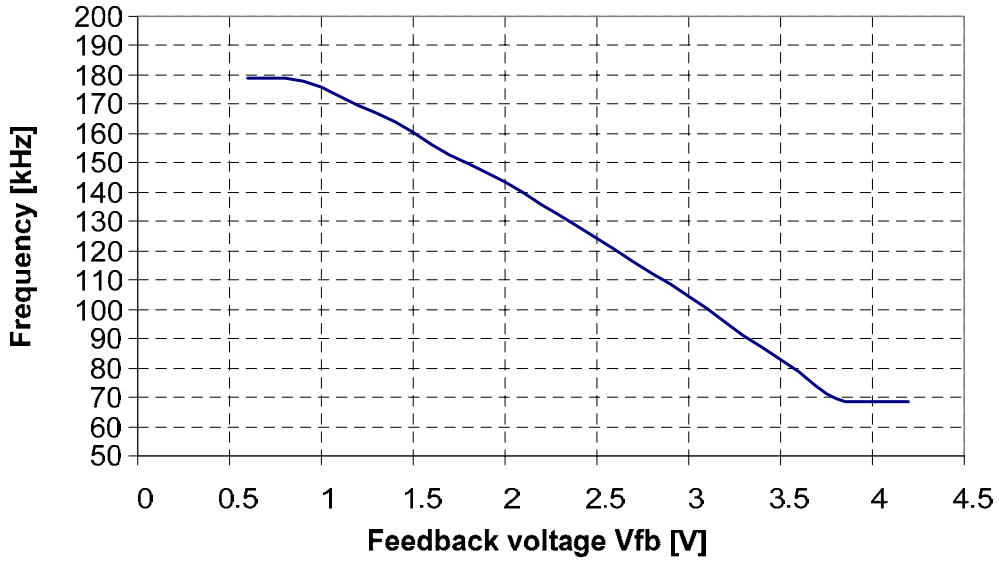


Figure 6 Switching frequency VS feedback @ R_{Fmin}=22kohm

At very light load condition with high input voltage, the designed maximum frequency may not be high enough to regulate the output voltage. In order to avoid this case, the feedback signal V_{FB} is continuously monitored. When V_{FB} drops below V_{FB_off} (typical 0.2V), the switching signal will be disabled after a fixed blanking time T_{FB} (typical 200ns). V_{FB} will then rise as Vout starts to decrease due to no switching signal. Once V_{FB} exceeds the threshold V_{FB_on} (typical 0.3V), IC resumes to normal operation.

4.5 Input voltage sense

The working range of mains input voltage needs to be specified for LLC resonant converter. It is important for the controller to have input voltage sensing function and protection features, which allows the IC to stop switching when the input voltage drops below the specified range and restart with soft start when the input voltage resumes to its normal level. The mains input voltage sensing circuit is shown in product datasheet [1]. Thanks to the internal current source I_{hys} connected between VINS pin and Ground, an adjustable hysteresis between the on and off threshold of mains input voltage can be created as

$$V_{hys} = R_{INS1} \cdot I_{hys}$$

The mains input voltage is divided by R_{INS1} and R_{INS2}. If the on and off threshold for mains input voltage is V_{mainon} and $V_{mainoff}$, the resistors R_{INS1} and R_{INS2} can be selected as

$$R_{INS1} = \frac{V_{mainon} - V_{mainoff}}{I_{hys}}, \qquad R_{INS2} = R_{INS1} \cdot \frac{V_{VINSon}}{V_{mainoff} - V_{VINSon}}$$

4.6 Blanking time in case of over load protection

In case of output over load or open control loop fault, the FB voltage will increase to its maximum level. If FB voltage is higher than V_{FBH} and this condition last longer than a fixed blanking time of T_{OLP} (20ms), the IC will start the extended blanking timer. The extended blanking timer is realized by charging and discharging the filter capacitor C_{FB} via the internal pull up resistor R_{FB} and switch Q_{FB}. The circuit for extended blanking time is shown in Figure 7.

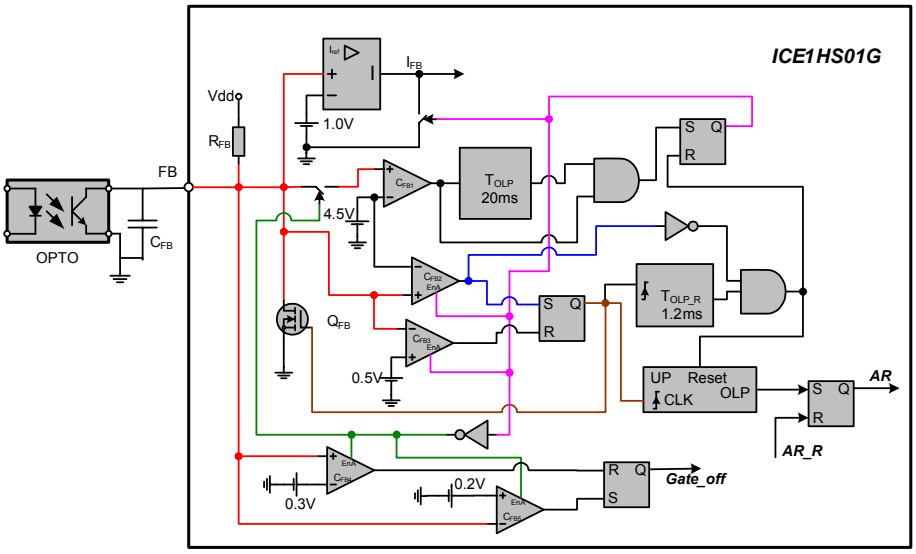


Figure 7 Circuit connected to FB pin

The FB voltage waveform during an OLP period is shown in Figure 8. After FB voltage has been higher than V_{FBH} (4.5V typically) for the fixed blanking time t1 shown in Figure 8, IC will use internal switch Q_{FB} to discharge V_{FB} to V_{FBL} (0.5V typically). After the switch Q_{FB} is released, C_{FB} will be charged up by Vdd through R_{FB}. The time needed for C_{FB} being charged from V_{FBL} to V_{FBH} can be calculated as:

$$t_{chg\_olp} = -\ln\left(\frac{V_{dd} - V_{FBH}}{V_{dd} - V_{FBL}}\right) \cdot R_{FB} \cdot C_{FB}$$

The time needed for C_{FB} being discharged from V_{FBH} to V_{FBL} can be calculated as:

$$t_{dischg\_olp} = \ln\left(\frac{V_{FBH}}{V_{FBL}}\right) \cdot R_{QFB} \cdot C_{FB}$$

where R_{QFB} is switch Q_{FB}'s on resitance. If C_{FB} is 680pF, t_{chg_olp} is about 30us, t_{dischg_olp} is about 1.4us.

After V_{FB} reaches V_{FBH}, an internal counter will increase by 1 and the capacitor is discharged to V_{FBL} by Q_{FB} again. The charging and discharging process of C_{FB} will be repeated for N_{OLP_E} times (N_{OLP_E}=512) if the fault condition still exists. After the last time of N_{OLP_E}, the FB voltage is pulled down to V_{FBL}, IC will stop switching when FB voltage rises to V_{FBH} again. This is called over load/ open loop proteciton. During the charging and discharging period, the IC will operate with frequency determined by I_{chg_min} and I_{CS}.

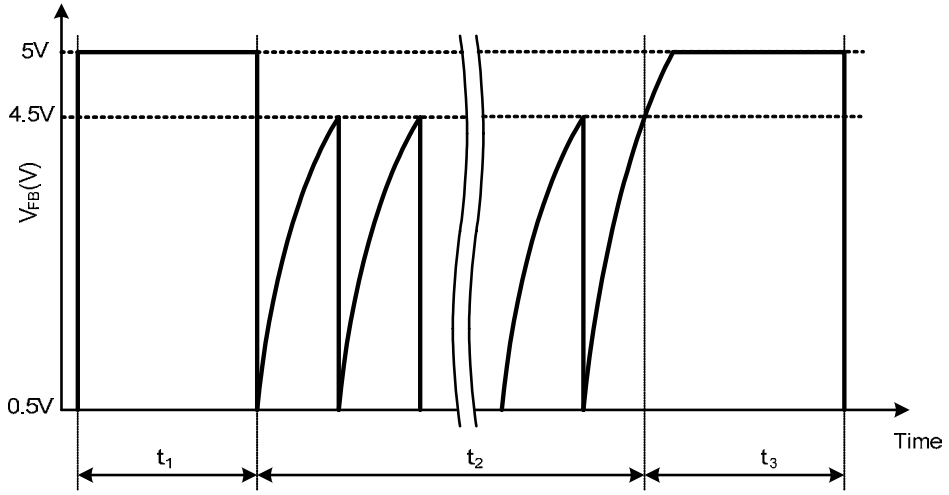


Figure 8 FB voltage waveform during over load protection

If the converter returns to normal operation during the extended blanking time period as mentioned above, FB voltage can not go up to V_{FBH} again. Therefore, after FB voltage is discharged to zero voltage, if it can not go up to V_{FBH} within T_{OLP_R} (1.28ms typically), IC will reset all the fault timer to zero and return to normal operation.

4.7 Auto restart time in case of over load protection

After IC enters into OLP, both switches will be stopped. However, the IC remains active and will try to start with soft start after an adjustable period. This period is realized by charging and discharging the capacitor C_{INS} ,connected to VINS pin, for N_{OLP_R} times (N_{OLP_R}=2048), hence, this period can be adjusted by C_{INS}, R_{INS1} and R_{INS2}. The circuit implementation of the adjustable off time is shown in Figure 9, and Figure 10 shows the voltage waveform of VINS pin in this case.

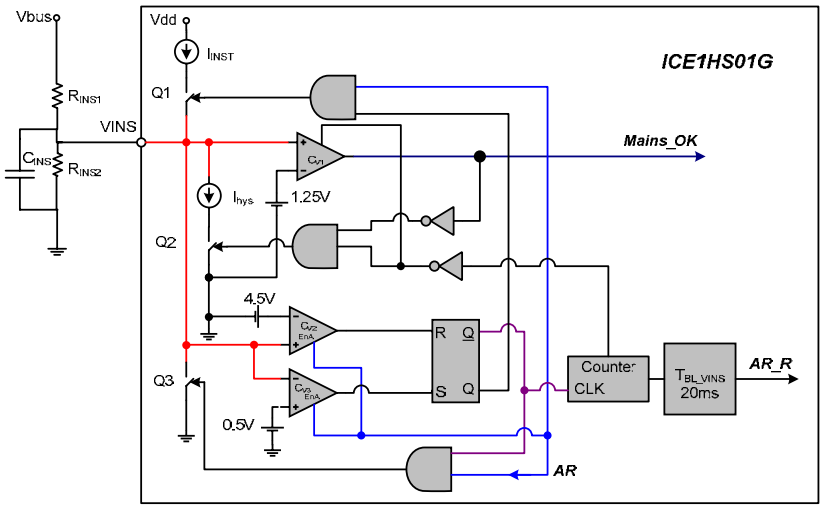


Figure 9 Circuit connected to VINS pin

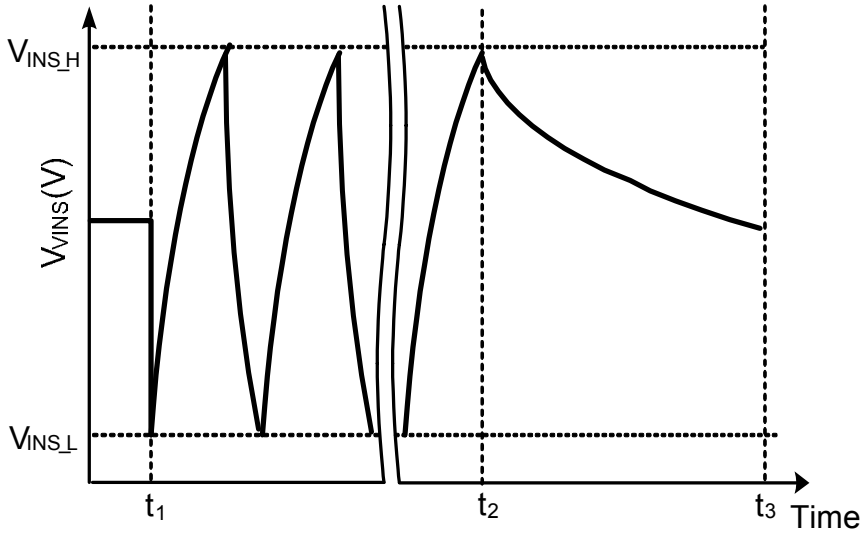


Figure 10 VINS voltage waveform during restart time

As shown in Figure 10, the voltage across C_{INS} is discharged to V_{INS_L} (0.5V typically) when IC goes into OLP at time t1. After that, an internal constant current source I_{INST} is turned on to charge C_{INS}. Once the voltage at VINS pin is charged to V_{INS_H} (4.5V typically), the current source will be turned off and C_{INS} is discharged by another switch Q3 to V_{INS_L} again. The charging and discharging of C_{INS} comprise one cycle. This cylce time is also influenced by the bus voltage. The charging and discharging time of C_{INS} can be approximated as

$$t_{charging} = -R_{eq} \cdot C_{INS} \cdot \ln\left(\frac{V_{BUS} \cdot \frac{R_{eq}}{R_{INS1}} + I_{INST} \cdot R_{eq} - V_{INSH}}{V_{BUS} \cdot \frac{R_{eq}}{R_{INS1}} + I_{INST} \cdot R_{eq} - V_{INSL}}\right)$$

$$t_{discharging} = -R_{eq2} \cdot C_{INS} \cdot \ln\left(\frac{V_{BUS} \cdot \frac{R_{eq2}}{R_{INS1}} - V_{INSL}}{V_{BUS} \cdot \frac{R_{eq2}}{R_{INS1}} - V_{INSH}}\right)$$

where R_{eq} is the equivalent resistance for parallelling of R_{INS1} and R_{INS2},

$$R_{eq} = R_{INS1} // R_{INS2}$$

R_{eq2} is the equivalent resistance for parallelling of R_{INS1}, R_{INS2} and R_{Q3} (900ohm typically).

$$R_{eq2} = R_{INS1} // R_{INS2} // R_{Q3}$$

IC will repeat the charging and discharging process for N_{OLP_R} times (N_{OLP_R}=2048). After that, IC will turn off the switches for both charging and discharging. In addition, the current source for hysteresis will be turned on and another blanking time of T_{BL_VINS}, the time between t2 and t3 as shown in Fiugre 10 will be added so that VINS pin fully recovers and represents the bus voltage information. IC will start the soft start after the additional blanking time in case V_{VINS} is higher than the V_{VINSon}.

5 Design Example

A 24V 200W LLC demoboard using ICE1HS01G is now available. In order to simplify and speed up this IC's feature evaluation, no PFC stage is implemented, so 280Vac input is recommended to feed this 200W demboard, thus around 380Vdc across bulk capacitor can be obtained.

5.1 Design Specifications

The LLC stage is usually used to follow a PFC stage, thus the nominal input voltage for LLC stage can be specified as:

$$V_{in\_nom} = 400\text{Vdc}$$

Output voltage is specified as 24V: $V_{out} = 24\text{V}$

Output current is specified as 8A: $I_{out} = 8\text{A}$

The required hold-up time: $T_h = 20\text{ms}$

The PFC output capacitor: $C_o = 220\text{uF}$

5.2 Define System Specifications

The estimated efficiency: $\eta = 0.93$

The input power will then be: $P_{in} = \frac{V_{out} \cdot I_{out}}{\eta} = 206.45\text{W}$

During the hold up time, the input voltage for LLC stage drops gradually to a lower level, and the output voltage of LLC stage is still required to be regulated. The required minimum input DC voltage can be estimated as:

$$V_{in\_\min} = \sqrt{V_{in\_nom}{}^2 - \frac{2 \cdot P_{in} \cdot T_h}{C_o}} = 349.95\text{V}$$

The resonant frequency is selected as: $f_r = 100\text{kHz}$

5.3 Define the Required Voltage Gain of the Resonant Network

The integrated magnetic solution is often be used for LLC resonant design. The resonant inductance L_r is often combined with the transformer into a single magnetic part. The transfomer's physical model is shown in Figure 11, where the topological analogy with the inductive part of the LLC resonant tank circuit is apparent.

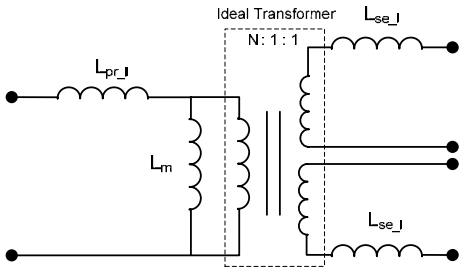


Figure 11 LLC integrated transformer model

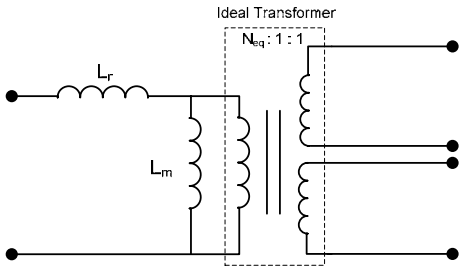


Figure 12 Transformer primary referred model

The transformer's all primary referred model is shown as Figure 12, where n_{eq} is the equivalent turn ratio. All the elements related to leakage flux are located on the primary side.

If ***Lp*** is defined as the primary inductance mearured at primary side with secondary winding open, Lp will be the sum of ***Lr*** and Lm. Considering the influence of secondary leakage inductance, the equivalent turn ratio can be estimated as [4]:

$$n_{eq} = \frac{n}{\sqrt{\frac{L_p}{L_p - L_r}}} = \frac{n}{\sqrt{\frac{m}{m-1}}}$$

where n is the transformer's physical turn ratio;

m is the ratio between primary inductance L_p and resonant inductance L_r: $m = L_p / L_r$

The equivalent circuit for LLC resonant network is ploted as Figure 13.

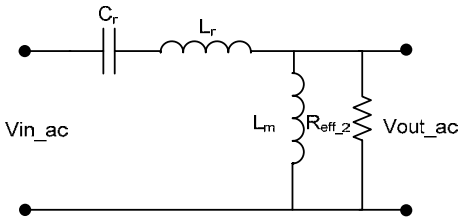


Figure 13 Equivalent circuit for LLC resonant network

where C_r is the resonant capacitor;

L_r is the resonant inductance, which is made by the transformer primary leakage inductance and the reflected secondary leakage inductance;

L_m is the magnetizing inductane;

R_{eff_2} is the effective load resistance considering the influence of secondary leakage inductance:

$$R_{eff\_2} = \frac{8}{\pi^2} \cdot n_{eq}^{\ 2} \cdot \frac{V_{out}}{I_{out}}$$

The input RMS voltage V_{in_ac} across the resonant network can be calculated as:

$$V_{in\_ac} = \frac{\sqrt{2}}{\pi} V_{in\_dc}$$

where V_{in_dc} is the DC input voltage for LLC stage, which is usually powered by frontend PFC stage.

The output RMS voltage V_{out_ac} across the effective load resistance is:

$$V_{out\_ac} = \frac{2\sqrt{2}}{\pi} V_{out} \cdot n_{eq}$$

Thus the voltage gain can be calculated as: $G = \frac{V_{out\_ac}}{V_{in\_ac}} = \frac{2 n_{eq} V_{out}}{V_{in\_dc}}$

As shown in Figure 13, the resonant network and the load acts as a voltage divider, the expression of the voltage gain can be obtained as:

$$G=\frac{2n_{eq}V_{out}}{V_{in\_dc}}=\left|\frac{\left(\frac{f}{f_r}\right)^2\cdot(m-1)}{\left(\frac{f^2}{f_p{}^2}-1\right)+j\left(\frac{f}{f_r}\right)\cdot\left(\frac{f^2}{f_r^2}-1\right)\cdot(m-1)\cdot Q_e}\right|=\frac{F^2(m-1)}{\sqrt{\left(m\cdot F^2-1\right)^2+F^2\left(F^2-1\right)^2(m-1)^2Q_e{}^2}}$$

with the following parameter definitions:

right-side resonant frequency: $f_r=\frac{1}{2\pi\sqrt{L_rC_r}}$

left-side resonant frequency: $f_p=\frac{1}{2\pi\sqrt{L_pC_r}}$

inductance ratio: $m=\frac{L_p}{L_r}$

normalized frequency: $F=\frac{f}{f_r}$

quality factor: $Q_e=\sqrt{\frac{L_r}{C_r}}\cdot\frac{1}{R_{eff\_2}}=\sqrt{\frac{L_r}{C_r}}\cdot\frac{8}{\pi^2}\cdot n_{eq}{}^2\cdot\frac{V_{out}}{I_{out}}$.

Considering $n_{eq}=\frac{n}{\sqrt{\frac{L_p}{L_p-L_r}}}=\frac{n}{\sqrt{\frac{m}{m-1}}}$, another voltage gain G' directly related to the physical turn ratio n can be expressed as:

$$G'=\frac{2nV_{out}}{V_{in\_dc}}=\left|\frac{\left(\frac{f}{f_r}\right)^2\cdot\sqrt{m(m-1)}}{\left(\frac{f^2}{f_p{}^2}-1\right)+j\left(\frac{f}{f_r}\right)\cdot\left(\frac{f^2}{f_r^2}-1\right)\cdot(m-1)\cdot Q_e}\right|=\frac{F^2\cdot\sqrt{m(m-1)}}{\sqrt{\left(m\cdot F^2-1\right)^2+F^2\cdot\left(F^2-1\right)^2(m-1)^2Q_e{}^2}}$$

For LLC topology, when operating close to the resonant point, the frequency's load-insensitivity can be achieved, thus the optimal operation point is put close to the resonant frequency point. Hence, the switching frequency is recommended to be put at the resonant point when LLC operates with nominal input voltage:

$$f_{s\_nom}=f_r$$

Based on above G' expression, the voltage gain at f_{s_nom} and V_{in_nom} can be given as:

$$G_{nom}=\sqrt{\frac{m}{m-1}}$$

Hence the gain at f_{s_nom} is determined by choosing the inductance ratio m .

Too small m means smaller L_p and bigger L_r, which will result in poor coupling of the transformer and deteriorate the efficiency due to increased circulating current. Typically m is set between 3 to 7.

If the chosen m value is: $m=5$

Then the voltage gain at f_{s_nom} and V_{in_nom} can be calculated as:

$$G_{nom} = \sqrt{\frac{m}{m-1}} = 1.12$$

Accordingly the maximum required voltage gain is at $V_{in\_\min}$ and can be given as:

$$G_{\max} = \frac{V_{in\_nom}}{V_{in\_\min}} \cdot G_{nom} = 1.28$$

5.4 Calculate the Transformer Turns Ratio

Assuming the secondary rectifier diode voltage drop V_f is:

$$V_f = 0.6\text{V}$$

The transformer turns ratio will be: $$n = \frac{V_{in\_nom}}{2 \cdot \left(V_{out} + V_f\right)} \cdot G_{nom} = 9.09 \approx 9$$

5.5 Calculate the Effective Load Resistance

The effective load resistance is: $$R_{eff} = \frac{8}{\pi^2} \cdot n^2 \cdot \frac{V_{out}}{I_{out}} = 196.97\Omega$$

If considering the transformer's secondary leakage inductance, the effective load resistance is:

$$R_{eff\_2} = \frac{8}{\pi^2} \cdot {n_{eq}}^2 \cdot \frac{V_{out}}{I_{out}} = \frac{R_{eff}}{{G_{nom}}^2} = 157.57\Omega$$

5.6 Determine the Resonant Network

The m value is chosen same as mentioned above: $m = 5$.

The gain equation can be recalculated as:

$$G' = \frac{2nV_{out}}{V_{in}} = \frac{F^2 \cdot \sqrt{m(m-1)}}{\sqrt{\left(m \cdot F^2 - 1\right)^2 + F^2 \cdot \left(F^2 - 1\right)^2 (m-1)^2 {Q_e}^2}} = \frac{1}{\sqrt{\left(\frac{5F^2 - 1}{F^2 \cdot \sqrt{20}}\right) + 0.8 \cdot {Q_e}^2 \cdot \left(F - \frac{1}{F}\right)^2}}$$

Then the frequency response of the voltage gain G' vs F and Q_e is plotted as following:

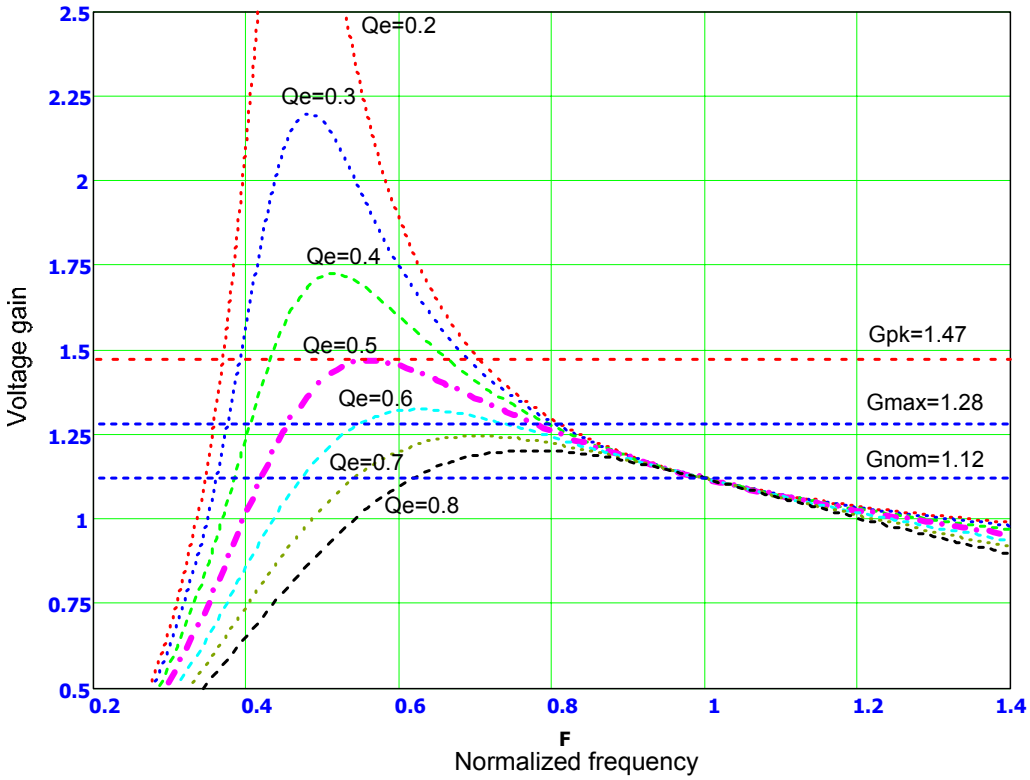


Figure 14 Voltage gain vs normalized frequency

As discussed above, the maximum required voltage gain $G_{\max}$ is calculated to meet the hold up time requirement. In addition, in order to ensure stable ZVS operation and meet the output voltage regulation requirement when LLC operates at the lowest allowable input voltage, the peak gain G_{PK} at full load condition should be somehow higher than $G_{\max}$.

Considering 15% margin: $G_{pk} = 1.15 \cdot G_{\max} = 1.47$

According to Figure 14, the voltage gain when $Q_e = 0.5$ can meet this peak gain requirement.

Accordingly, the resonant capacitor can be selected as:

$$C_r = \frac{1}{2\pi \cdot Q_e \cdot f_r \cdot R_{eff\_2}} = 20.2\text{nF}$$

Also the resonant inductance will then be: $L_r = \frac{1}{(2\pi \cdot f_r)^2 \cdot C_r} = 125.39\text{uH}$

The primary inductance is: $L_p = m \cdot L_r = 626.97\text{uH}$

When using the integrated magnetic solution, the resonant inductance L_r is implemented by the leakage inductance, hence the value of L_r is not easy to control. The resonant network parameters based on above calculation often needs to be changed according to the measured inductance values and the standard capacitance value.

5.7 Transformer Design

The worst case for LLC transformer's operation is that when LLC operates at minimum switching frequency when input DC voltage drops to the lowest allowable voltage and full load.

The maximum required voltage gain occurs at $V_{in\_\min}$ and can be given as:

$$G_{\max} = \frac{V_{in\_nom}}{V_{in\_\min}} \cdot G_{nom} = 1.28$$

Base on Figure 14, it can be roughly estimated that

$$G = 1.28 \text{ when } F = 0.78 \text{ and } Q_e = 0.5$$

Accordingly the minimum switching frequency can be obtained as:

$$f_{\min} = F \cdot f_r = 78\text{kHz}$$

According to Faraday's Law, the minimum number of primary turns for LLC transformer can be estimated as:

$$N_{p\_\min} == \frac{n_{eq} \cdot (V_{out} + V_f)}{2 f_{\min} \cdot \Delta B \cdot A_e} = \frac{n \cdot (V_{out} + V_f)}{\sqrt{m/(m-1)} \cdot 2 f_{\min} \cdot \Delta B \cdot A_e}$$

The transformer core is selected as PC47 EER32, its effective cross sectional area is:

$$A_e = 79.6\text{mm}^2$$

To avoid saturation, the flux density swing (peak to peak) is chosen as:

$$\Delta B = 0.45\text{T}$$

The minimum number of primary turns can be calculated as:

$$N_{p\_\min} = \frac{n \cdot (V_{out} + V_f)}{\sqrt{m/(m-1)} \cdot 2 f_{\min} \cdot \Delta B \cdot A_e} = \frac{9 \cdot (24\text{V} + 0.6\text{V})}{1.12 \cdot 2 \cdot 78\text{kHz} \cdot 0.45\text{T} \cdot 79.6\text{mm}^2} = 35.44$$

The actual number of primary turns can be selected as: $N_p = 36$

Accordingly the number of secondary turns is: $N_s = N_p / n = 4$

5.8 Primary current, Resonant Cap Voltage and OCP level

The primary RMS current flowing through resonant capacitor can be obtained as:

$$I_{r\_rms} = \frac{1}{\eta} \cdot \sqrt{\left(\frac{\pi \cdot I_{out}}{2\sqrt{2} \cdot n}\right)^2 + \left(\frac{n(V_{out} + V_f)}{4\sqrt{2} \cdot f_r \cdot M \cdot (L_p - L_r)}\right)^2} = 1.3\text{A}$$

Hence, the primary peak current is: $I_{r\_pk} = \sqrt{2} \cdot I_{r\_rms} = 1.84\text{A}$

The over current protection level is set to about 50% margin of this peak current:

$$I_{ocp} = (1 + 50\%) \cdot I_{r\_pk} = 2.76\text{A}$$

The maximum voltage across resonant capacitor occurs at nominal input dc voltage and OCP level:

$$V_{Cr\_\max} = \frac{V_{in\_nom}}{2} + \frac{I_{ocp}}{2\pi \cdot f_r \cdot C_r} = 436.36\text{V}$$

Thus, a 630V film capacitor with low ESR is recommened to be used as resonant capacitor.

5.9 Output Rectifier

For the output winding with center tap, the output diode voltage stress is

$$V_d = \left(V_{out} + V_f\right) \cdot 2 = 49.2\text{V}$$

The RMS current flowing through the output rectifier diode can be estimated as:

$$I_d = \frac{\pi}{4} \cdot I_{out} = 6.28\text{A}$$

6 Experiment Verification

A 200W half bridge LLC resonant converter demoboard with ICE1HS01G is implemented as shown in Figure 15. Also the full load efficiency of LLC stage has reached 94.35% as shown in Figure 22. The detailed schematic circuit is shown in Figure 16 and Figure 17.
The specification of this 200W LLC demoboard is listed as following table 1.

Table 1 200W Demoboard Specification

Normal Input AC voltage	280Vac
Normal DC bulk voltage	400Vdc
Mains under voltage protection point	300Vdc
Auxiliary power supply for IC VCC	15Vdc
Normal output full load	24V/8A
Switching frequency	100kHz @ 24V/8A and 400Vdc input

6.1 200W 24V HB LLC Resonant Converter using ICE1HS01G

Figure 15 200W half bridge LLC resonant converter demoboard using ICE1HS01G

6.2 Schematic of 200W Half Bridge LLC Resonant Converter

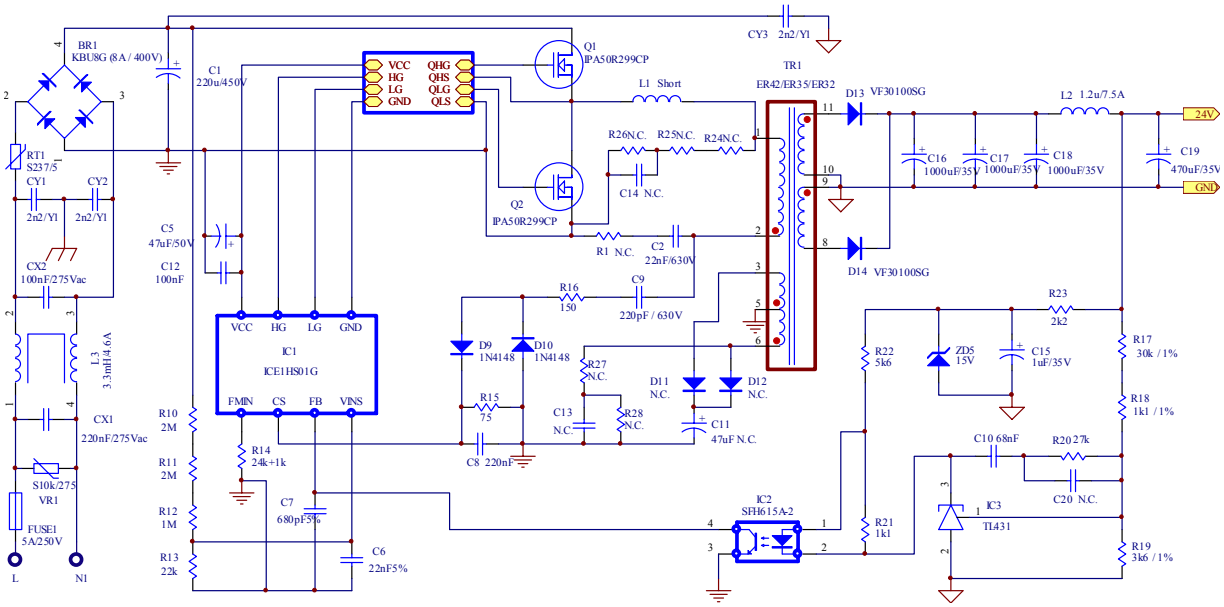


Figure 16 Schematics of 200W half-bridge LLC resonant converter

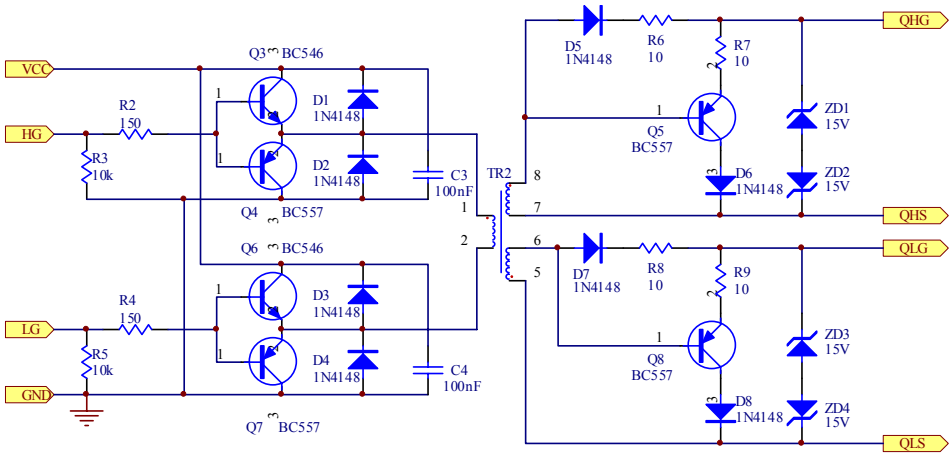


Figure 17 Schematics of driver circuit

The AC line input side comprises the input fuse FUSE1 as overcurrent protection. The X2 Capacitors CX1, CX2 and Choke L3 and Y1 capacitors CY1 and CY2 forms a main filter to minimize the feedback of RFI into the main supply. RT1 is placed in series with input to limit the initial peak inrush current. After the bridge rectifier BR1, together with a smoothing capacitor C1, a voltage of 300VDC to 400 VDC is provided, depending on mains input voltage, to simulate the real operation condition with front end PFC pre_regulator.

As shown in Figure 17, a cost-effective pulse transformer TR2 is used to transmit the driver signal to MOSFETs for isolation purpose. The totem pole driver circuits (optional), including a NPN and a PNP transistor is used to drive the pulse transformer. In the secondary side of the driver circuit, R7, R9, D6, D8, Q5, and Q8 are used to accelerate the turn-off speed of MOSFET. If the sink impedance of the pulse transformer is enough, these circuits can also be saved. In this case, a simplified driver circuit is shown in Figure 18.

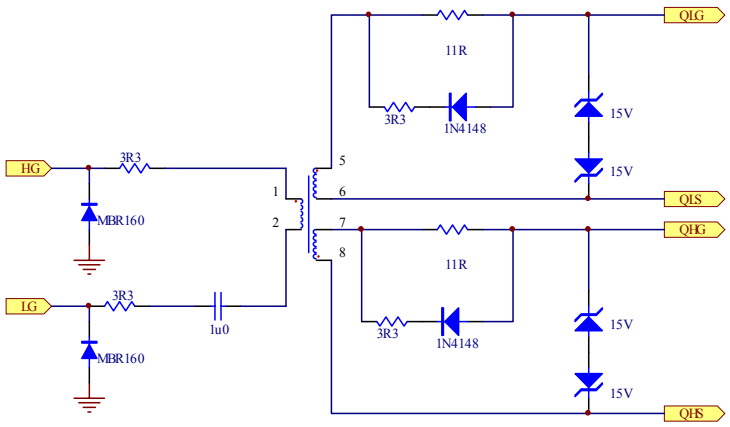


Figure 18 A simplified driver circuit

6.3 PCB Bottom Layer

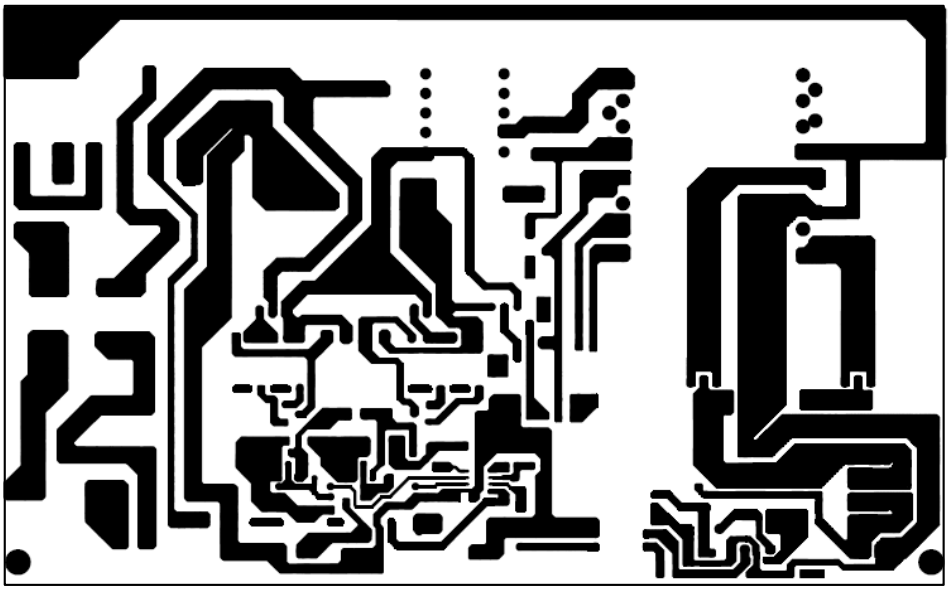


Figure 19 Solder side copper – View from component side

6.4 Transformer Construction

- Bobbin: Split type EC32, Horizontal version from TDK
- Core: PC47 ER32 from TDK
- Primary inductance: 616µH±5%, Gapped between Pin 1 and Pin 3
- Leakage inductance: 136µH±5%, measured between Pin 1 and Pin 3 by shorting (Pin 7 & 8)
- Measured at frequency of 40kHz

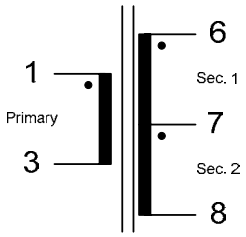


Figure 20 LLC resonant transformer electrical diagram

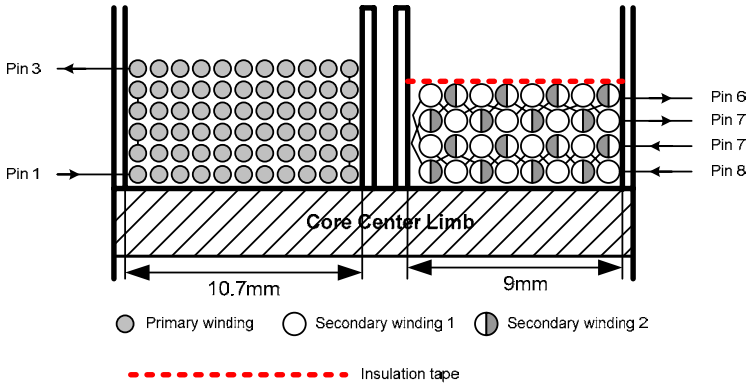


Figure 21 LLC resonant transformer winding position

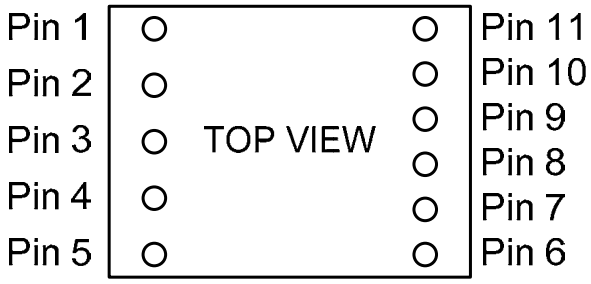


Figure 22 LLC resonant transformer complete – top view

Table 2 LLC resonant transformer winding characteristics

Pins	winding	turns	wire
1~3	primary	36	13*0.20
8~7	Secondary 1	4	18*0.20
6~7	Secondary 2	4	18*0.20

6.5 Test Results

- **Efficiency Mesurements**

Table 3 shows the output voltage measurements at the nominal input bulk voltage 400Vdc, with different load conditions. The bulk voltage 400Vdc is directly supplied from Chroma programmable DC power supply. Hense, there is no current flowing through the bridge rectifier, and the measured efficiency is actually the LLC stage's efficiency.

Table 3 Efficiency measurements @ Vbulk=400Vdc

24Vout [V]	24Vout current [A]	Pinput_main power [W]	Pinput_IC and Driver [W]	Poutput [W]	Efficiency [%]
23.92	7.980	201.8	15*0.034=0.51	190.882	94.35

23.92	6.977	175.9	15*0.034=0.51	166.890	94.60
23.93	5.989	150.9	15*0.034=0.51	143.317	94.65
23.93	4.986	125.6	15*0.034=0.51	119.315	94.61
23.93	3.984	100.5	15*0.034=0.51	95.337	94.38
23.93	2.996	75.9	15*0.034=0.51	71.694	93.83
23.93	1.993	51.1	15*0.035=0.525	47.692	92.38
23.93	0.990	26.5	15*0.035=0.525	23.691	87.66

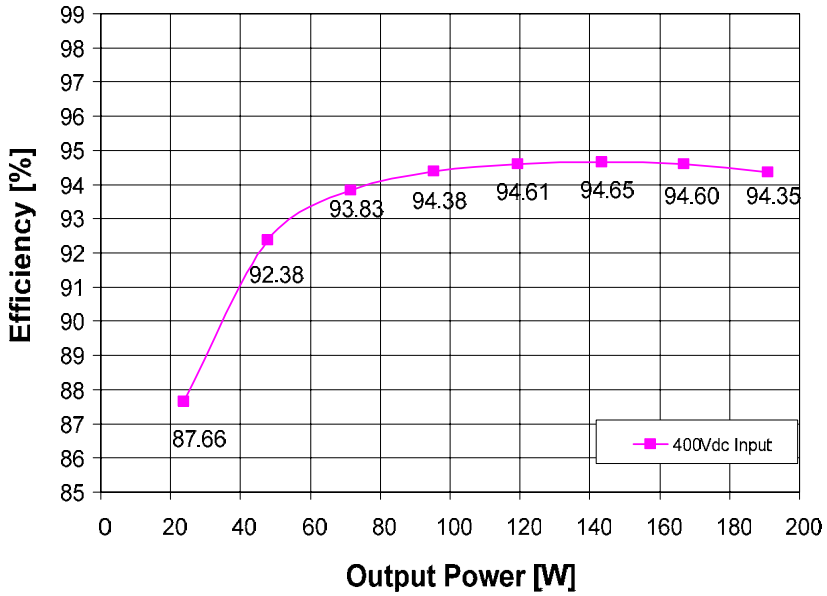
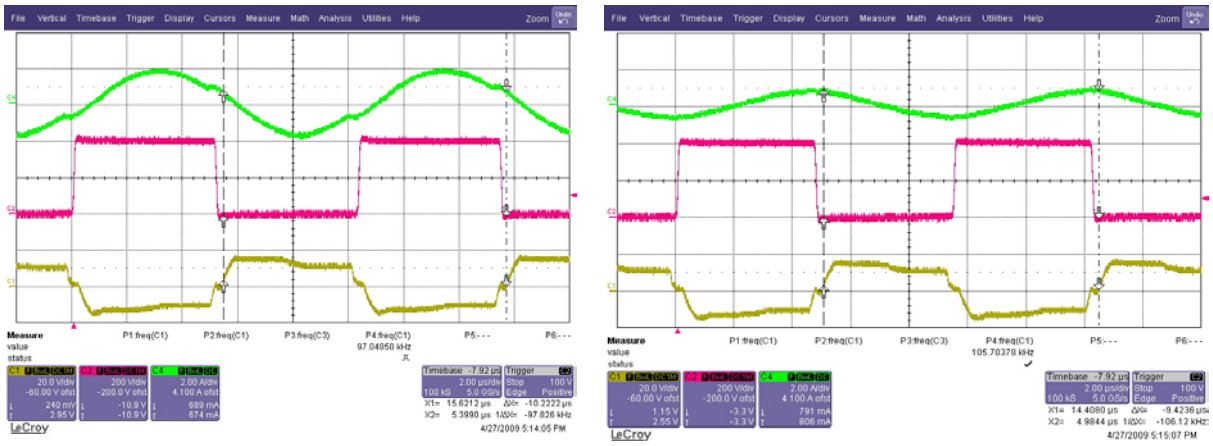


Figure 23 LLC stage efficiency

The power losses due to IC and driver circuit are both included. In addition, the efficiency values were measured after 30 minutes of warm-up at full load.

- **Resonant stage operating waveforms**



a. full load 8A output

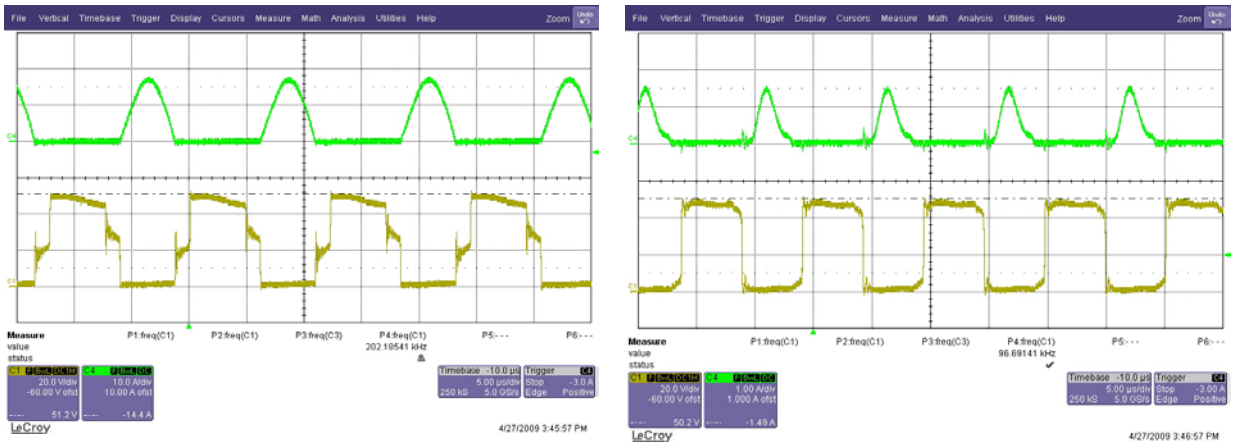
b. light load 0.5A output

Figure 24 Resonant stage operating waveforms

Figure 24 shows the resonant waveforms during steady state operation of this LLC resonant circuit at nominal dc input voltage 400Vdc and full load 8A and light load 0.5A condition. Channel 1 shows the Mosfet drive signal V_{gs}. The half bridge square voltage, which driving the resonant circuit, is shown in channel 2. It

can be found that the zero voltage switching is achieved. The primary resonant current is shown by channel 4, it is almost sinusoidal because the operating point is close to the resonant frequency f_r .

- **Secondary side operating waveforms**



a. full load 8A output

b. light load 0.5A output

Figure 25 Secondary rectifier diode voltage stress and flowing current

Figure 25 shows the voltage across the secondary rectifier diode, the voltage stress equals to 51V. The current flowing through rectifier diode is also shown by channel 4. This current shape is almost a sine wave, and its average value equals to one half the output current.

7 References

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