Guidelines for CoolSiC™ MOSFET gate drive voltage window

About this document

Infineon Technologies strives to enhance electrical systems with comprehensive semiconductor competence. Its expertise is revealed in its products and their behavior under relevant usage conditions, and in its willingness to share knowledge on latest semiconductor technologies. For new technologies, such as silicon carbide (SiC) MOSFETs, this is of particular importance because SiC MOSFETs under certain operating conditions show characteristics different from silicon (Si) switches. Experience and accompanying literature for this new technology are not available in public to the same extent as they are for technologies that have been in the market for a long time.

One important aspect to be considered for SiC MOSFETs is the gate threshold voltage ($V_{GS(th)}$) drift over long-term operations. Infineon was the first to discover this gate threshold voltage ($V_{GS(th)}$) drift caused by dynamic components over long-term operations. It was also the first to recommend an operating gate voltage area to minimize the drift.

After continuous research and development, the CoolSiC™ MOSFET M1H show a significant improvement in $V_{GS(th)}$ stability. The drift caused by the dynamic components is reduced significantly.

This version of the application note provides updated guidelines on the CoolSiC™ MOSFET gate voltage.

Scope and purpose

- Explain the long-term behavior of $V_{GS(th)}$ under switching operation
- To discuss its impact on the application
- To provide design guidelines to limit the related increase of on-state resistance $R_{DS(on)}$ as the major implication for the user in the application

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1 $V_{GS(th)}$ drift phenomenon

The nature of the wide-bandgap material SiC, and the different properties of the semiconductor-dielectric interface, compared to silicon material, causes some natural peculiarities in the threshold voltage variation and bias-temperature instability (BTI) that need to be understood and assessed. Extensive investigations have been conducted to understand such differences, to explain their relation to the semiconductor material, to clarify their relevance for the application, and to define the consequences with respect to specification and system design.

As far as the static gate-bias stress is concerned, standard test procedures typically used to characterize the threshold voltage and threshold voltage drifts for Si devices need to be adapted for SiC MOSFETs. Based on these findings, a new measurement stress procedure has been developed for the BTI evaluation of SiC MOSFETs, which allows one to distinguish between reversible threshold voltage hysteresis and more permanent threshold voltage drift (BTI). This measurement technique has been used for an in-depth study assessing the $V_{GS(th)}$-stability of recently launched SiC MOSFET parts. It has been demonstrated that Infineon 1200 V CoolSiC™ MOSFET excels in overall $V_{GS(th)}$ stability, in particular due to very low negative BTI and a very narrow drift variation among different devices [1].

Besides the drift driven by static stress, the threshold voltage of SiC MOSFET devices may undergo an additional drift triggered by switching events (turn-on and turn-off of the device). This additional component can only be identified in long-term switching tests. Current data shows that this effect is related to gate-oxide trap dynamics. As related internal studies have shown, this effect is a general characteristic of the current SiC MOSFET technologies. It is not limited to Infineon's CoolSiC™ MOSFET devices.

The characteristics of this phenomenon for Infineon CoolSiC™ MOSFET have been studied by performing long-term tests under various switching conditions. The data shows that switching stress leads to a slow $V_{GS(th)}$ increase over time. However, irrespective of the parameters chosen a negative switching-induced $V_{GS(th)}$ drift has never been observed. The $V_{GS(th)}$ drift value is similar among the different devices that have been stressed at the same operating conditions. An increase in threshold voltage, $V_{GS(th)}$, reduces the MOS channel overdrive ($V_{GS(on)} - V_{GS(th)}$) and therefore, an increased channel resistance (R_{ch}) is observed. This phenomenon is described in equation [1], where L is the length of the channel, W is the width of the channel, μ_n is the free electron mobility, C_{ox} is the gate oxide capacitance, $V_{GS(on)}$ is the positive on-state gate voltage, and $V_{GS(th)}$ is the threshold voltage of the device [2].

$$R_{ch} \approx \frac{L}{\mu_n \cdot C_{ox} \cdot W \cdot (V_{GS(on)} - V_{GS(th)})} \qquad (1)$$

The total $R_{DS(on)}$ resistance is determined by the sum of single resistances. These are the channel resistance (R_{ch}), the resistance of the junction field-effect transistor (R_{JFET}), the epitaxial layer resistance of the drift region (R_{epi}), and the resistance of the highly doped SiC substrate (R_{Sub}). The entire chain for the total $R_{DS(on)}$ is described in equation [2].
Thus, an increase in $V_{GS(th)}$ causes a slight increase in the channel resistance, which is followed by a slight increase in $R_{DS(on)}$, and a slight increase in on-state losses over time.

$$R_{DS(on)} = R_{ch} + R_{JFET} + R_{epi} + R_{Sub} \qquad (2)$$

VGS(th) drift phenomenon

The noticeable impact of the $V_{GS(th)}$ increase on the $R_{DS(on)}$ differs among the voltage classes of the devices. The higher the voltage class, the more pronounced is the contribution of the epitaxial layer resistance (R_{epi}). Consequently, the R_{epi} is more dominant, and contributes more to the total $R_{DS(on)}$ compared to smaller voltage classes like 650 V. As a consequence, we can conclude that the impact of the drift in $V_{GS(th)}$ on $R_{DS(on)}$ is less severe for higher voltage classes.

Please note that the basic function of the device is not affected, in particular:

- The blocking capability
- The reliability level of the devices (e.g., cosmic radiation robustness, humidity robustness, etc.)
- The $V_{GS(th)}$ drift has a negligible effect on the total switching losses

Key parameters that influence the switching-induced $V_{GS(th)}$ drift include:

- The number of switching events, translating into switching frequency and total operation time
- Gate drive voltage, mainly $V_{GS(off)}$
- The overshoot and undershoot of the gate-source terminal directly at the chip

The following operation parameters were found to have minor or negligible impact on the switching-induced $V_{GS(th)}$ drift:

- Junction temperature
- Switching slopes (dV/dt and dI/dt)
- Drain-source voltage
- Drain current

2 Impact on the application

The major impact of $V_{GS(th)}$ drift is a long-term increase in $R_{DS(on)}$ for the chosen V_{GS} in an application. Generally, an increase in $R_{DS(on)}$ increases conduction losses leading to an increase in junction temperature, T_{vj}, over time. This increase of T_{vj} over time should also be considered when assessing power cycling.

Whether T_{vj} increase is critical or not depends on individual applications and their operating conditions. In many cases the impact is minor and leads to a negligible increase in T_{vj} even after a lifetime of 20 years. In other applications, it could be more critical. Therefore, the design guideline shown in Chapter 3 must be considered.

The varying impact of a given, fixed-amplitude $V_{GS(th)}$ drift on different applications can be illustrated using two examples (half-bridge configuration in a DC-AC inverter). The first example represents applications in which conductions losses (P_{con}) dominate loss distribution. The second example represents applications in which both switching (P_{sw}) and conduction losses are equally distributed. The parameters of the two examples are listed in Table 1.

Table 1 Parameters of the two examples

	Example 1: Conduction losses dominate	Example 2: Conduction losses and switching losses are equally distributed
Switching frequency (kHz)	8	30
Nominal current (A)	50	38.5
Output voltage (V)	400	400
Output frequency (Hz)	50	50
DC link voltage (V)	600	600
Power factor	1	1
Thermal resistance (K/W)	3.6	3.6
Ambient temperature (°C)	40	40

For each example, the effects of $V_{GS(th)}$ drift on loss distribution and junction temperature are shown in Figure 1. Both examples have the same $V_{GS(th)}$ drift.

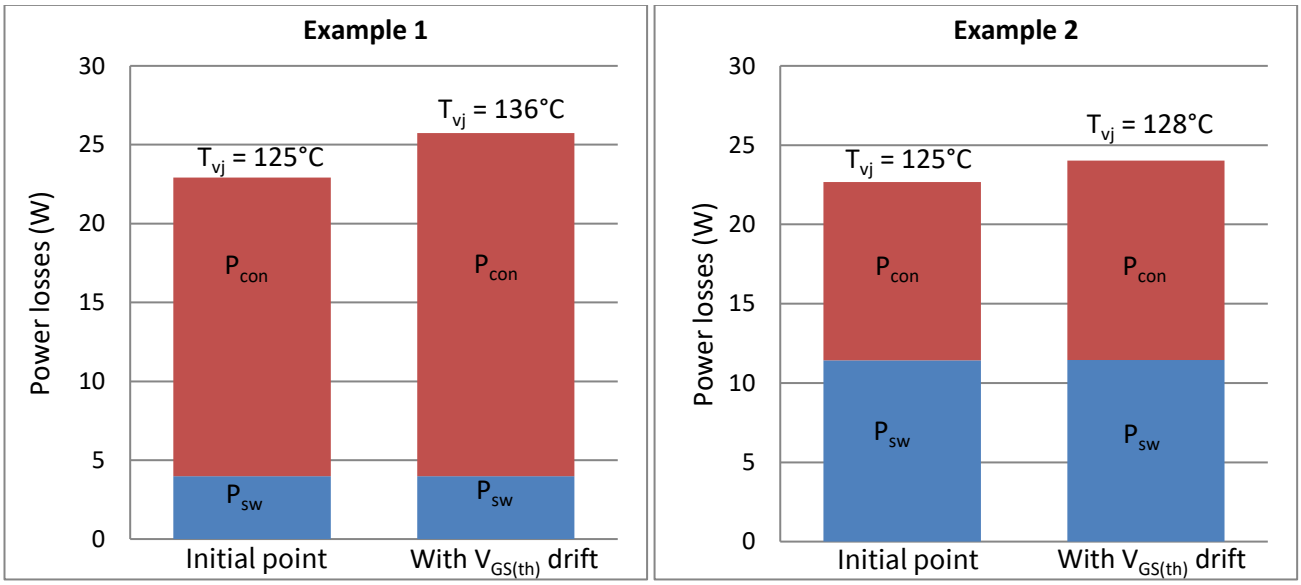

Figure 1 Examples of $V_{GS(th)}$ drift impact on applications

Impact on the application

As seen, in example 1 where conduction losses dominate, a $V_{GS(th)}$ drift leads to notably higher total loss and thus, to higher junction temperature. For such applications, the design guidelines detailed in Chapter 3 must be considered. For applications with balanced switching and conduction losses, a $V_{GS(th)}$ drift has only a minor effect on total loss and junction temperature.

Applications in which the overall losses are dominated by dynamic losses, the impact of $V_{GS(th)}$ drift is nearly negligible.

Infineon has developed a new stress test procedure – known as GSS – to identify drifts under realistic, application-oriented switching conditions. GSS test results show a comparable parameter drift as under real application conditions, and can now be established as a new test on the chip qualification plans to ensure long term performance and reliability [4]. The test is also described in JEDEC Guideline JEP195.

This is how Infineon assesses the worst-case $R_{DS(on)}$ drift at the end of mission profiles, presented in the following chapters.

3 Gate drive voltage guidelines

The sections in this chapter give guidance on how the change in $R_{DS(on)}$ can be predicted for different voltage classes and limited to an acceptable range.

3.1 Guidelines for 1200 V devices

The dynamic drift of the $V_{GS(th)}$ increases with the number of switching events. To understand this more clearly: the total number of switching events is translated into a normalized switching frequency, which takes into consideration 10 years of full operation (24h/7d). With the known actual switching frequency, f_{sw}, in kHz, the target lifetime in years, and the operating time as a percentage of the total system's lifetime, a normalized switching frequency can be defined using the following formula:

Normalized f_{sw} = actual f_{sw} [kHz] × lifetime [years] × operation time in percentage [%] ÷ 10 [years]

The recommended operating area provided by Infineon is differentseparately given for CoolSiC™ MOSFETs in module and in discrete packages even though the basic chip technology is the same. It is because overshoots and undershoots in the gate signal are strongly dependent on operation conditions, circuit design, and parasitics. In particular, the recommended operating area (ROA) for discrete devices is more conservative due to the greater flexibility in circuit design, application conditions, inverter topology, gate drive design, PCB layout, and thermal design. Due to these reasons, the ROA of discrete devices also include a potential overshoot of 2 V to account for variabilities in gate driver design. For modules, no extra overshoot needs to be considered because, since 0 V overshoot can be achieved in any case by a proper gate driver design.

With estimated normalized switching frequency based on an actual application, the minimum turn-off gate voltage, including a potential undershoot, can be extracted from Figure 2 and Figure 3, respectively for discrete and module products. The diagrams have been updated with new data for the Industry M1H version with improved gate oxide, as well as for Automotive M1, M1T, and M1H.

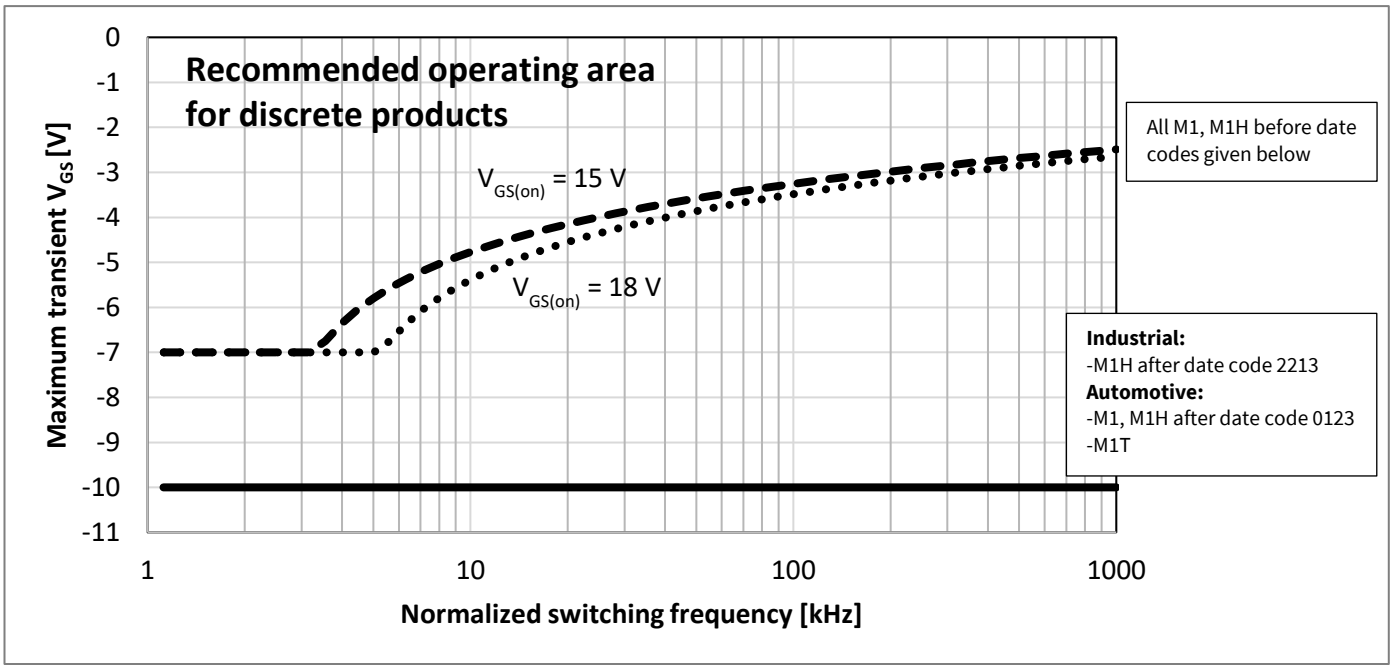

Figure 2 Minimum turn-off gate voltage for 1200 V discrete package products

Gate drive voltage guidelines

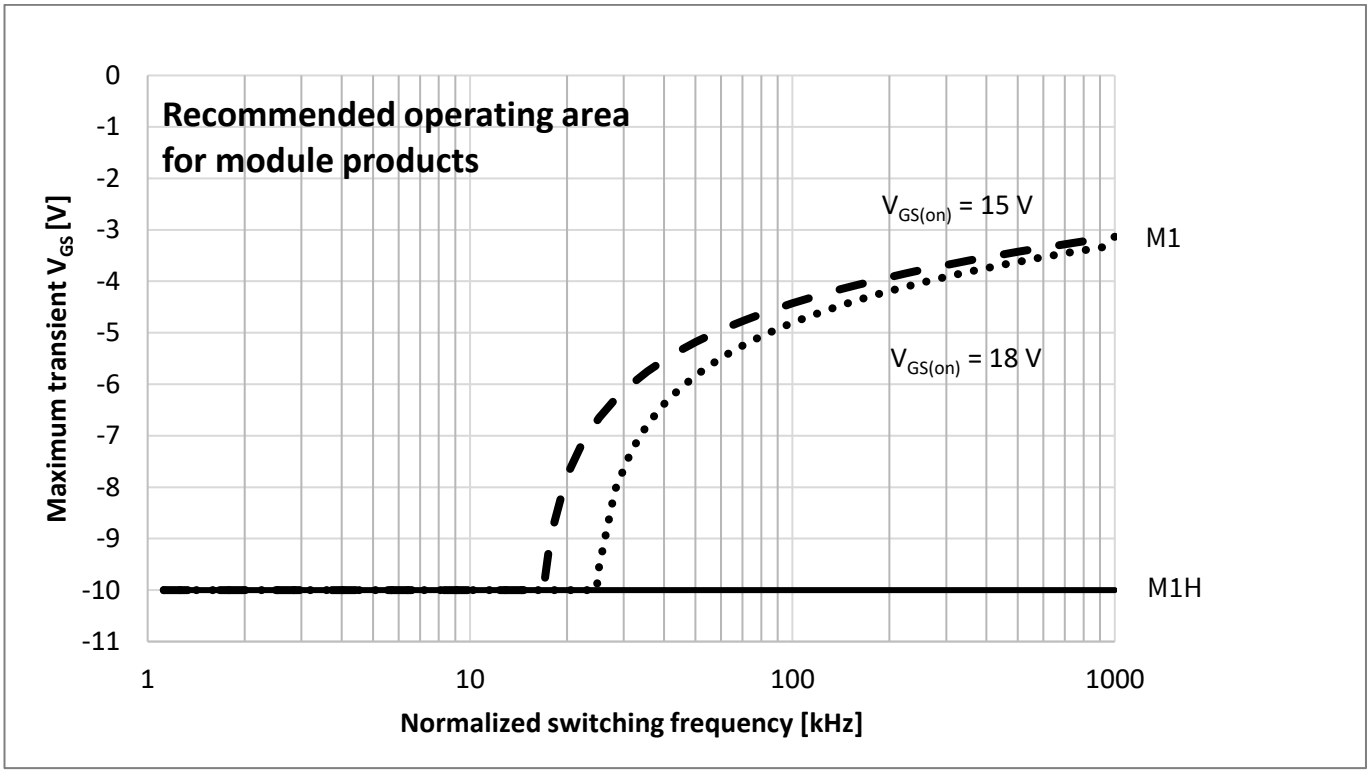

Figure 3 Minimum turn-off gate voltage for 1200 V module products

Details on how to use this information are described in the following example. A solar inverter has:

- An actual switching frequency of 20 kHz
- A targeted lifetime of 20 years
- An operating time of 50%
- A normalized switching frequency of 20 kHz * 20 years * 50%/10 years = 20 kHz

For a turn-on voltage of 18 V, using CoolSiC™ MOSFETs M1 in discrete packages, the turn-off gate voltage including undershoot has to be between -4.6 V and 0 V, as can be seen in Figure 2. For a turn-on voltage of 15 V, using CoolSiC™ MOSFET M1 modules, the turn-off gate voltage including undershoot has to be designed between -7.7 V and 0 V (see Figure 3).

The minimum turn-off voltage, which defines the recommended operating area, is set to ensure that the $R_{DS(on)}$ increase at I_{nom} and T_{vj} = 125°C will not exceed 15% of the initial value during the entire product lifetime.

The relative increase of $R_{DS(on)}$ depends on the operating current, I_d, and junction temperature, T_{vj}, as shown in Figure 4.

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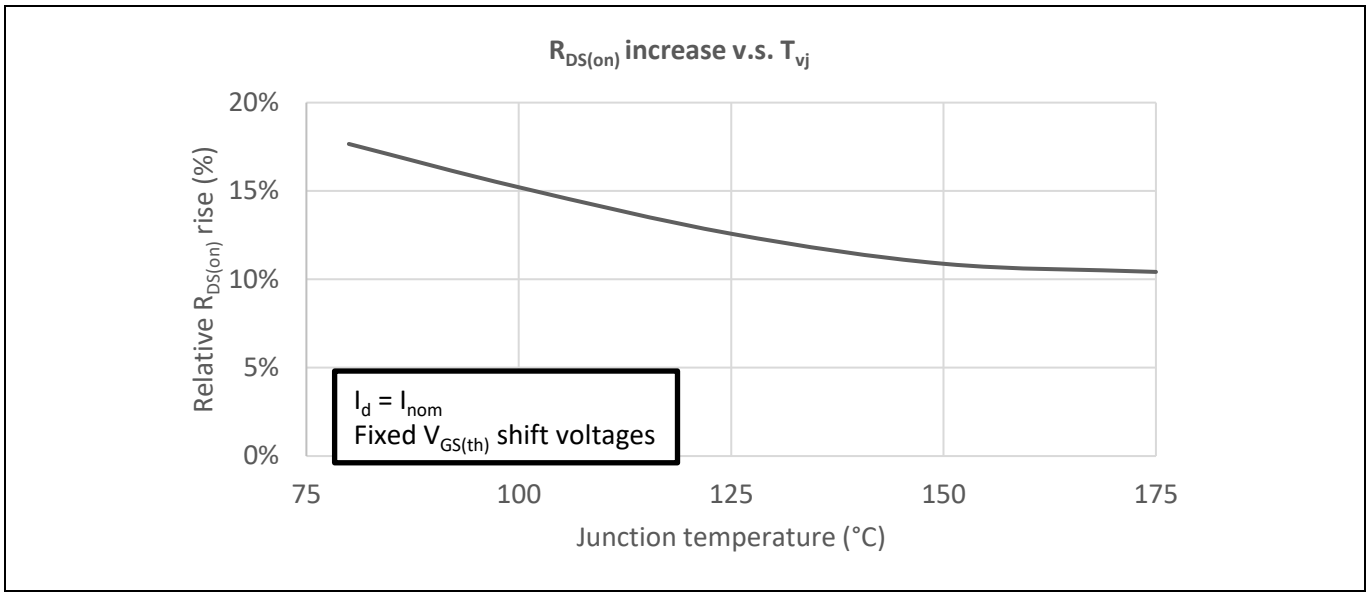

Figure 4 Relative $R_{DS(on)}$ increase at different junction temperatures

Finally, please note that independent of the ROA, the lowest peak gate voltage must never exceed the maximum ratings given in the product datasheet.

3.1.1 Assessment of worst-case $R_{DS(on)}$ drift at the end of the mission profile

Infineon always strives to enhance newer semiconductors generations in regards to their behavior and performance. Technologies like the 1200 V CoolSiC™ MOSFET M1H shows significant improvements with regard to threshold voltage stability. This allows designers to significantly enhance the allowed gate operation window for 1200 V M1H and still stay well below 15% $R_{DS(on)}$ drift.

Extensive tests under various operation conditions were carried out by Infineon to develop a predictive model that describes the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}) [3] [4]. This gives the opportunity to predict the worst-case $R_{DS(on)}$ change accurately for arbitrary mission profiles.

To assess the worst-case, end-of-mission profile (EoMP) $R_{DS(on)}$ drift for individual applications, one needs to consider the total number of switching events until EoMP. This number can be easily calculated from the lifetime target, the total operation time and the switching frequency of the application. With the number of switching cycles (N_{cycles}) the relative change in $R_{DS(on)}$ can be extracted from Figure 5

In Figure 5, the maximum positive and negative dynamic gate-source voltage of the respective data sheets have been considered. Both diagrams represent drift values under worst-case conditions, and are valid as long as the devices do not exceed the limits given in the datasheets of the respective product. The diagrams enable the customers to choose any parameter set inside the datasheet framework that fits their application best, without spending much effort on considering the drift impact, and parasitic overshoots and undershoots in the gate signal.

1200 V CoolSiC™ MOSFET product families have the recommended $V_{GS(on)}$ as follows:

- $V_{GS(on)}$ = 15 V for M1 products
- $V_{GS(on)}$ = 18 V for M1H products (Automotive)
- $V_{GS(on)}$ = 15 to 18 V for M1H products (Industry)
- $V_{GS(on)}$ = 20 V for M1T and Gen1p in D2PAK family (AIMBG120RxxxM1)

Gate drive voltage guidelines

Applications running at well-controlled gate bias levels that are well below the maximum limits given in the datasheet may exhibit even lower $R_{DS(on)}$ drift values for the same number of switching cycles, as shown in Figure 5 [3] [4].

When operating at a less negative turn-off gate voltage (e.g., -2 V instead of -5 V), the impact on the application is slight. Here, several application-relevant parameters should be considered. For example, E_{on} and E_{off} change slightly and the forward voltage of the SiC MOSFET body diode reduces.

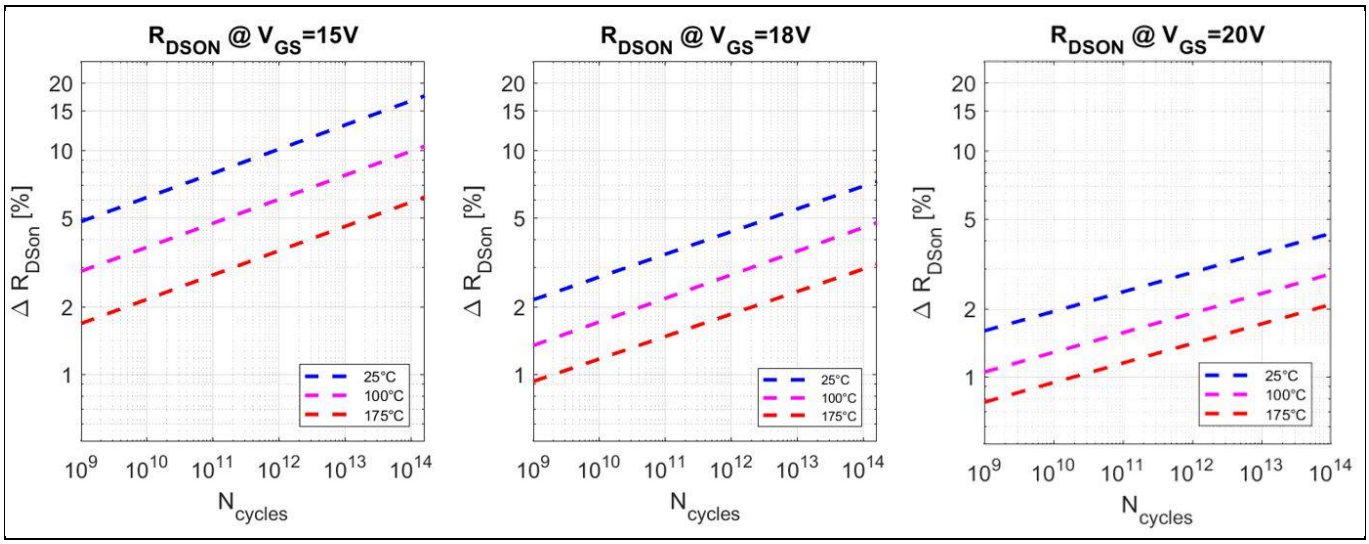

Figure 5 **Left: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 15 V, T_{vjop}= 25°C, 100°C, and 175°C**
Center: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 18 V, T_{vjop}= 25°C, 100°C, and 175°C
Right: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 20 V, T_{vjop}= 25°C, 100°C, and 175°C

The following example explains how to use this information.

- Targeted lifetime [years]: 20
- Real operation time [%]: 50, i.e., 10 years
- Real operating time [s]: 315360000 s (10 years)
- Switching frequency [kHz]: 48
- Cycle duration [s]: 1/switching frequency = 0.0000208
- Number of cycles at end of life: operating time/cycle duration = ~1.52E+13

For a turn-on voltage of 18 V, a ~6% change in $R_{DS(on)}$ at 25°C and ~3% at 175°C can be expected, as shown in Figure 5 on the right.
For a turn-on voltage of 15 V, a ~13% change in $R_{DS(on)}$ at 25°C and ~5% at 175°C can be expected, as shown in Figure 5 on left.

3.2 Guidelines for 650 V devices

The $R_{DS(on)}$ variation caused by switching events with a negative gate voltage turn-off ($V_{GS(off)}$) is more pronounced in 650 V CoolSiC™ MOSFET devices compared to devices with a higher breakdown voltage (e.g., 1200 V CoolSiC™ MOSFET). This is because R_{ch} has a higher contribution to the overall $R_{DS(on)}$. However, the $R_{DS(on)}$ variation can be reduced to a negligible value by operating the device within the gate-source voltage operating range specified in the product datasheet.

3.2.1 Assessment of worst-case $R_{DS(on)}$ drift at the end of the mission profile

To extend the negative driving voltage capability of 650 V CoolSiC™ MOSFET G1, several tests under various operating conditions following the methodology presented in [3] and [4] were carried out to develop a model that enables to assess the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}).

To assess the worst-case end-of-mission profile (EoMP) $R_{DS(on)}$ - drift for individual applications one needs to consider the total number of switching events until EoMP. This number can be easily calculated from the lifetime target, the total operation time and the switching frequency of the application. With the number of switching cycles (N_{cycles}) the relative change in $R_{DS(on)}$ can be extracted from Figure 6.

In Figure 6 the maximum positive and negative dynamic gate-source voltage of the respective datasheets have been considered. The diagram represents drift values under worst-case conditions, and are valid as long as the devices do not exceed the limits given in the datasheet of the respective products. The diagrams enable customers to choose any parameter set inside the datasheet framework that fits their application best, without spending much effort on considering the drift impact, and parasitic overshoots and undershoots in the gate signal.

If the gate-source voltage at the device pins is kept within the limits specified in the operating range of the product datasheet (“Gate-source voltage operating range including undershoots”), the $R_{DS(on)}$ does not exceed the maximum datasheet specification over lifetime.

The recommended on-state driving voltage for 650 V CoolSiC™ MOSFET G1 products is $V_{GS(on)}$=18 V. Products belonging to this family are identified by the following part number structure:

- IMx(x)**65**Ryyy**M1H** (industrial grade)
  Where:
  - x(x) is the package identifier: “W” (TO247-3), “ZA” (TO247-4), “BG” (D2PAK-7), “T” (TOLL)
  - yyy is the typical $R_{DS(on)}$ in mΩ

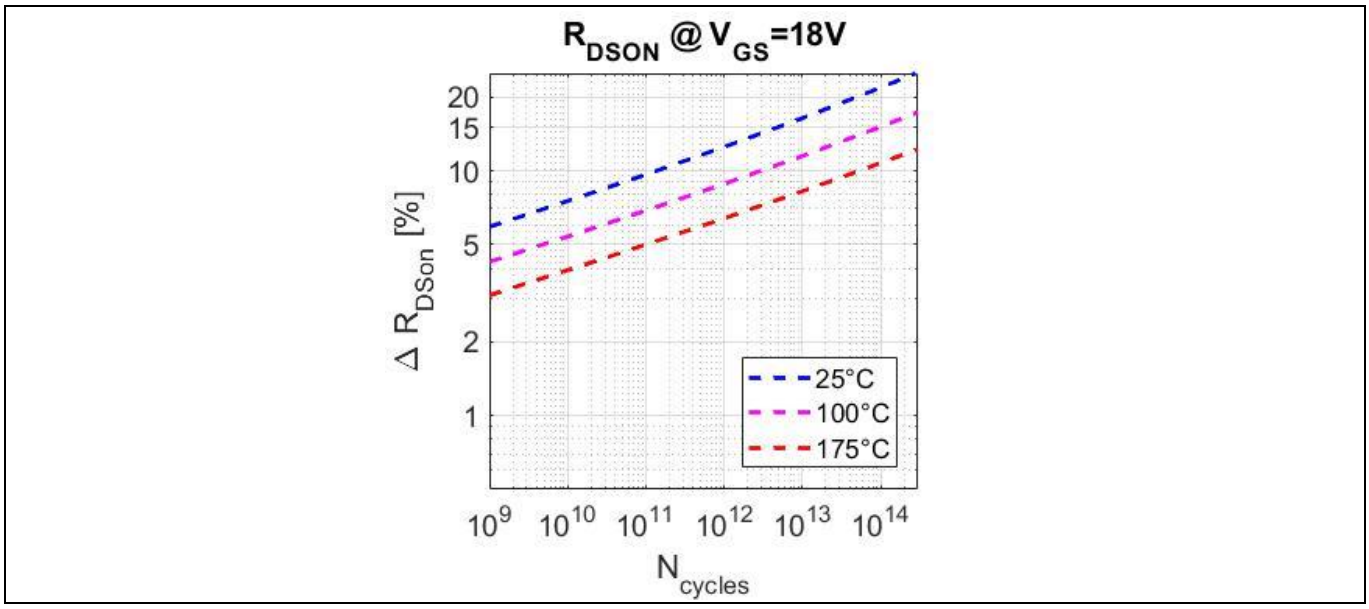

Figure 6 Relative $R_{DS(on)}$change at $V_{GS(on)}$ = 18 V, T_{vjop} = 25°C, 100°C, and 175°C based on extrapolation of intermediate readouts

The following example explains how to use this information:

- Targeted lifetime [years]: 10
- Real operation time [%]: 50 = 5 years
- Real operation time [s]: 1.577E8 (5 years)
- Switching frequency [kHz]: 65
- Cycle duration [s]: 1/switching frequency = 0.0000154
- Number of cycles at end of life: operating time/cycle duration = ~1.025 E+13

For a turn-on voltage of 18 V, a 12% change in $R_{DS(on)}$ at 100°C and 8% at 175°C can be expected, as shown in Figure 6.

3.3 Guidelines for 750 V devices

For In theThe 750 V CoolSiC™ MOSFET G1 technology (available in automotive and industrial grade) exhibits a dependency of $R_{DS(on)}$ on the threshold voltage, $V_{GS(th)}$, in between the ones shown by the 650 V and 1200 V rated devices, resulting in an $R_{DS(on)}$ drift substantially lower than that of the 650 V technology, but slightly higher than that of 1200 V. This is because for the 750 V technology the contribution of channel resistance, R_{ch}, to the overall $R_{DS(on)}$ is lower than that for 650 V, but higher compared to 1200 V.

3.3.1 Assessment of worst-case $R_{DS(on)}$ drift at the end of the mission profile

Similar to 1200 V and 2 kV technologies, extensive tests were also performed by Infineon for the 750 V technology under various operating conditions to develop a predictive model that describes the change in $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}) [3] [4]. This helps predict the worst-case $R_{DS(on)}$ change accurately for any mission profile.

To assess the worst-case, end-of-mission profile (EoMP) $R_{DS(on)}$ drift for individual applications, the total number of switching events until EoMP need to be considered. This number can be easily calculated using the lifetime target, the total operating time, and the switching frequency of the application. Based on the number of switching cycles (N_{cycles}), the relative change in $R_{DS(on)}$ can be seen in Figure 7.

Gate drive voltage guidelines

In Figure 7, the maximum positive and negative dynamic gate-source voltage given in the respective product datasheets have been considered. The diagrams show drift values under worst-case conditions, and are valid as long as the devices do not exceed the limits given in the datasheets. With the help of these diagrams, customers can choose any parameter set inside the datasheet framework that fits their application best without spending much effort on considering the drift impact, and parasitic overshoots and undershoots in the gate signal.

If the gate-source voltage at the device pins is kept within the limits specified in the operating range of the product datasheet ("Gate-source voltage operating range including undershoots"), the $R_{DS(on)}$ does not exceed the maximum datasheet specification over lifetime.

The recommended on-state driving voltage for 750 V CoolSiC™ MOSFET G1 products is $V_{GS(on)}$ = 18 V. Products belonging to this family can be identified using the following part number structure:

- AIMxx**75**yyy**M1H** (automotive grade)
- IMxx**75**Ryyy**M1H** (industrial grade)

  Where:
  - xx is the package identifier: "BG" (D2PAK-7), "DQ" (QDPAK TSC), "ZA" (TO247-4)
  - yyy is the typical $R_{DS(on)}$ in mΩ

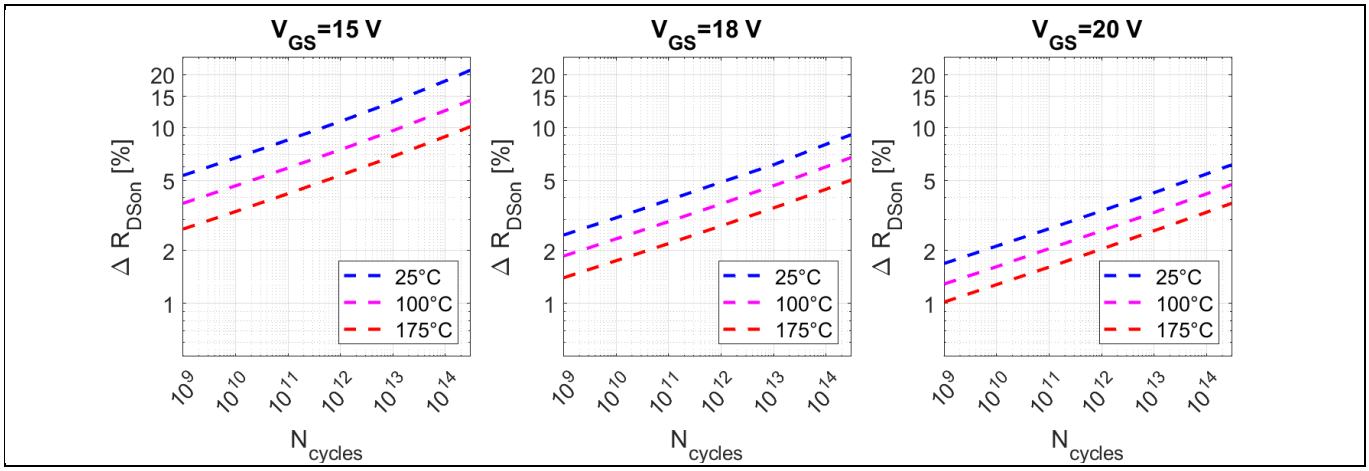

Figure 7 **Left: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 15 V, $T_{j,op}$ = 25°C, 100°C, and 175°C**
Center: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 18 V, $T_{j,op}$ = 25°C, 100°C, and 175°C
Right: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 20 V, $T_{j,op}$ = 25°C, 100°C, and 175°C

The following example explains how to use this information:

- Targeted lifetime [years]: 20
- Real operation time [%]: 50 = 10 years
- Real operation time [s]: 315360000 s (10 years)
- Switching frequency [kHz]: 48
- Cycle duration [s]: 1/switching frequency = 0.0000208
- Number of cycles at end of life: operating time/cycle duration = ~1.52E+13

For a turn-on voltage of 15 V, a ~15% change in $R_{DS(on)}$ at 25°C and ~7% at 175°C can be expected as shown in Figure 7 on the left.

Gate drive voltage guidelines

For a turn-on voltage of 18 V, a ~7% change in $R_{DS(on)}$ at 25°C and ~4% at 175°C can be expected, as shown in Figure 7 in the center diagram.

For a turn-on voltage of 20 V, a ~5% change in $R_{DS(on)}$ at 25°C and ~3% at 175°C can be expected, as shown in Figure 7 on the right.

3.4 Guidelines for 2000 V devices

Compared to 650 V, 750 V, and 1200 V rated devices, the 2 kV SiC MOSFET technology shows a lower dependency of $R_{DS(on)}$ on the threshold voltage, leading to lower $R_{DS(on)}$-drifts. As mentioned during the description of the phenomenon, an increase in threshold voltage, $V_{GS(th)}$, causes a slight increase in the channel resistance, $R_{ch.}$, followed by the $R_{DS(on)}$. However, for higher voltage devices the $R_{DS(on)}$ is more dominated by EPI resistance due to the thicker EPI layer, and is less influenced by the channel resistance.

As for all voltage classes, the M1H base technology comes with an improved gate oxide and shows a significant improvement with regard to bipolar AC stress, also referred to as gate switching instability (GSI). With 2 kV CoolSiC™ MOSFET M1H, Infineon provides great stability and diminishes the impact of the drift phenomenon, providing complete freedom to choose negative gate-source voltage, and allowing to go down to -10 V while still ensuring safe operation.

3.4.1 Assessment of worst-case $R_{DS(on)}$ drift at the end of the mission profile

Following the approach and boundary conditions of 1200 V devices, for the 2 kV technology too Infineon has carried out extensive tests to develop a predictive model that describes the change of $R_{DS(on)}$ as a function of the number of cycles (N_{cycles}), as shown in Figure 8.

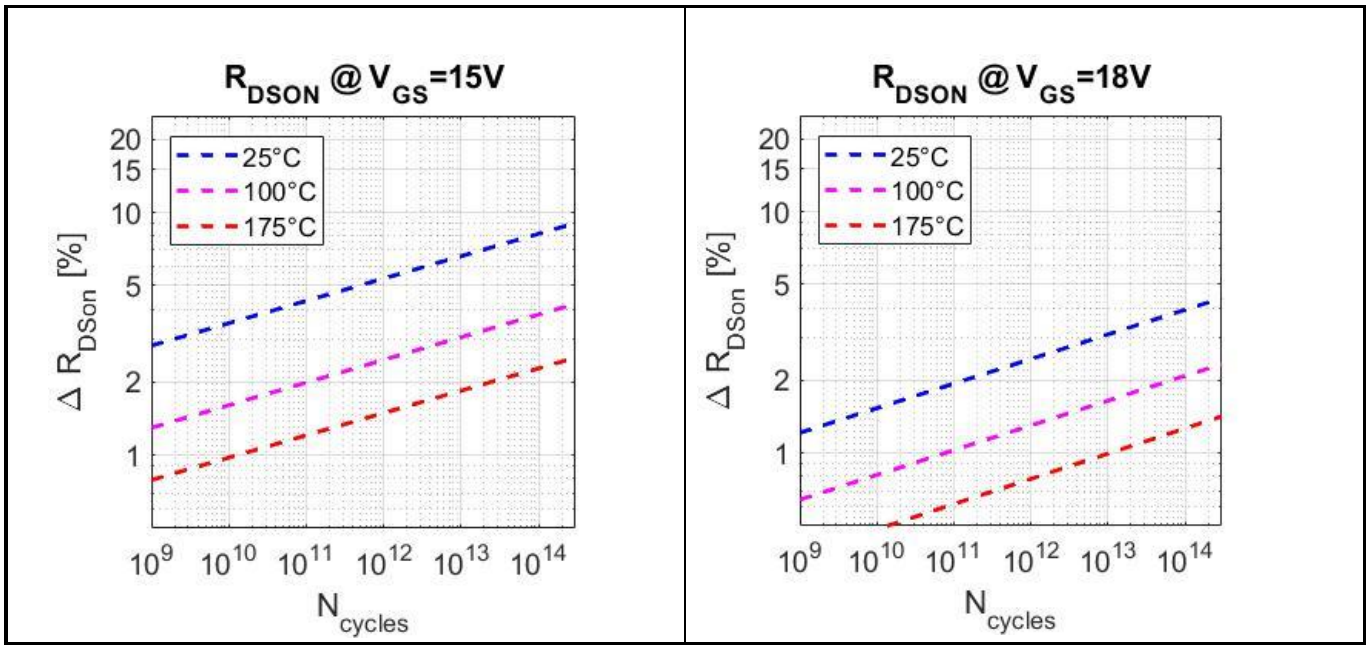

Figure 8 Left: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 15 V, T_{vjop} = 25°C, 100°C, and 175°C
Right: Relative $R_{DS(on)}$ change at $V_{GS(on)}$ = 18 V, T_{vjop} = 25°C, 100°C, and 175°C

How to use this information is explained in the following example:

- Targeted lifetime [years]: 20
- Real operating time [%]: 50 = 10 years
- Real operating time [s]: 315360000 s (10 years)
- Switching frequency [kHz]: 48
- Cycle duration [s]: 1/switching frequency = 0.0000208
- Number of cycles at end of life: operating time/cycle duration = ~1.52E+13

For a turn-on voltage of 15 V, a ~7% change in $R_{DS(on)}$ at 25°C and ~2% at 175°C can be expected (see Figure 8 on left).

For a turn-on voltage of 18 V, a ~3% change in $R_{DS(on)}$ at 25°C and ~1% at 175°C can be expected, as shown in Figure 8 on the right.

3.5 Definition of gate-voltage overshoot and undershoot

The $V_{GS(th)}$ drift is a long-term effect, therefore only repetitive overshoots and undershoots should be considered. An overshoot or undershoot of the gate voltage caused by non-standard operating conditions (e.g., power-grid instability, short-circuit conditions, etc.) should not be considered.

Overshoot and undershoot are only critical for $V_{GS(th)}$ drift if the spikes reach the gate- source terminals directly at the chip. To quantify them experimentally, overshoots and undershoots would ideally be measured directly at chip terminals. However, as this is not always possible, the following guidelines provide a good estimation:

- If isolation is not required, use a direct probe with high bandwidth (100 MHz)
- If isolation is required, use a differential probe with high bandwidth and high common-mode rejection capability
- Always try to measure as close to the chip as possible, as shown in Figure 9

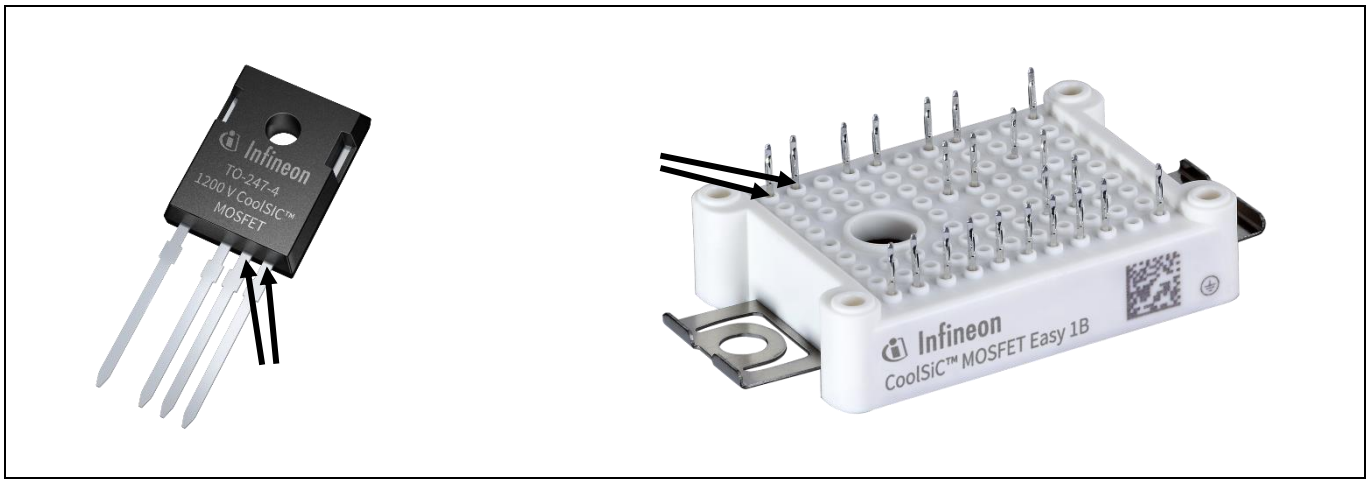

Figure 9 Example of gate voltage measurement points

The shape of the gate voltage overshoot and undershoot may vary between individual inverter designs. The peak voltage should be considered, as shown in Figure 10.

Gate drive voltage guidelines

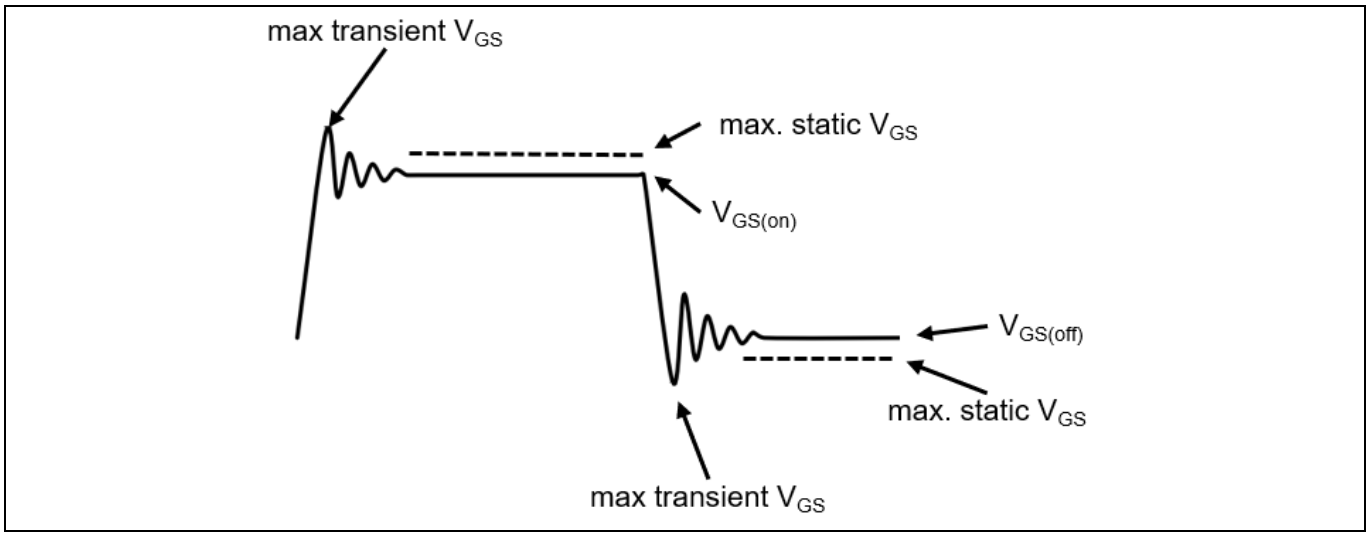

Figure 10 Gate voltage overshoot and undershoot

4 References

[1] T. Aichinger, G. Rescher, G. Pobegen, “Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs,” Microelectronics Reliability 80, 2018, pp. 68–78.

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[3] P. Salmen, M. W. Feil, K. Waschneck, H. Reisinger, G. Rescher, T. Aichinger, “A new test procedure to realistically estimate end-of-life electrical parameter stability of SiC MOSFETs in switching operation,” 2021 IEEE International Reliability Physics Symposium (IRPS), 2021.

[4] P. Salmen, M. W. Feil, K. Waschneck, H. Reisinger, G. Rescher, I. Voss, M. Sievers, T. Aichinger, “Gate-switching-stress test: Electrical parameter stability of SiC MOSFETs in switching operation”, Microelectronics Reliability, 2022.

Revision history

Document version	Date of release	Description of changes
1.0	2018-05-28	Initial version
1.1	2019-05-06	Included the undershoot/overshoot in the ROA, and modified corresponding wording
1.2	2022-03-04	Extended $V_{GS(th)}$ drift phenomenon explanation Included end-of-life assessment for 1200 V M1H Included end-of-life assessment for 650 V M1H Updated gate overshoots and undershoot waveforms in Section 3.3 – Extended references
1.3	2023-05-04	Included guidelines for 2000 V M1H (industrial) and M1H and M1T (automotive) Reference to the new GSS test
1.4	2023-11-17	Included guidelines for 750 V M1H (automotive and industrial) Updated 650 V M1H product list, corresponding wording and example

Revision history

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Email: erratum@infineon.com

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