Getting started with EiceDRIVER™ APD 2ED4820-EM

About this document

Scope and purpose

This document describes how to get started with the 48 V smart high-side MOSFET gate driver with SPI: EiceDRIVER™ APD 2ED4820-EM.

Intended audience

Hardware enginers who have to build the schematic & layout integrating EiceDRIVER™ APD 2ED4820-EM.

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1 Introduction to EiceDRIVER™ APD 2ED4820-EM

EiceDRIVER™ APD 2ED4820-EM is a gate driver designed for high current 48 V automotive applications, with powerful gate outputs to drive many MOSFETs in parallel in order to minimize the conduction losses. It supports the back-to-back configuration, both common source and common drain structures, thanks to its two gate outputs.

In common source configuration, one gate output can be used to pre-charge loads with high input capacitance. EiceDRIVER™ APD 2ED4820-EM generates the supply for the gate outputs based on an integrated one-stage charge pump with external pump and tank capacitors.

EiceDRIVER™ APD 2ED4820-EM comes with an SPI interface, for easy configuration, diagnosis and control.

Several protection mechanisms are provided:

- Supply under and overvoltage detection with configurable restart timer
- Charge pump undervoltage detection
- Gate to source undervoltage detection with immediate lock-out to prevent linear mode conduction of the MOSFETs
- Configurable drain to source overvoltage detection, which can also be deactivated
- Configurable overcurrent protection based on an analog current sense amplifier compatible for high-side or low-side shunt topologies
- Internal overtemperature warning and protection

An interrupt pin informs the MCU whenever one of these protections is triggered. Status registers can then be read by the MCU to understand what was the trigger for the notification.
The output of the current sense amplifier can be monitored by the MCU to implement additional protections, such as wire overtemperature.
In addition, EiceDRIVER™ APD 2ED4820-EM enables to implement an open load detection mechanism, checking the source voltage of the MOSFETs with respect to ground in the OFF state.

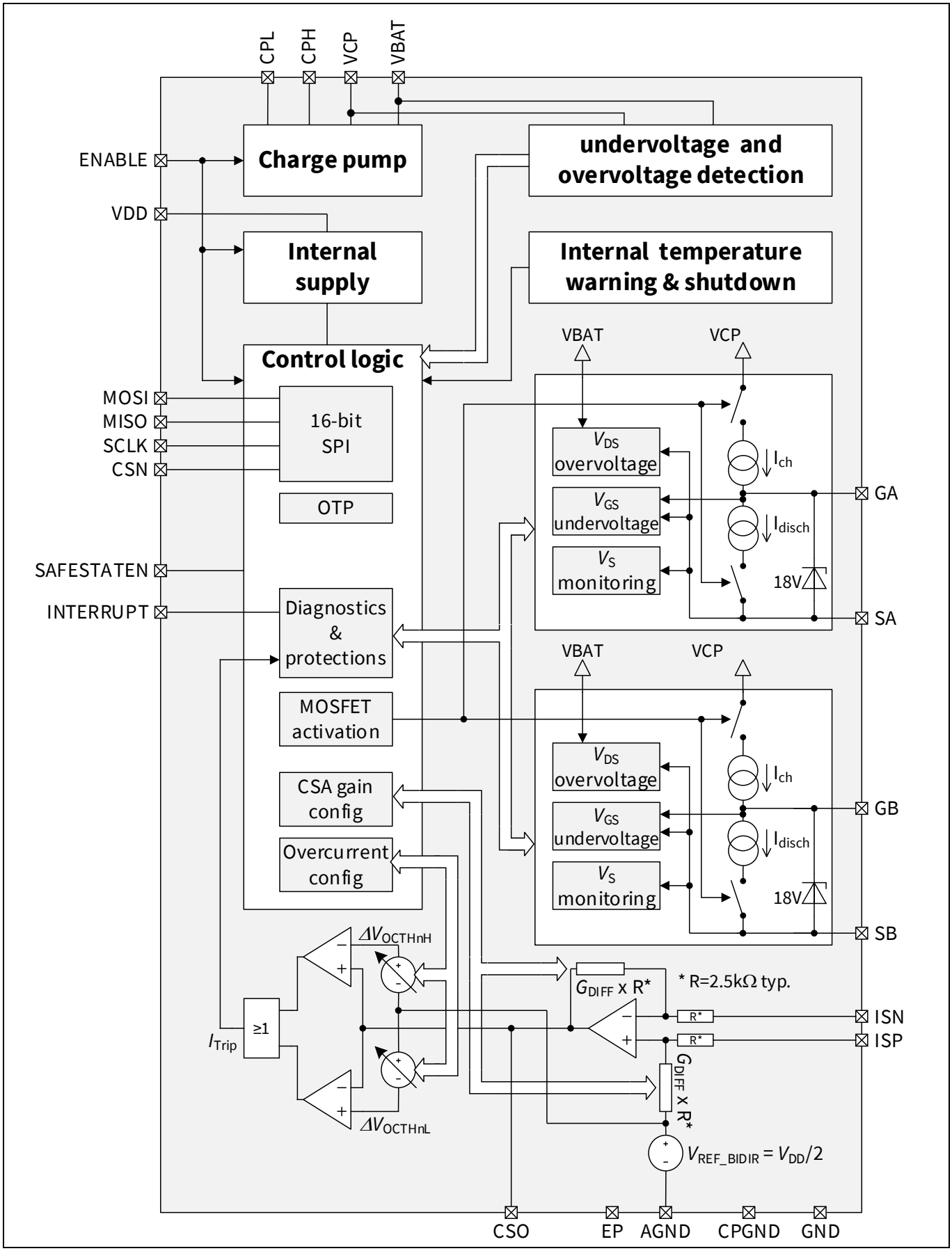

Figure 1 2ED4820-EM internal block diagram

2 Set of values to easily get started with 2ED4820-EM

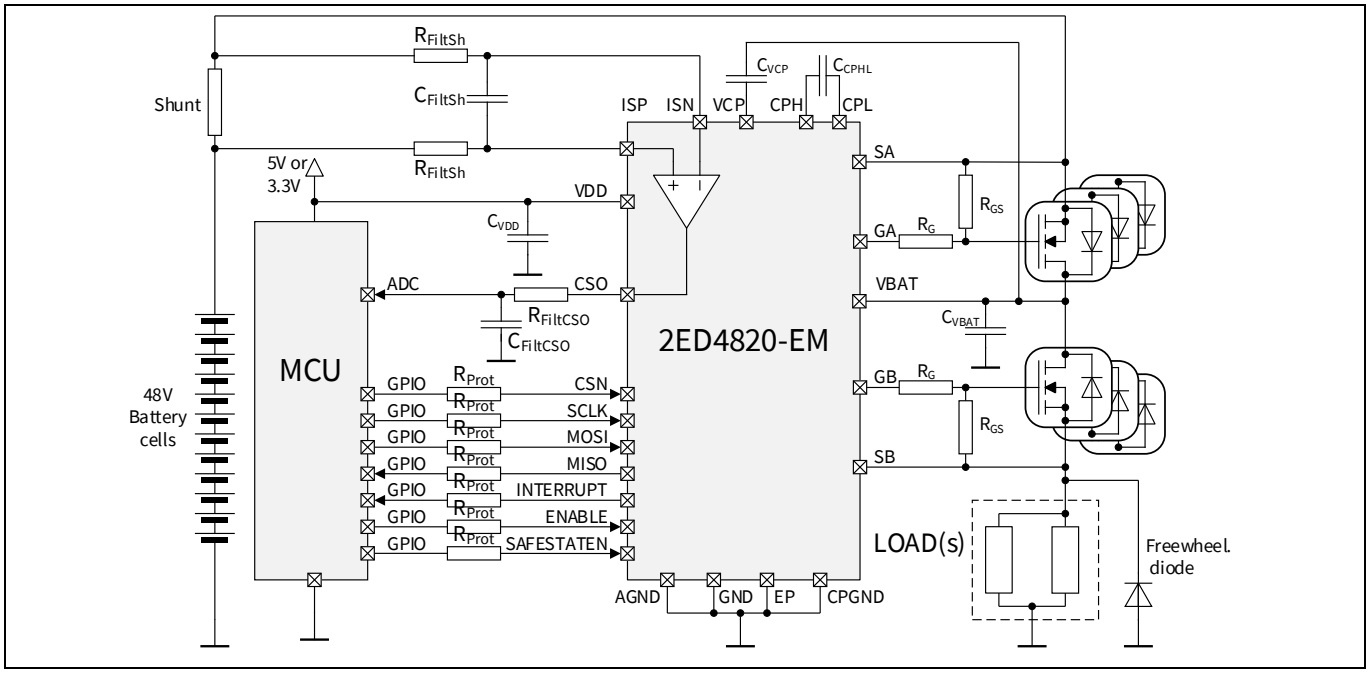

Figure 2 Reference schematic

Table 1 Set of values for the external components to easily get started

Ref.	Value	Purpose	Rationale for the value
R_{Prot}	1.0 kΩ	Protection of the microcontroller	
C_{VDD}	1.0 µF	Supply decoupling; on layout, located close to the VDD & GND pins	Fixed value
C_{VBAT}	4.7 µF + 22 nF	Supply decoupling; on layout, located close to the VBAT & AGND pins	Small value (22 nF) added for EMC optimization To be checked on system level
C_{VCP}	2.2 µF	Charge pump output capacitor	Ensure $10\ \mu F \geq C_{VCP} \geq [1.2 \times NbrMOS \times Q_g]$ where NbrMOS is the number of MOSFETs to switch ON simultaneously
C_{CPHL}	220 nF	Charge pump capacitor	Fixed value
R_G	10.0 Ω	Gate protection resistor	Ensure $[R_G \times NbrMOS \times C_{iss}] \geq 1\ \mu s$
R_{GS}	150.0 kΩ	Gate to source pull-down resistor	$R_{GS} \geq 2.8\ k\Omega$ to keep $I_{GS} \leq 5\ mA$ and avoid overloading the charge pump
$R_{FiltCSO}$	10.0 kΩ	Protection of the microcontroller and Low pass filter on current sense output	
$C_{FiltCSO}$	100 nF	Low pass filter on current sense output	Size $C_{FiltCSO}$ to have the proper bandwidth with $R_{FiltCSO}$
R_{FiltSh}	4.7 Ω	Filter to cancel the inductive part of the shunt	$R_{FilSh} \leq 20\Omega$ to limit the effect on CSA gain accuracy below 1%
C_{FiltSh}	1 µF	Filter to cancel the inductive part of the shunt	$C_{FiltSh} = \frac{L_{Shunt}}{2 \times R_{FiltSh} \times R_{Shunt}}$ where LShunt is the parasitic inductance of the shunt.

3 What to do with unused pins?

3.1 Unused gate driver outputs

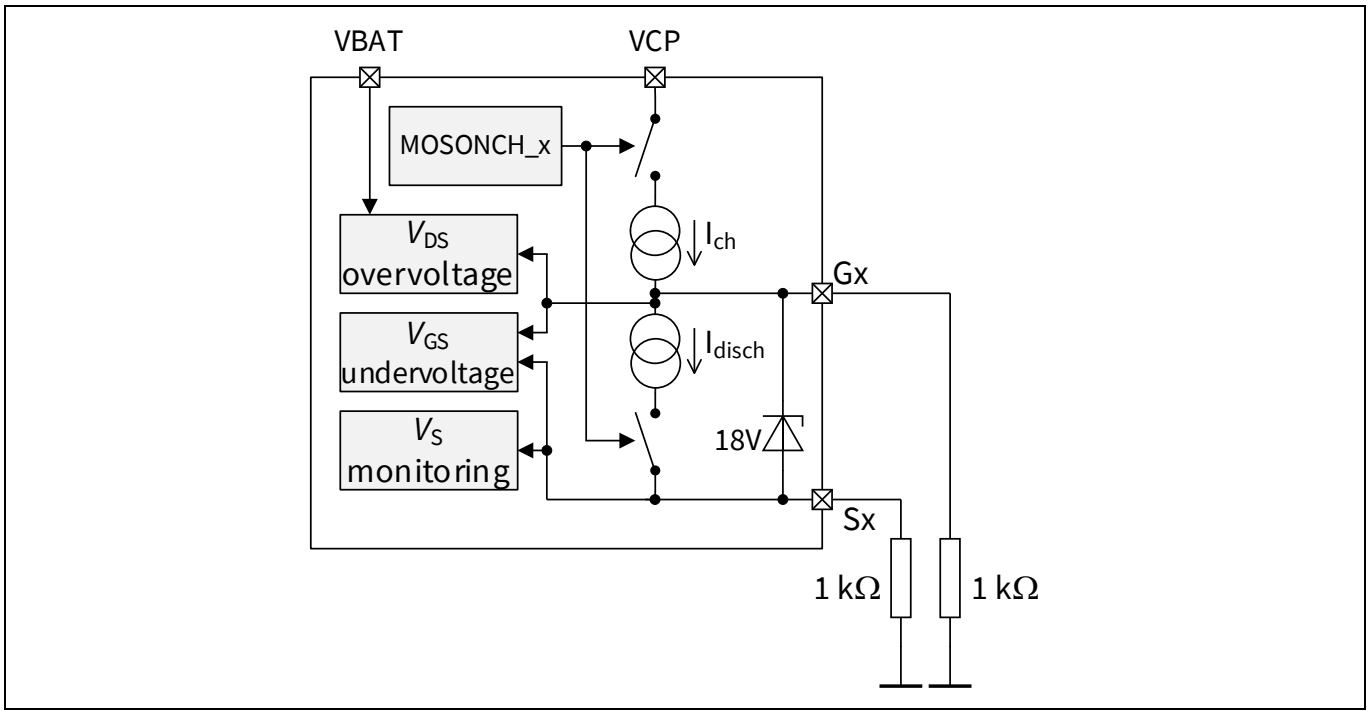

Figure 3 Recommanded connection when 1 channel gate driver is unused in the application

3.2 Unused current sense amplifier

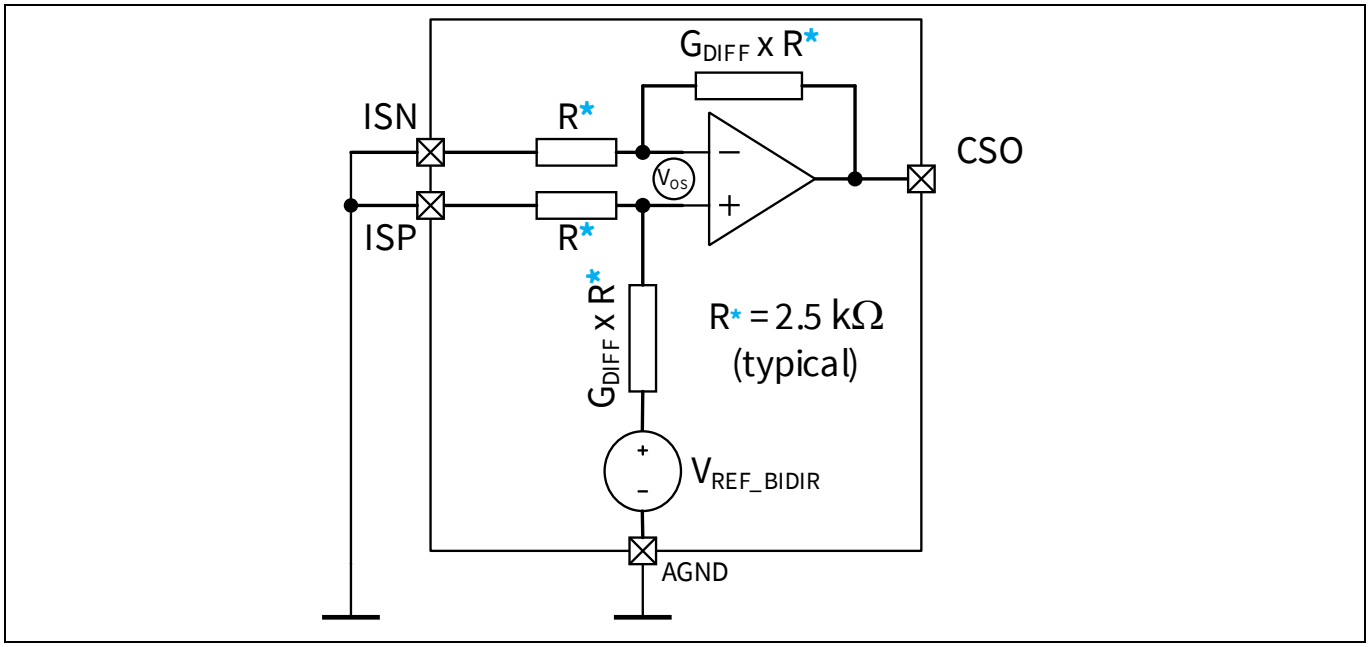

Figure 4 Recommanded connection when the current sense amplifier is unused in the application

In addition to connecting ISP and ISN pins to ground, it is recommended to set $G_{DIFF} = 47.7$ so that the remaining biasing current on ISP and ISN is reduced to a minimum value (the Current sense amplifier cannot be disabled when ENABLE is set high, so it still contributes to the current drawn on VBAT, even if it not used).

4 PCB layout recommandations

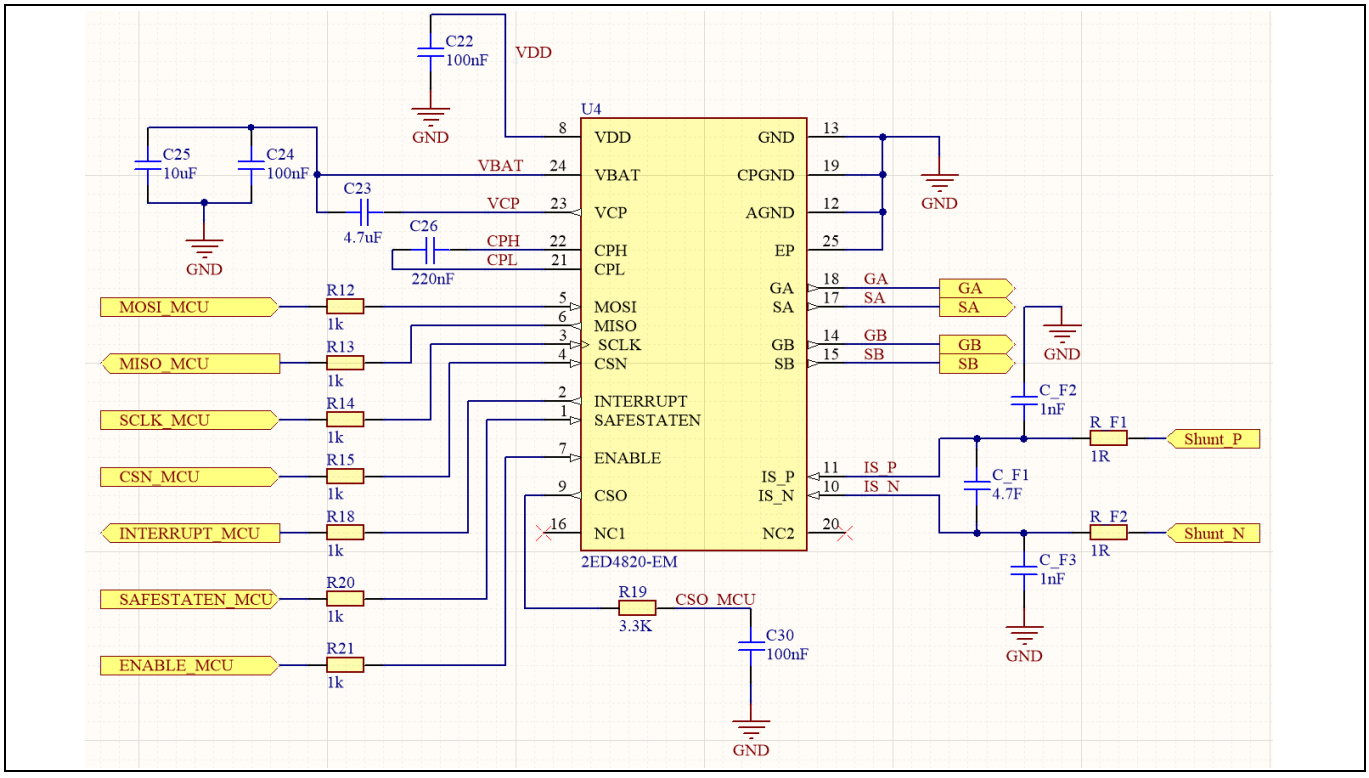

Figure 5 Reference schematic for components identification on the recommended layout.

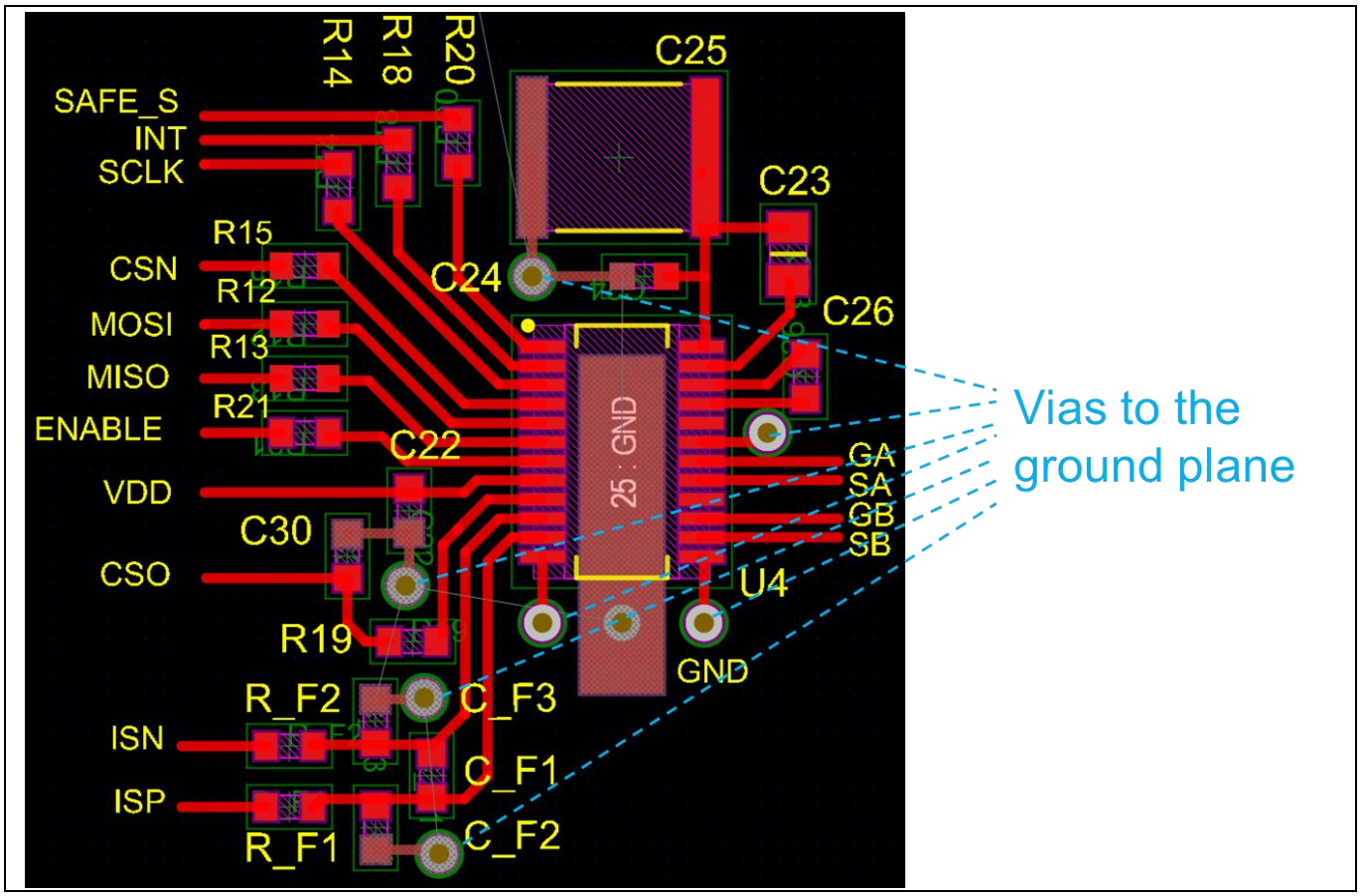

Figure 6 Recommanded layout.

PCB layout recommandations

Table 2 Cross reference between application diagram and schematic

Ref. on diagram	Component ID on schematic	Recommandation
R_{Prot}	R12, R13, R14, R15, R18, R20, R21	
C_{VDD}	C22	Position very close to VDD pin
C_{VBAT}	C24, C25	Position the low value (C24) very close to VBAT pin, high value (C25) close to C24.
C_{VCP}	C23	Position very close to VCP and VBAT pins
C_{CPHL}	C26	Position very close to CPH and CPL pins
$R_{FiltCSO}$	R_F2, R_F1	Position in a very symmetrical structure together with C_F1; use same wire length & parallel tracks to connect to ISP and ISN pins and to the shunt kelvin contacts
$C_{FiltCSO}$	C_F1	See R_F2 & R_F1
R_{FiltSh}	R19	
C_{FiltSh}	C30	

5 Detailed analysis for protections resistors of the SPI interface

It is highly recommended to insert a protection resistor (R_{PROT}) between the digital IOs of 2ED4820-EM and the pins of the driving circuit (microcontroller in general). The purpose is to limit the current in case this driving circuit is exposed to a high voltage available on 2ED4820-EM (VBAT, VCP, CPL, CPH, GA, GB, SA, SB, optionally ISN & ISP). This may happen in case of a short-circuit created between one of these pins or corresponding signal lines and a digital IO of the driving circuit.

To size this resistor, 2 parameters have to be considered:

1. The track length on the PCB between the driving circuit and 2ED4820-EM
2. The operating frequency of the SPI interface.

The track length will translate into a parasitic capacitance (C_{TRACK})to the ground plane. Together with the protection resistor (R_{PROT}), this parasitic capacitor forms a low pass filter, with a time constant: R_{PROT} x C_{TRACK}. This low pass filter slows down the rise & fall edges of the SPI signals: MOSI, MISO, SCLK and CSN.

The recommendation is to keep this time constant below 3 % of the SPI clock period:

$$R_{PROT} \times C_{TRACK} \leq 0.03 \times \frac{1}{f_{SPI}}$$

$$R_{PROT} \leq 0.03 \times \frac{1}{C_{TRACK} \times f_{SPI}}$$

The rule of thumb to estimate the parasitic capacitance of the track is to use 1 pF per centimeter.

Table 3 gives a set of values for the protection resistor (R_{PROT}) as a function of the SPI clock and the parasitic capacitor of the signal track:

Table 3 Recommended values for the protection resistor depending on the SPI clock & track length

f_{SPI}	≤ 10 cm (≤ 10 pF)	≤ 20 cm (≤ 20 pF)	≤ 30 cm (≤ 30 pF)
5Mhz	600 Ω	300 Ω	200 Ω
2.5Mhz	1.2 kΩ	600 Ω	300 Ω
1Mhz	3.0 kΩ	1.5 kΩ	1.0 kΩ
0.5Mhz	6.0 kΩ	3.0 kΩ	2.0 kΩ

6 Detailed analysis for the Charge Pump external components

6.1 Charge pump concept

The charge pump is a 1-stage capacitive DC-DC voltage converter, generating an output voltage (V_{CP}) 14 V above the supply voltage (V_{BAT}).

Table 4 Typical values for key parameters extracted from table 7 in the datasheet

Parameter	Symbol	Typ. value	Unit
Charge pump frequency	f_{CP}	156	kHz
VCP_PUMP_H threshold	$V_{VCP\_PUMP\_H}$	14	V
VCP_PUMP_L threshold	$V_{VCP\_PUMP\_L}$	13	V
CPL pulsed current	$\lvert I_{CPL\_PULSE} \rvert$	80	mA

A pump capacitor (C_{CPHL}) is used to charge a tank capacitor (C_{VCP}). As shown below, the pump phase is split into 2 steps, with a timing derived from a dedicated reference clock, called f_{CP}:

1. C_{CPHL} is charged from VBAT during half of f_{CP} period (3.2 µs) by a low-side current source of I_{CPL_PULSE}=80 mA typ.
2. The charge previously stored in C_{CPHL} is transferred to C_{VCP} during the other half of f_{CP} period (3.2µs) by activating a high side current source of I_{CPL_PULSE}=80 mA typ.

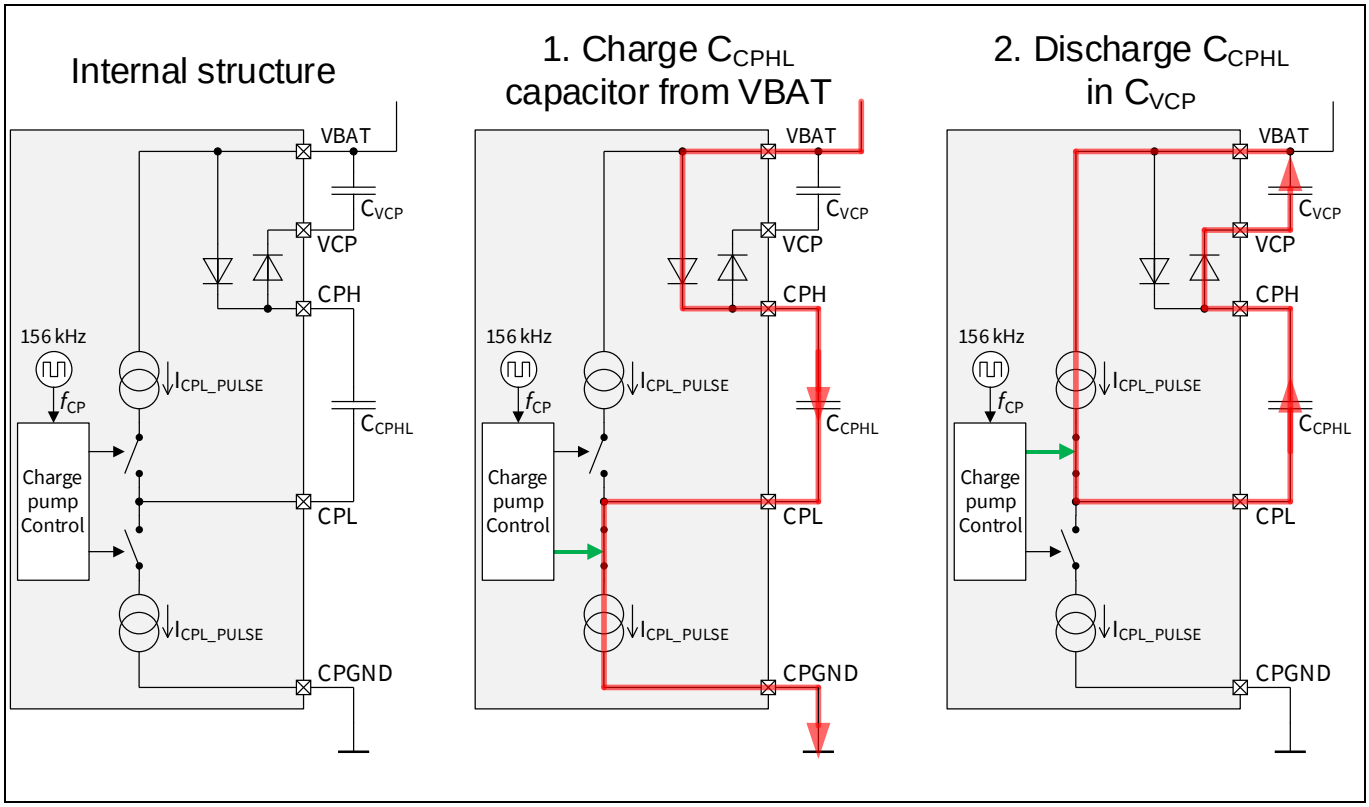

Figure 7 Charge pump internal structure and description of the 2-step pump phase.

6.2 Before the activation of the charge pump

While the **ENABLE** pin is maintained to logical '0', C_{VCP} is discharged and V_{CP} voltage is very close to V_{BAT} voltage due to the 2 internal diodes between **VBAT** and **VCP** pins.

6.3 Activation of the charge pump

When the **ENABLE** pin is set to logical '1', the charge pump starts a long pump phase, alternating between the 2 steps described above at f_{CP} frequency. When V_{CP} reaches the $V_{CP\_PUMP\_H}$ threshold, the pump phase is stopped.

6.4 Regulating the charge pump output voltage

When the pump phase is stopped, the voltage on V_{CP} decreases until it reaches the $V_{CP\_PUMP\_L}$ threshold. This is the discharge phase, where C_{VCP} discharges due to the current consumed internally in 2ED4820-EM plus optional current drawn by external circuitries also supplied by the charge pump.

A new pump phase is then triggered, to move the V_{CP} voltage back above the $V_{CP\_PUMP\_H}$ threshold, followed by a discharge phase until the $V_{CP\_PUMP\_L}$ threshold. The output voltage is therefore alternating between the 2 thresholds $V_{CP\_PUMP\_H}$ and $V_{CP\_PUMP\_L}$ with a sawtooth waveform, until the 2ED4820-EM is put in sleep mode by setting the **ENABLE** pin to logical '0'.

The resulting sawtooth frequency depends on the value of the C_{VCP} and C_{CPHL} and on the current drawn on the charge pump: the higher this current, the shorter the discharge phase so the higher the sawtooth frequency.

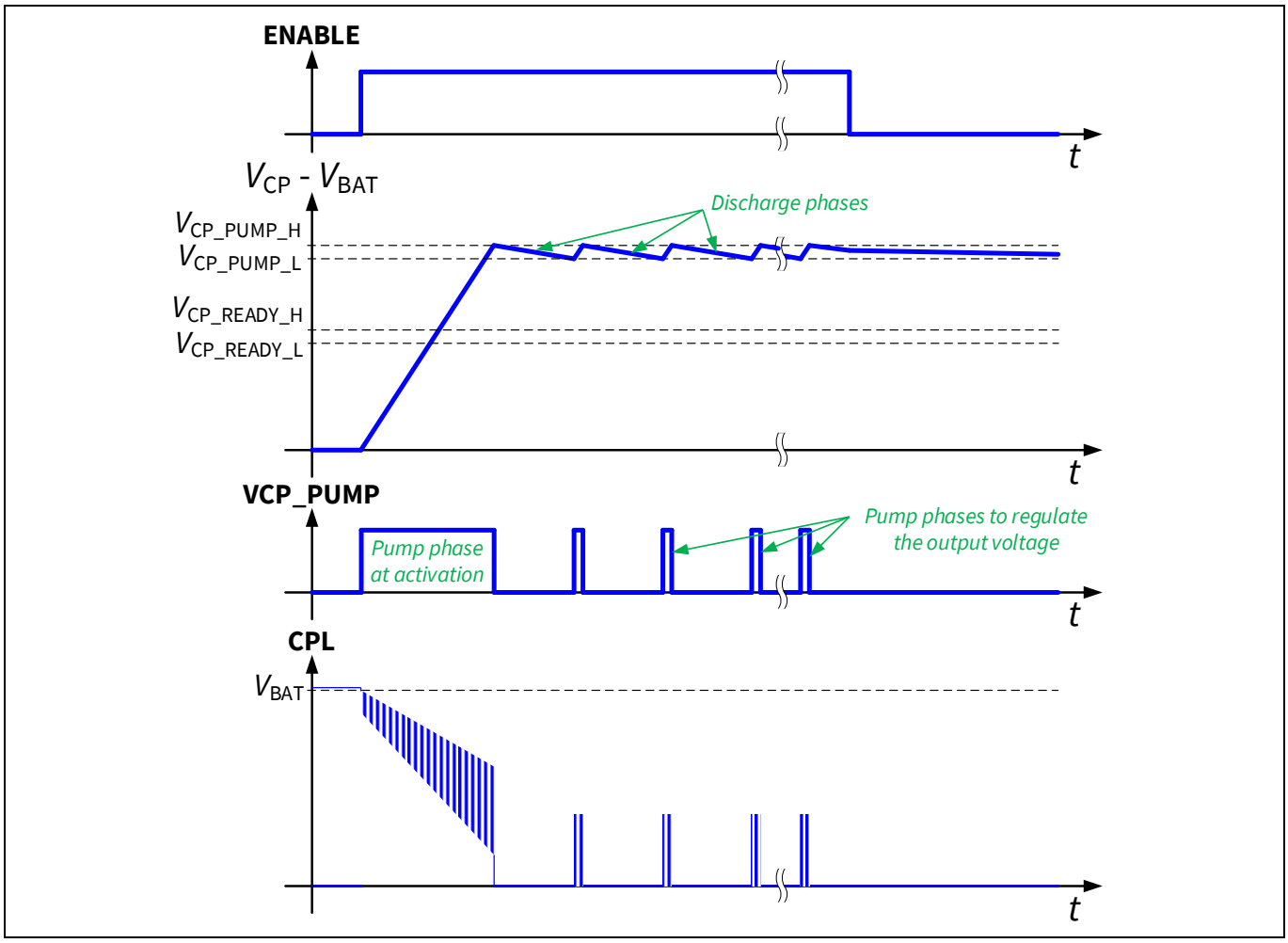

Figure 8 Charge pump activation and regulation.

6.5 Sizing C_{CPHL}

C_{CPHL} is charged during half of f_{CP} period (t_{charge_Ccphl} = 3.2 µs) by a low-side current source of I_{CPL_PULSE} = 80 mA typ.

The voltage variation across C_{CPHL} has to be small compared to $V_{CP\_PUMP\_H}$ to reduce the switching losses in the low-side current source. Assuming a voltage increase of ΔV_{Charge_Ccphl} = 1V, the value for C_{CPHL} is calculated using the well-known charge formula: $C \times \Delta V = i \times \Delta t$

$$C_{CPHL} \times \Delta V_{Charge\_Ccphl} = I_{CPL\_PULSE} \times t_{Charge\_Ccphl}$$

$$C_{CPHL} = \frac{I_{CPL\_PULSE} \times t_{Charge\_Ccphl}}{\Delta V_{Charge\_Ccphl}} = \frac{0.08 \times 3.2 * 10^{-6}}{1} = 256\ nF$$

The recommended value is therefore: **C_{CPHL} = 220 nF** (the resulting ΔV_{Charge_Ccphl} is 1.16 V).

6.6 Sizing C_{VCP}

6.6.1 Minimum value defined by the MOSFETs charge at turn ON

As specified in the datasheet, the current used to turn ON the MOSFETs is I_{CHARGE} = 300mA (typ.).
I_{CHARGE} exceeds by far the current capability of the pump phase which is 40mA typ. (C_{VCP} is charged by I_{CPL_PULSE} only half of the time). C_{VCP} has therefore to be sized so that it can store sufficient charge to turn ON the MOSFETs with a reduced voltage drop, for which the proposed target is $\Delta V_{Discharge\_Cvcp}$ = 1V.
The maximum charge consumed on C_{VCP} is then: $Q_{VCP} = C_{VCP} \times \Delta V_{Didscharge\_Cvcp}$.

On the MOSFETs side, the charge to turn ON is given in the datasheets: it is called Qg.

Qg is unfortunately specified for a full V_{GS} of 10V, while 2ED4820-EM is applying a V_{GS} of:
$V_{CP\_Avg} = [V_{CP\_PUMP\_H} + V_{CP\_PUMP\_L}]/2$ = **13.5V** typ.

It is necessary to add the resulting additional charge: $Qg\_add = C_{iss} \times [\ V_{CP\_Avg} - 10\ ] = C_{iss} \times 3.5$.

The charge for one single MOSFET with V_{GS} from 0V to V_{CP_Avg} is therefore: $Q_{1xMOS} = Qg + Qg\_add = Qg + C_{iss} \times 3.5$.

Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=100 A, V_{GS}=0 to 10 V	-	56	73	nC
Gate to drain charge	Q_{gd}		-	37	56	
Gate charge total	Q_g		-	178	231	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	12500	16250	pF
Output capacitance	C_{oss}		-	2000	2600	
Reverse transfer capacitance	C_{rss}		-	86	130	

Figure 9 Extract from the datasheet of IAUT300N08S5N011 (80 V, 1.1mΩ in TOLL).

To ensure that the C_{VCP} discharge is limited to V_{Drop}, the following equation has to be fullfilled:

$$C_{VCP} \times \Delta V_{Discharge\_Cvcp} \geq NbrMOS \times Q_{1xMOS}$$

Detailed analysis for the Charge Pump external components

$$\Rightarrow C_{VCP} \times \Delta V_{Discharge\_Cvcp} \geq NbrMOS \times \left[Q_g + (C_{iSS} \times 3.5)\right] \text{ where } \Delta V_{Discharge\_Cvcp} = 1V, \text{ so}$$

$$C_{VCP} \geq NbrMOS \times \left[Q_g + (C_{iSS} \times 3.5)\right]$$

Note: The number of MOSFETs (NbrMOS) to consider is the total number of MOSFETs activated simultaneously. If channels A and B are activated at the same time (same SPI command), the number of MOSFETs to consider is the total of MOSFETs driven from GA and GB pins.

Considering 8 MOSFETs IAUT300N08S5N011 connected in back-to-back (2 times 4 MOSFETs) common drain simultaneously switched ON, the resulting minimum value for C_{VCP} is:

$$C_{VCP} \geq NbrMOS \times \left[Q_g + (C_{iSS} \times 3.5)\right] \Rightarrow C_{VCP} \geq 8 \times [178 \times 10^{-9} + (12500 \times 10^{-12} \times 3.5)]$$

$$\boldsymbol{C_{VCP} \geq 1.77\ \mu F}$$

6.6.2 Minimum value defined by the sawtooth peak-to-peak voltage

When 2ED4820-EM is used in applications where there is no need to use MOSFETs in parallel (DC current below 30A typically), the total gate charge is rather small (Qg).

As an example, 2ED4820 EB2 2HSV48 demoboard is based on two IAUC100N08S5N043 transistors configured in either common drain or common source back-to-back.

Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	2970	3860	pF
Output capacitance	C_{oss}		-	490	640	
Reverse transfer capacitance	C_{rss}		-	23	35	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=50 A, V_{GS}=0 to 10 V	-	14	18	nC
Gate to drain charge	Q_{gd}		-	9.3	14	
Gate charge total	Q_g		-	43	56	

Figure 10 Extract from IAUC100N08S5N043 datasheet.

$$C_{VCP} \geq NbrMOS \times \left[Q_g + (C_{iSS} \times 3.5)\right] \Rightarrow 8 \times [43 \times 10^{-9} + (2970 \times 10^{-12} \times 3.5)]$$

$$\boldsymbol{C_{VCP} \geq 107\ nF}$$

The value for C_{VCP} is smaller than C_{CPHL}, which would generate the following issue: the voltage step generated by the transfer of C_{CPHL} to C_{VCP} during the pump phase is higher than the hysteresis defined between $V_{CP\_PUMP\_H}$ and $V_{CP\_PUMP\_L}$ thresholds ($V_{CP\_PUMP\_HY}$ = 1V typ.):

$$C_{VCP} \times \Delta V_{Charge\_Cvcp} = I_{CPL\_PULSE} \times t_{Charge\_Cvcp}$$

$$\Delta V_{Charge\_Cvcp} = \frac{I_{CPL\_PULSE} \times t_{Charge\_Cvcp}}{C_{VCP}} \quad \Rightarrow \quad \Delta V_{Charge\_Cvcp} = \frac{0.08 \times 3.2 \times 10^{-6}}{107 \times 10^{-9}} = 2.4\ V$$

In order to have a good control of the sawtooth waveform and to limit the peak voltage on C_{VCP}, the recommendation is to have C_{VCP} >> C_{CPHL} so that ΔV_{Charge_Cvcp} is controlled by the two thresholds $V_{CP\_PUMP\_H}$ and $V_{CP\_PUMP\_L}$.

Detailed analysis for the Charge Pump external components

The number of charge pulses during the pump phase ($Nbr_{ChargePulses}$)will be a function of the ratio between C_{VCP} and C_{CPHL}. To calculate it, we consider that the pump phase stops when the charge stored in C_{CPHL} multiplied by $Nbr_{ChargePulses}$ equals the required charge on C_{VCP} to reach the sawtooth hysteresis:

$$Nbr_{ChargePulses} \times \left[C_{CPHL} \times \Delta V_{Charge\_Ccphl}\right] \sim C_{VCP} \times V_{CP\_PUMP\_HY}$$

$$Nbr_{ChargePulses} \sim \frac{C_{VCP}}{C_{CPHL}} \times \frac{V_{CP\_PUMP\_HY}}{\Delta V_{Charge\_Ccphl}}$$

Note: This formula applies when there is a limited current loading the charge pump, so that we can consider that the entire charge current goes to C_{VCP} and not to the load.

It is recommended to have at least 3 charge pulses for a controlled hysteresis and frequency of the sawtooth waveform on VCP.

$$C_{VCP} \sim Nbr_{ChargePulses} \times C_{CPHL} \times \frac{\Delta V_{Charge\_Ccphl}}{V_{CP\_PUMP\_HY}}$$

$$Nbr_{ChargePulses} > 3 \quad \rightarrow \quad C_{VCP} > 3 \times 0.22 \frac{1.16}{1}$$

$$\boldsymbol{C_{VCP} > 0.77\ \mu F}$$

6.6.1 Maximum value defined by the undervoltage blanking time

2ED4820-EM comes with a latching fault detection: charge pump undervoltage. To avoid a wrong trigger at activation, a blanking mechanism is implemented, during a time $t_{VCP\_UV\_BLK}$.

The value of C_{VCP} has therefore to ensure that the voltage across the capacitor reaches $V_{CP\_UV\_H}$ before the time $t_{VCP\_UV\_BLK}$.

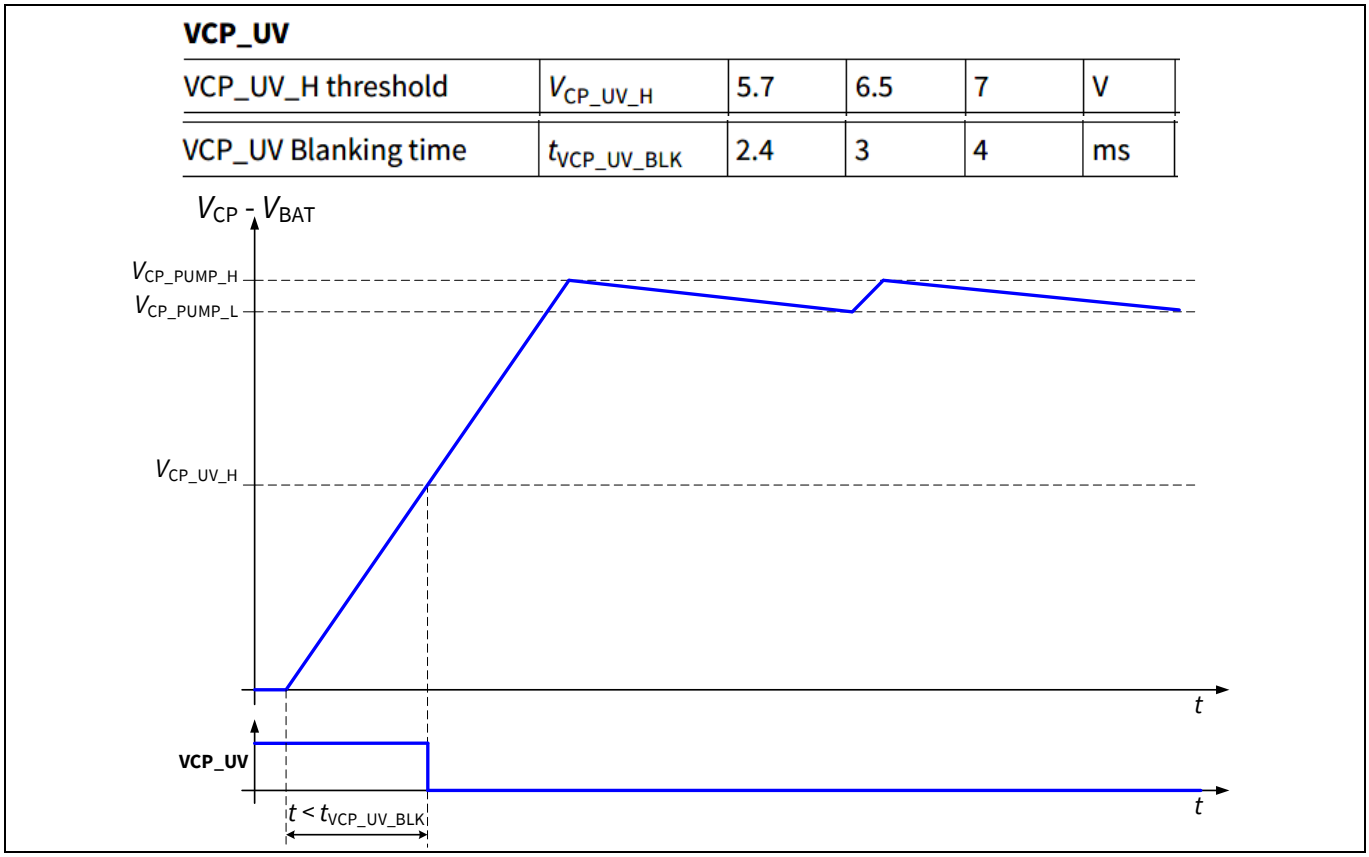

Figure 11 Charge pump undervoltage blanking during activation.

During the pump phase, C_{VCP} is charged by a current source I_{CPL_PULSE} for half of the time, so the time to charge C_{VCP} until $V_{CP\_UV\_H}$ is defined by: $t_{ch} = \frac{C_{VCP} \times V_{CP\_UV\_H}}{\left[\frac{1}{2} \times I_{CPL\_PULSE}\right]}$

This time has to be smaller than $t_{VCP\_UV\_H}$: $t_{ch} \leq t_{VCP\_UV\_BLK} \Rightarrow \frac{C_{VCP} \times V_{CP\_UV\_H}}{\left[\frac{1}{2} \times I_{CPL\_PULSE}\right]} \leq t_{VCP\_UV\_BLK}$

$$C_{VCP} \leq \frac{\left[\frac{1}{2} \times I_{CPL\_PULSE,min}\right] \times t_{VCP\_UV\_BLK,min}}{V_{CP\_UV\_H,max}} \Rightarrow C_{VCP} \leq \frac{\left[\frac{1}{2} \times 0.06\right] \times 0.0024}{7} \Rightarrow \boldsymbol{C_{VCP} \leq 10.3\ \mu F}$$

This value is independent of the number of MOSFETs to drive.

6.6.1 Range of values for C_{VCP}

As a summary, C_{VCP} has to fulfill:

$$\boldsymbol{C_{VCP} > 0.77 \mu F}$$

$$\boldsymbol{C_{VCP} \geq NbrMOS \times \left[Q_g + (C_{iSS} \times 3.5)\right]}$$

$$\boldsymbol{C_{VCP} \leq 10.3\ \mu F}$$

6.7 Maximum output current for external circuits

The charge pump is designed to deliver the required current for the internal circuits it supplies:

- The gate output drivers for channels A & B
- The current sense amplifier

The datasheet specifies the maximum current which can be also consumed in addition from an external circuit supplied from the charge pump: it can deliver at least 10 mA

Charge pump output current							
Charge pump output current capability at VCP	I_{CPO}	–	–	-10	mA	C_{CPHL} = 220 nF;	PRQ-349

Figure 12 Maximum output current capability.

6.8 Scope captures

In this section, 2ED4820-EM is configured with:

- C_{VCP} = 2.2 µF
- C_{CPHL} = 220 nF
- ENABLE = '1'; Both channels A & B are OFF.

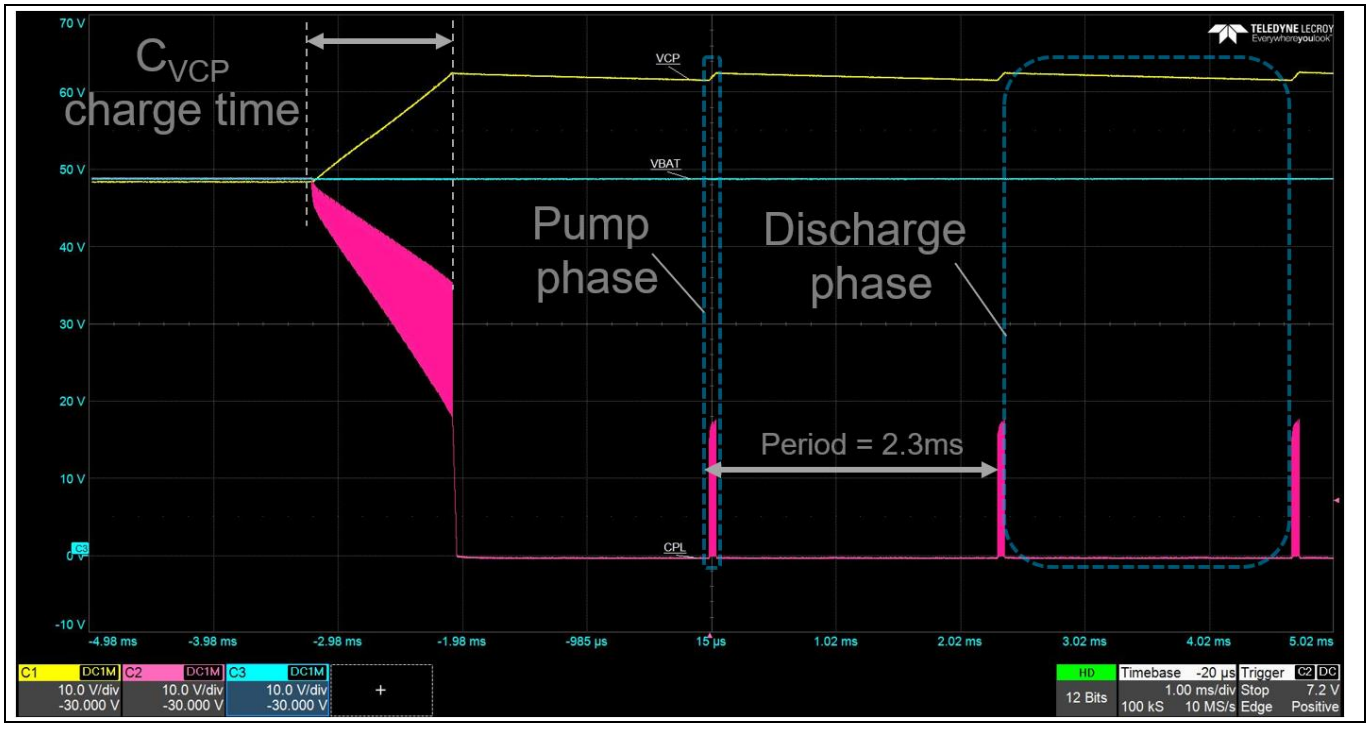

Figure 13 Charge pump activation

The average current consumption on CVCP can be estimated based on the duration of the discharge phase:

$$I_{VCP\_Avg} = \frac{C_{VCP} \times [V_{CP\_PUMP\_H} - V_{CP\_PUMP\_L}]}{t_{Disch\_Phase}} = \frac{C_{VCP} \times V_{CP\_PUMP\_HY}}{t_{Disch\_Phase}}$$

$$I_{VCP\_Avg} = \frac{2.2\times10^{-6}\times1}{2.2\times10^{-3}} = 1\ mA \text{ (both channels A \& B are OFF)}$$

Detailed analysis for the Charge Pump external components

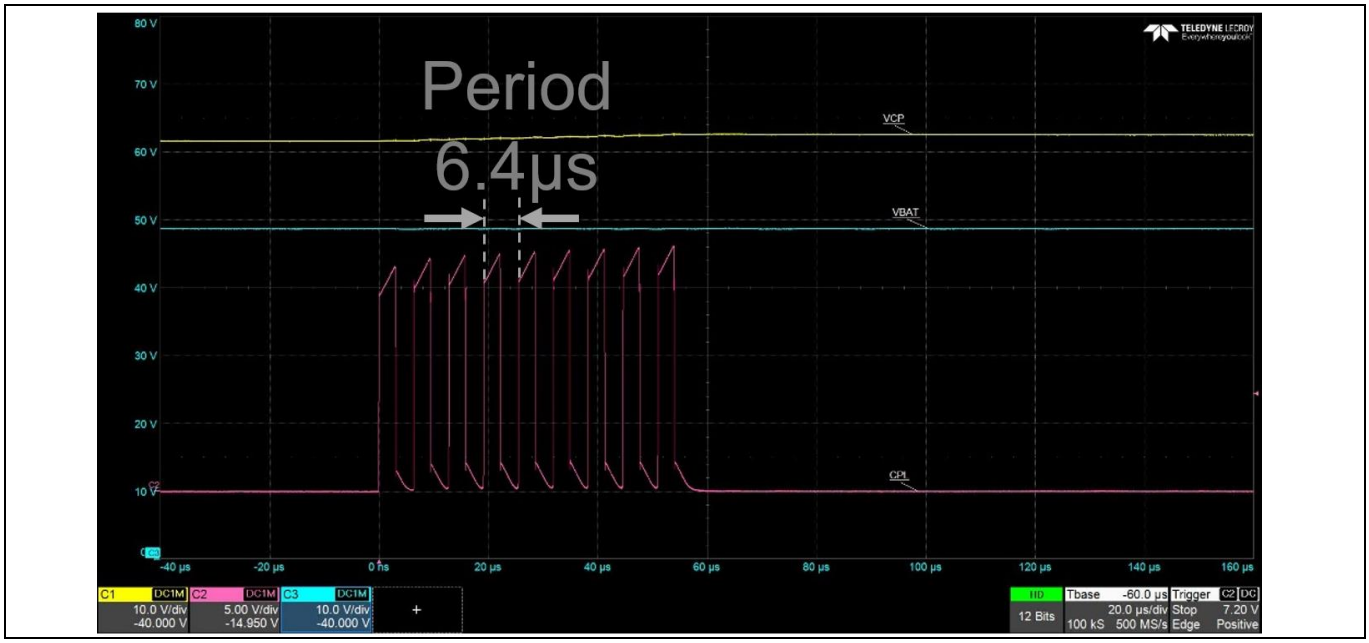

Figure 14 CPL shape zoomed.

The number of pulses during the pump phase can be checked by the formula described previously:

$$Nbr_{ChargePulses} \sim \frac{C_{VCP} \times V_{CP\_PUMP\_HY}}{C_{CPHL} \times \Delta V_{Charge\_Ccphl}} \quad => \quad Nbr_{ChargePulses} \sim \frac{2.2 \times 1}{0.22 \times 1.16} = 8.6 \text{ pulses}$$

Now adding a 60kΩ resistor on VCP to ground on the VCP pin, to simulate an external circuitry consuming 10mA, the charge pump behavior becomes:

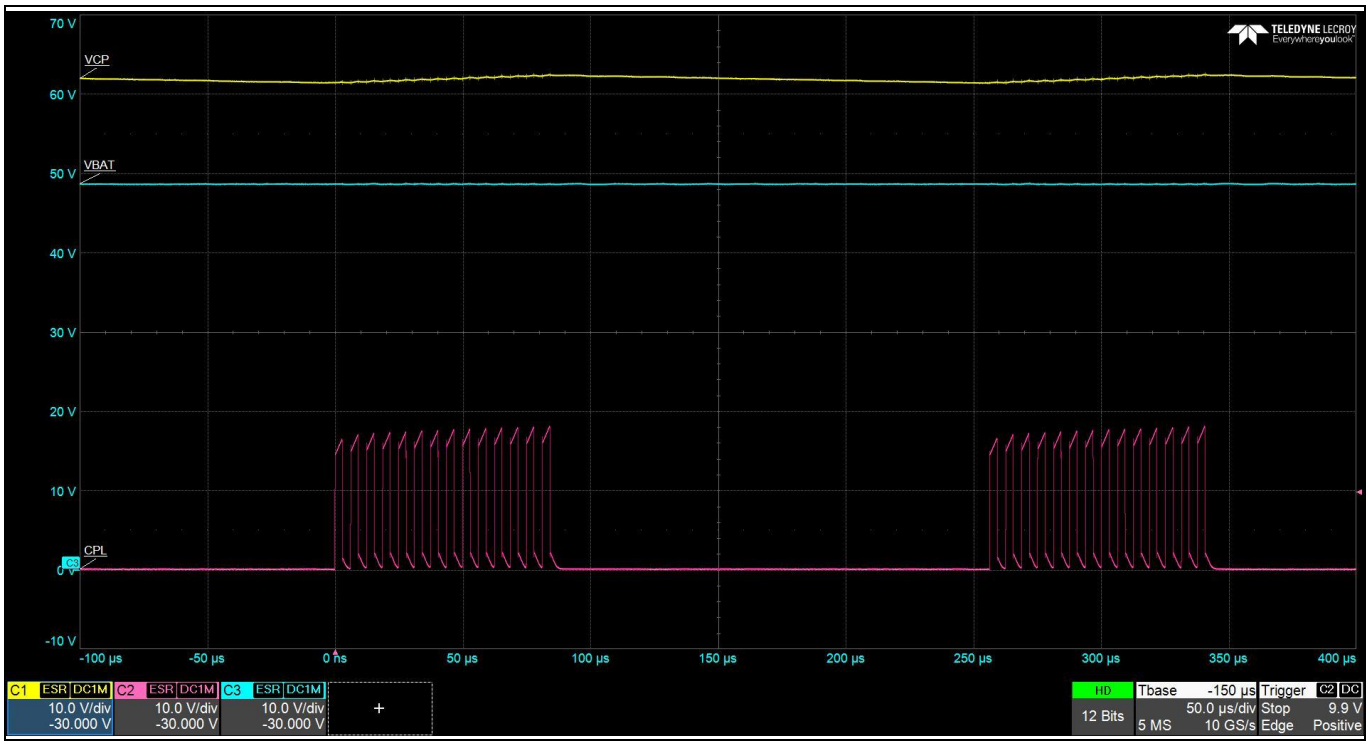

Figure 15 C_{VCP} = 2.2 µF, both channels OFF + 60 kΩ resistor between VCP pin and ground.

Detailed analysis for the Charge Pump external components

The pump phase counts now 14 pulses due to the 10 mA DC current added on the output of the charge pump, which makes the pump phase less efficient to recharge C_{VCP} (part of the charge current goes to the load, not to C_{VCP}).

The next scope plot shows the comparison of the VCP and CPL voltages when using C_{VCP} = 2.2 µF or C_{VCP} = 100 nF. Both plots are based on the same timescale (500 µs/div) for an easy comparison.

Table 5 Comparison of the behaviors when changing C_{VCP}

Parameter	C_{VCP} = 2.2 µF	C_{VCP} = 100 nF
Voltage ripple on VCP	1 V	>2 V
Period between Pump phases	2.2 ms	Unstable: from 100 µs to 250 µs
Number of pulses in pump phase	9 or 10	1 or 2

Figure 16 Effect of small value for C_{VCP} < C_{CPHL}.

Detailed analysis for the Charge Pump external components

Moving C_{VCP} to 680 nF (possible here since the 2ED4820-EM only drives two IAUC100N08S5N043 with Qg = 43 nC), the period between 2 pump phases is now much more stable, at 700µs (based on the current consumed when the channels A & B are both OFF). Each pump phase is 3-pulse long.

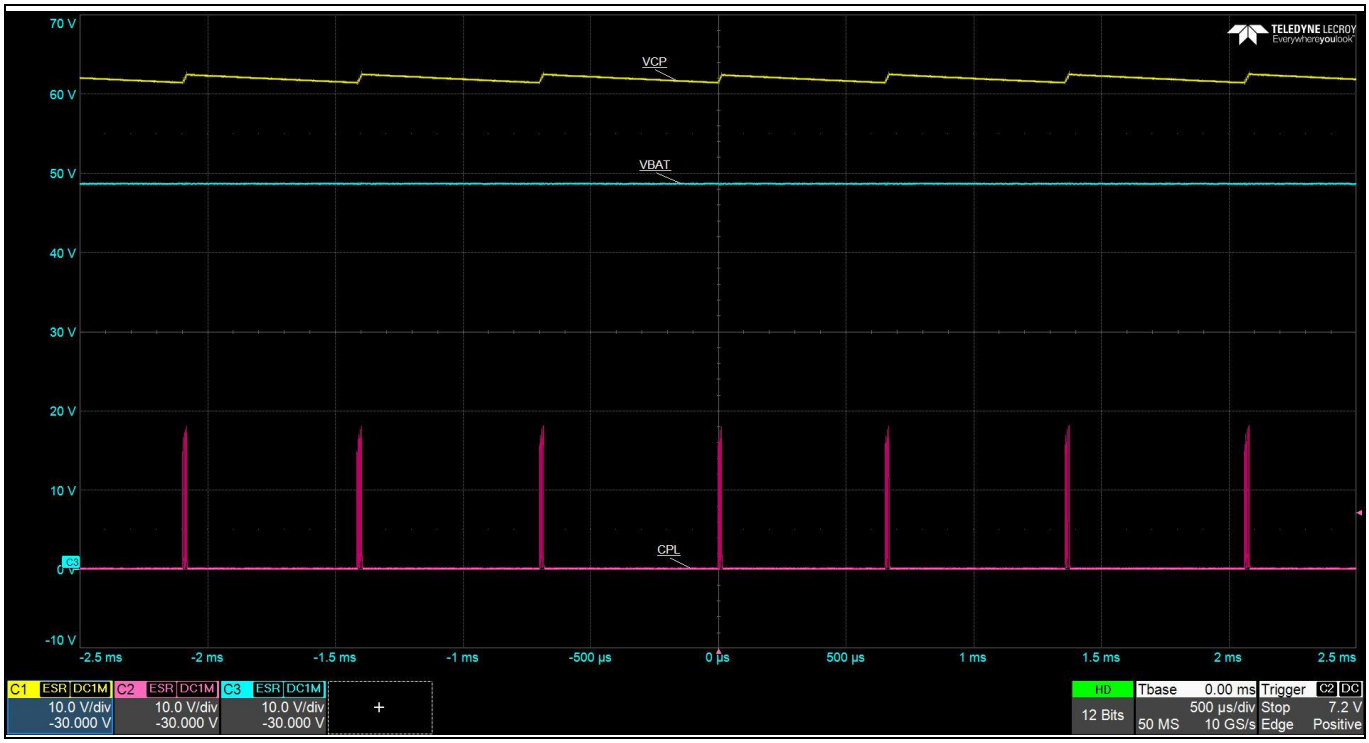

Figure 17 C_{VCP} = 680 nF, both channels OFF.

Adding an external 60kΩ resistor to ground on the VCP pin, to simulate an external circuitry consuming 10mA, the charge pump behavior is still correct (stable discharge time, 5 pulses during the pump phase):

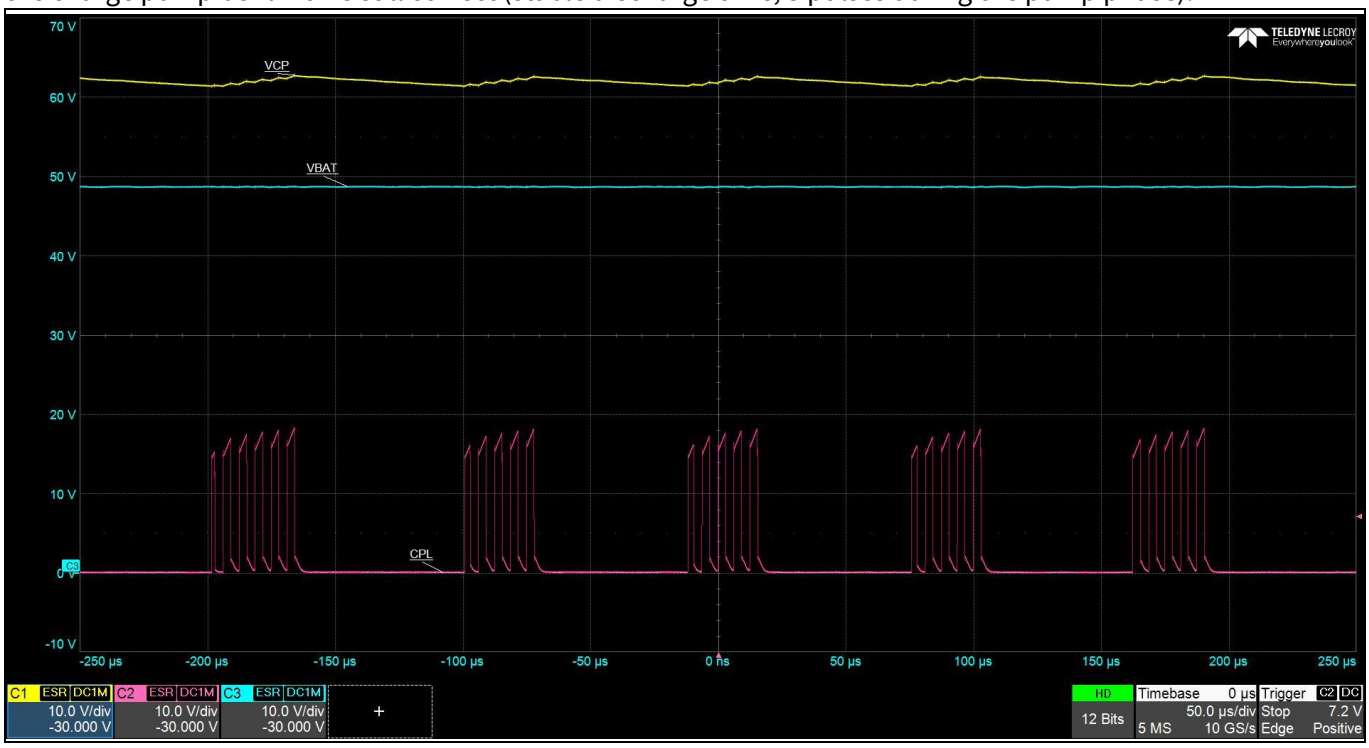

Figure 18 C_{VCP} = 680 nF, both channels OFF + 60 kΩ resistor between VCP pin and ground.

7 Detailed analysis for the R_G & R_{GS} resistors

2ED4820-EM comes with a unique gate drive sheme: it is based on switched current sources combined with an integrated 18V Zener diode.

This concept brings several benefits:

1. Controlled voltage slew rate on the gate, thanks to the constant charge and sink currents
2. No need for external protection circuit built with [resistor + Zener diode] to prevent the V_{GS} of the MOSFET(s) to exceed their maximum rating.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Gate charge current high	I_{CHARGE}	–	–	-300	mA	$V_{Gx} = V_{Sx} = 0$ V	PRQ-133
Gate charge current low	I_{CHARGE_LOW}	-5	-4	-2.5	mA	–	PRQ-488
Gate discharge current	I_{SINK}	0.9	1.1	1.3	A	$V_{Gx} - V_{Sx} = 13$ V	PRQ-134

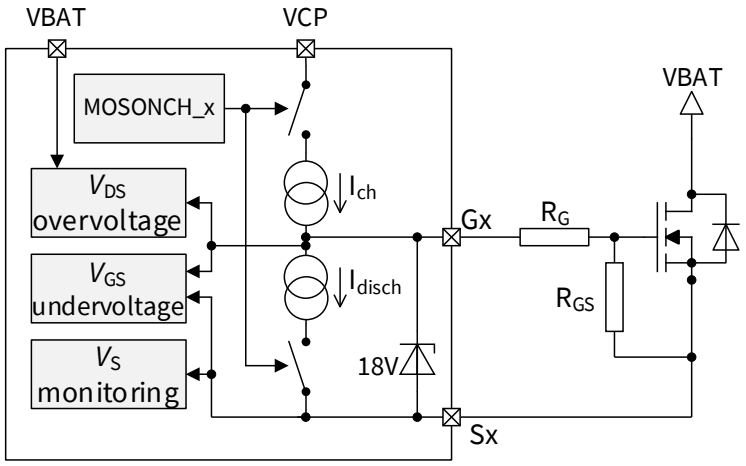

Figure 19 2ED4820-EM gate driver concept.

7.1 R_G resistor

A series resistor on the MOSFET gate (R_G) is requested, to fulfill the dV_{Sx}/dt parameter listed in the absolute maximum ratings:

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Source voltage transients slew rate	dV_{Sx}/dt	-70	–	70	V/µs	1)	PRQ-399

Figure 20 2ED4820-EM datasheet extract showing the maximum allowed slew rate on Sx pins.

R_G value has to be tuned depending on the number of MOSFETs connected to the corresponding Gx pin.
This is especially requested when there is a low number of small MOSFETs connected, because the charge and discharge currents are very high, which leads to very fast slew rate when the total C_{iss} is small.

Detailed analysis for the RG & RGS resistors

The next figure shows scope plots captured on the 2HSV48 EB2 demoboard, where only two IAUC100N08S5N043 are driven: when R_G = 10 Ω, the slew rate is so fast that the gate driver oscillates for a short time before the MOSFETs are properly switched OFF.

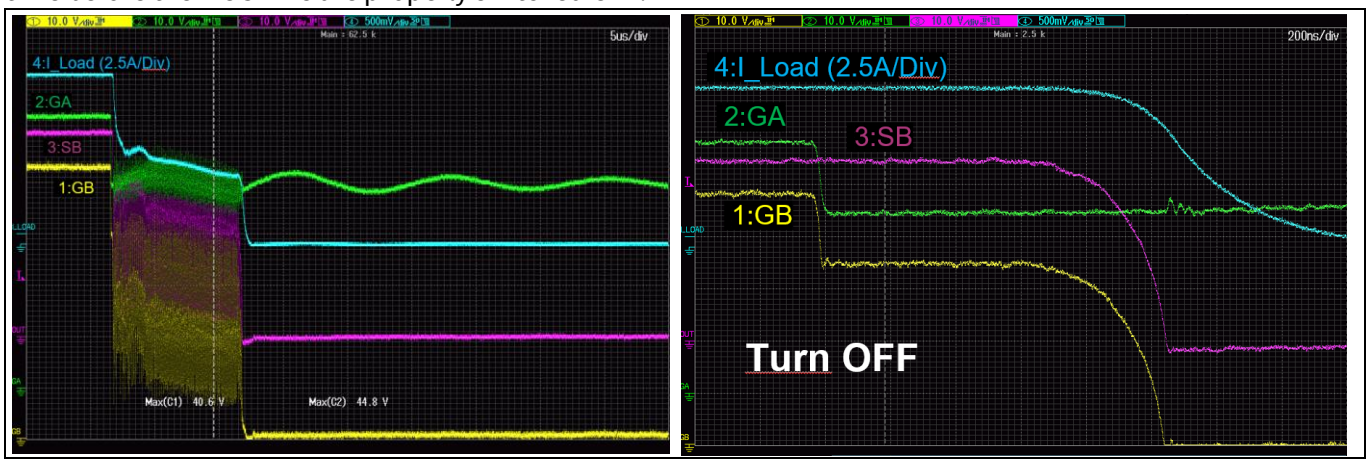

Figure 21 Left hand side: R_G = 10 Ω, right hand side: R_G = 180 Ω.

The criteria to properly size R_G is:

$$R_G \times C_{iss} \geq 1\ \mu s$$

$$R_G \geq \frac{1\mu s}{C_{iss}}$$

Considering two IAUC100N08S5N043 with C_{iss} = 2970 pF, we end up with:

$$R_G \geq \frac{10^{-6}}{(2 \times 2970) \times 10^{-12}} \quad => \quad R_G \geq 168\ \Omega$$

When there are multiple MOSFETs in parallel, it is helpful to use one R_G resistor per MOSFET: this is a way to better balance the signal propagation from the EiceDRIVER™ APD 2ED4820-EM to the gate pins of each MOSFET, resulting in a better sharing of the current at turn ON and turn OFF.

Figure 22 illustrates a configuration with four pairs of MOSFETs in common source back-to-back. The benefit of the individual R_G resistor is also that it is possible to check each individual MOSFET on the manufacturing production line, applying a voltage on each gate thanks to the test points.

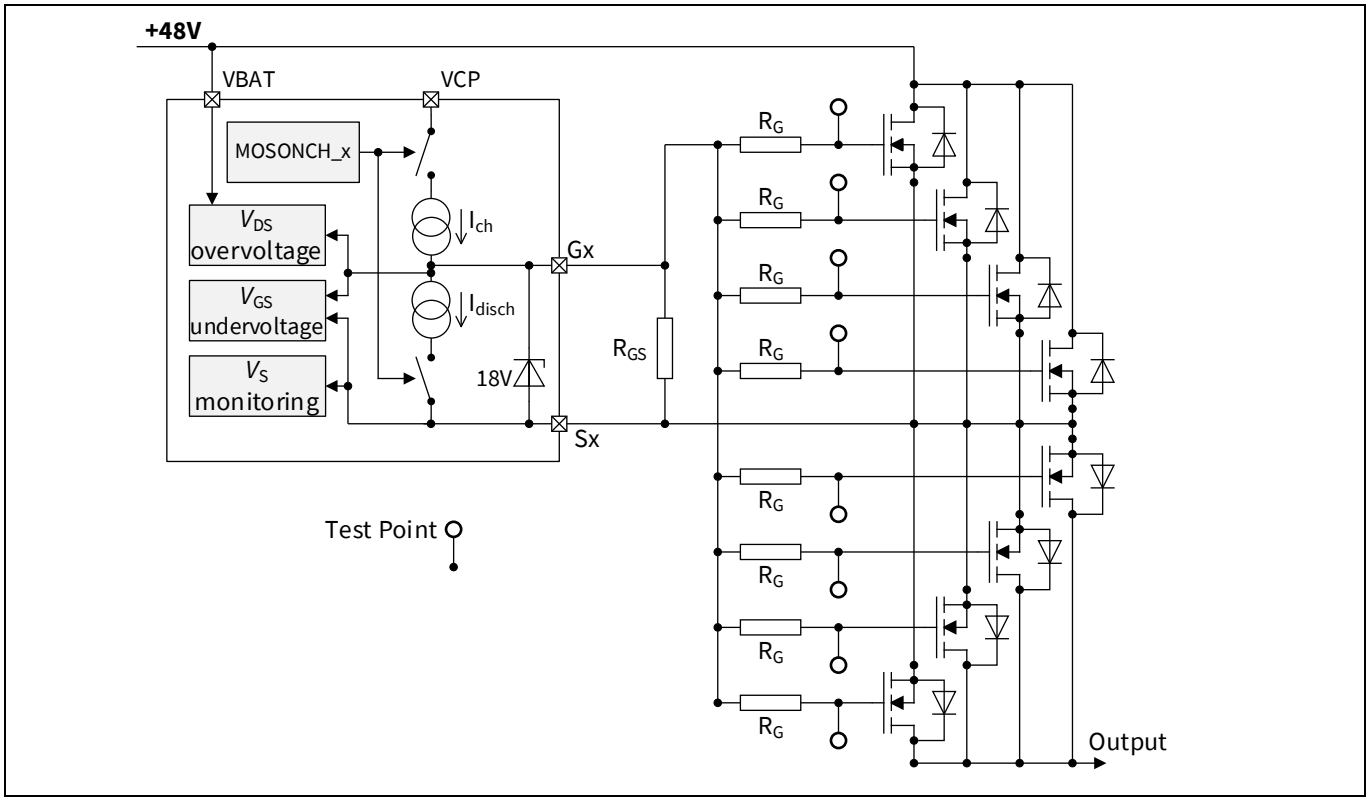

Figure 22 Example of a network of RG resistors for a common source structure with 2x 4 MOSFETs.

7.1 R_{GS} resistor

An additional resistor is often added between the MOSFETs gate & source pins (R_{GS}) as a way to ensure that the MOSFET(s) are kept OFF by default. This R_{GS} resistor adds a DC current on the charge pump when the MOSFETs are turned ON, which has to be kept below the maximum allowed current consumption:

Charge pump output current							
Charge pump output current capability at VCP	I_{CPO}	–	–	-10	mA	C_{CPHL} = 220 nF;	PRQ-349

Figure 23 Maximum output current capability.

Each channel has therefore to consume less than 5 mA on the charge pump. This translates into a minimum value for R_{GS}: $V_{CP\_PUMP\_H}$

$$R_{GS} \geq \frac{V_{CP\_PUMP\_H}}{\frac{1}{2} \times I_{CPO}}$$

$$R_{GS} \geq \frac{14}{\frac{1}{2} \times 0.01}$$

$$R_{GS} \geq 2.8\ k\Omega$$

8 Detailed analysis for the R_{FiltSh} & C_{FiltSh} filter

8.1 Parasitic inductance of a shunt

Ultra-low ohmic power shunts have a rather big mechanical size and they come with a parasitic inductance:

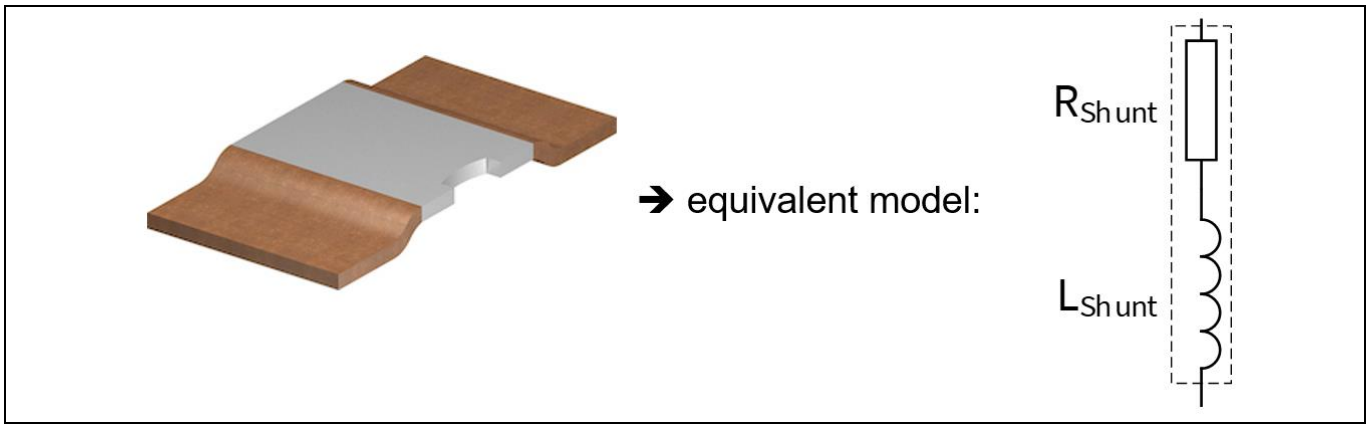

Figure 24 Equivalent model of an ultra-low ohmic power shunt.

Assuming a shunt with R_{Shunt} = 100µΩ and L_{Shunt} = 1nH:

- In 48V application, when a short-circuit happens with parasitic wiring inductance of L_{Wire} = **2µH** *(roughly 2 meters for non-shielded wires)*, the current slope is:

$$\frac{dI}{dt} = \frac{U}{L_{Wire}} = \frac{48}{2.10^{-6}} = 24.10^{6} A/s = \mathbf{24}\boldsymbol{A}/\mu\boldsymbol{s}$$

- Such a current slope in the parasitic inductor of the Shunt translates into a voltage drop of:

$$U_{Error} = L_{Shunt} \times \frac{dI}{dt} = 10^{-9} \times 24.10^{6} = \mathbf{24}\boldsymbol{mV}$$

- Since the shunt is 100µΩ, this means an error on the current sensed of:

$$I_{Error} = \frac{U_{Error}}{R_{Shunt}} = \frac{0.024}{0.0001} = \mathbf{240}\boldsymbol{A}\ !!$$

To cancel this error introduced by the parasitic inductance of the shunt, a filter is added in parallel to the shunt. It is built with two resistors and one capacitor according to the schematic shown in **Figure 25**:

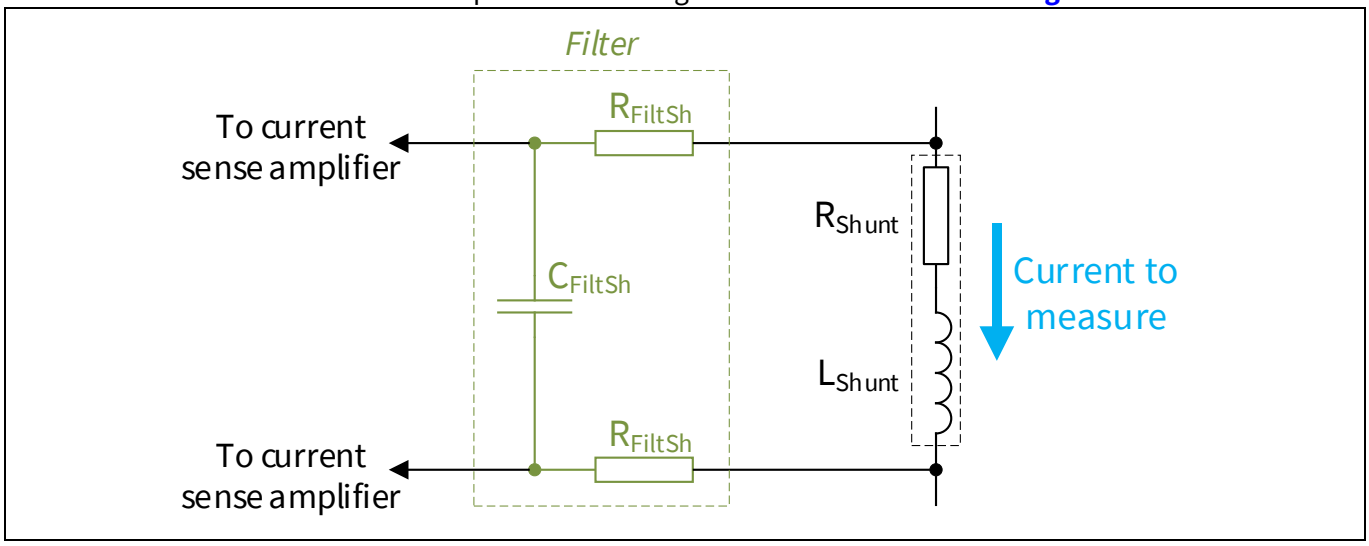

Figure 25 Equivalent model of an ultra-low ohmic power shunt.

Detailed analysis for the RFiltSh & CFiltSh filter

The filter is optimum when (2xR_{FiltSh})xC_{FiltSh} time constant maches the L_{Shunt}/R_{Shunt} time constant: the capacitance value is calculated by:

$$C_{FiltSh} = \frac{L_{Shunt}}{(2 \times R_{FiltSh}) \times R_{Shunt}}$$

The resistors value R_{FiltSh} is contrained by the input impedance of the differential current sense amplifier integrated in the EiceDRIVER™ APD 2ED4820-EM:

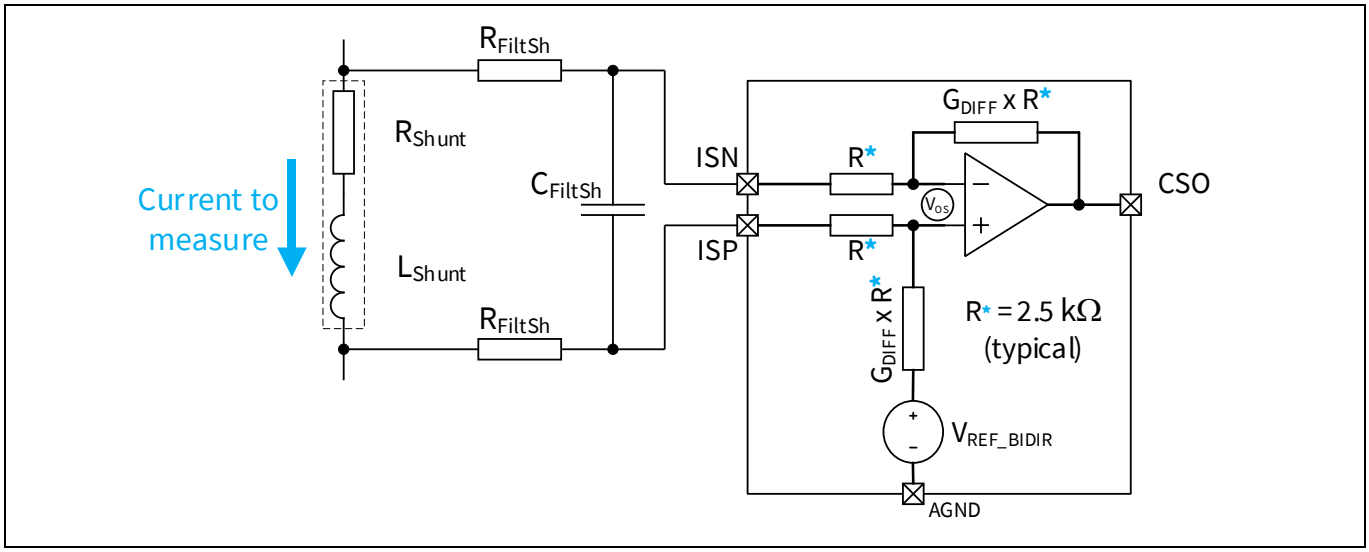

Figure 26 Shunt, Filter and differential current sense amplifier interconnection.

Without the filter, the gain of the current sense amplifier is defined by:

$$Gain = \frac{G_{DIFF} \times R}{R}$$

Adding the external R_{FiltSh} resistors, the gain becomes:

$$Gain = \frac{G_{DIFF} \times R}{(R + R_{FiltSh})}$$

To limit the error on the gain below 1%, R_{FiltSh} has to be sized such that:

$$R_{FiltSh} \leq 0.01 \times R$$

$$R_{FiltSh} \leq 25\Omega$$

To illustrate the benefit of the filter, here are simulation results, with current slopes of 20A/µs (which are achievable in a system with 48V supply and 2.4µH parasitic wiring inductance):

1. **Figure 27** shows the output of the filter versus the current in the shunt: there is a perfect match
2. **Figure 28** shows the output of the filter if C_{FiltSh} is deviating from the ideal value by +/-20%

These simulations clearly show that

- It is necessary to carefully characterize the value of the parasitic inductance of the shunt, L_{Shunt}
- It is necessary to use resistors and capacitors with a good accuracy for R_{FiltSh} and C_{FiltSh}.

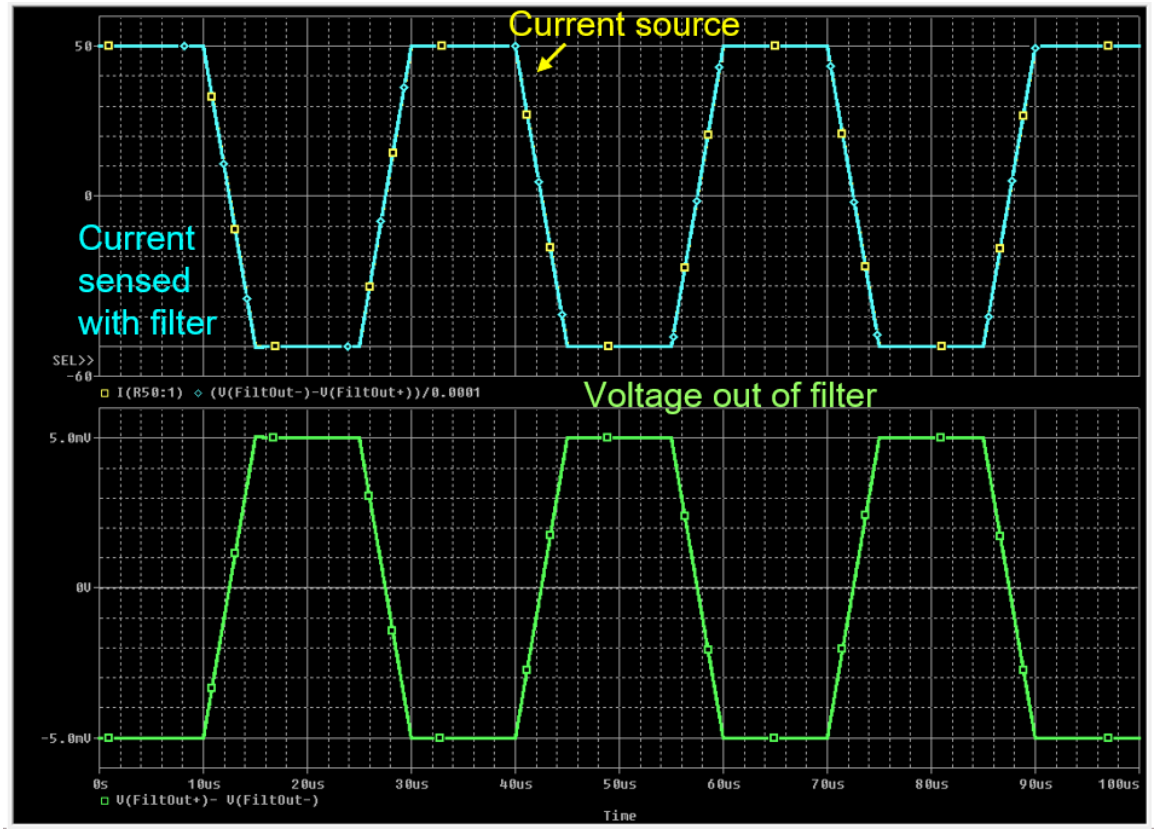

Figure 27 Conditions: RShunt = 100µΩ, LShunt = 1nH, RFiltSh = 4.7Ω, CFiltSh = 1.064µF.

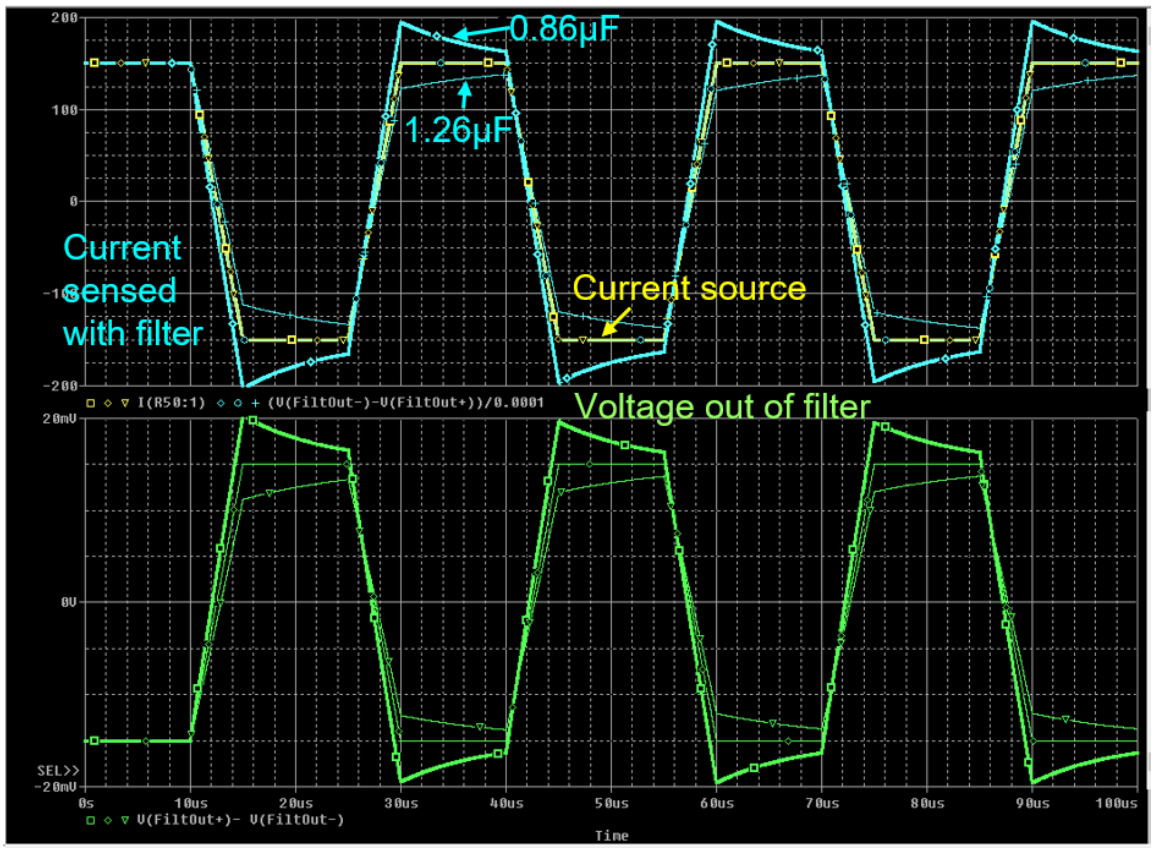

Figure 28 Conditions: RShunt = 100µΩ, LShunt = 1nH, RFiltSh = 4.7Ω, CFiltSh = 1.064µF +/-20%.

Revision history

Document version	Date of release	Description of changes
Rev 1.0	2022-01-03	First version
Rev 1.1	2022-01-06	Updated the front-page layout

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