Dual-channel isolated EiceDRIVER™ 2EDF7275K in telecom bricks

Application example in a 600 W quarter-brick 48 V to 12 V full-bridge to full-bridge rectifier evaluation board

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About this document

Scope and purpose

This application note presents the benefits of using the EiceDRIVER™ **2EDF7275K** to increase the system efficiency, power density and robustness of telecom bricks. The 4 A/8 A source/sink output currents, combined with a low 37 ns propagation delay and highly accurate timing over both temperature and production, are the perfect fit for high-frequency Pulse Width Modulation (PWM) control with the tightest possible dead-time windows, delivering highest conversion efficiency. This dual-channel isolated gate driver IC is available in a small form-factor LGA-13 5 mm x 5 mm package, which enables significant PCB area saving in DC-DC converters. A 600 W Quarter-Brick (QB) 48 V to 12 V Full-Bridge to Full-Bridge (FB-FB) rectifier evaluation board is used as an application example.

Intended audience

This application note is targeted at application engineers and designers of Switch-Mode Power Supplies (SMPS) for telecom bricks looking for isolated gate driving solutions for power MOSFETs.

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1 Introduction

Telecom DC-DC converter bricks can leverage the benefits of using the EiceDRIVER™ **2EDF7275K** [1] to increase system efficiency, power density and robustness. A 600 W QB 48 V to 12 V FB-FB rectifier evaluation board is used as an application example for the **2EDF7275K** dual-channel isolated gate driver IC, as shown in **Figure 1**. In this first section, the system is described along with the FB-FB topology and respective modulation. Additionally, the main parameters that should be considered during the gate driver selection are also provided including a comparison between the **2EDF7275K** and the next best competitor alternatives. Section 2 describes this gate driver IC and in addition provides the design guidelines for the bypass capacitors and bootstrap circuit, as well as the PCB layout recommendations. The specifications, schematic and layout of the evaluation board are shown in section 3. Finally, the performance results are provided in section 4, including the efficiency measurement for different dead-time settings.

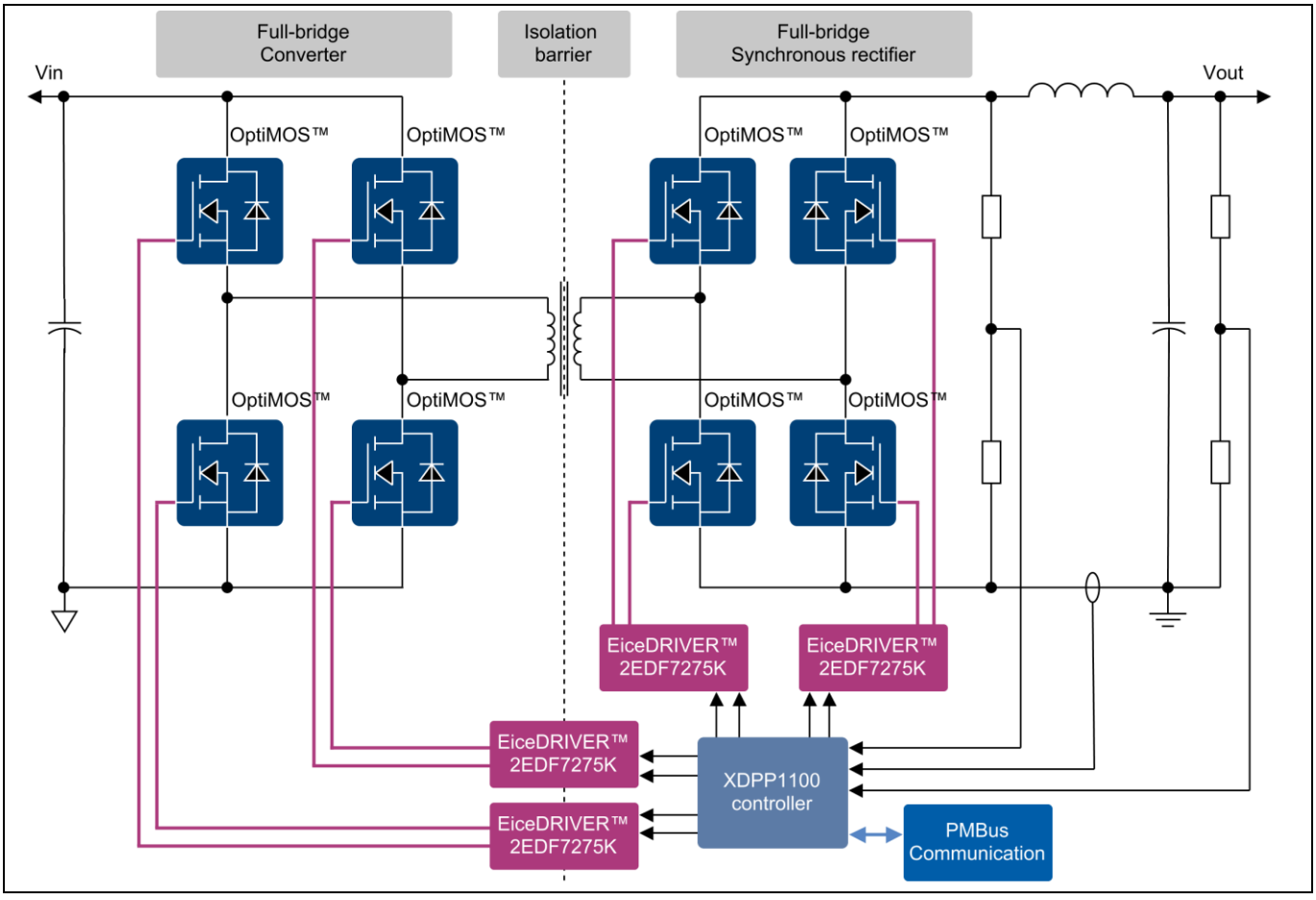

Figure 1 Application diagram of a telecom quarter-brick FB-FB rectifier

1.1 System description

The power conversion sector is always pursuing new solutions to improve efficiency, increase power density and reduce total system cost. In order to increase the power density it's crucial to minimize the heat dissipation by increasing the conversion efficiency. Furthermore, every percentage point in efficiency has a huge impact on the Total Cost of Ownership (TCO) of the telecom station over its life cycle. A QB DC-DC converter is a power module designed to act as the interface between the 48 V and 12 V bus applications. In terms of control architecture, it can be based on a primary-side analog controller or a secondary-side digital controller. The trend in recent years is to use digitally controlled QB DC-DC converters with the ability to optimize the dead-time according to the load in order to achieve the best efficiency.

As described in [2], the isolated FB-FB rectifier QB topology enables the highest efficiency in the 600 W to 800 W power range. This is attained by employing a FB rectifier on the secondary side instead of a center-tapped transformer (FB-CT) with a Low-Side (LS) synchronous rectifier. The latter enables use of a dual-channel non-isolated gate driver IC (e.g., EiceDRIVER™ **2EDN** [3]) referenced to ground as a driving circuit for the two power MOSFETs. Alternatively, the FB-FB topology uses a standard transformer combined with a FB synchronous rectifier on the secondary side, as shown in **Figure 1**.

The XDPP1100 digital controller [4, 5] sits on the secondary side and generates the PWM signals for all the OptiMOS™ power MOSFETs. The EiceDRIVER™ **2EDF7275K** dual-channel isolated gate driver IC provides 1.5 kV DC input-to-output isolation by means of Infineon's Coreless Transformer (CT) technology [6]. By combining the gate driving capability with the galvanic isolation in the same IC, it is possible to avoid the need for a dedicated digital isolator device to transfer the PWM signal across the isolation barrier, from the controller to the primary side of the QB [7]. This clearly simplifies the PCB layout and enables a higher power density and level of integration. Furthermore, the Bill of Materials (BOM) can be further reduced if this driver is used for both primary- and secondary-side full-bridges.

1.2 Topology and modulation

Figure 2 depicts the FB-FB topology employed in the QB evaluation board that will be presented in section 2. As can be seen, the primary side is based on a FB converter (Q3, Q4, Q7, Q8) connected to the primary winding of the transformer. Then, the transformer secondary winding is connected to a full-bridge rectifier with two OptiMOS™ power MOSFETs in parallel for each switch (Q9 to Q16). An LC filter is employed to reduce the output current and output voltage ripple.

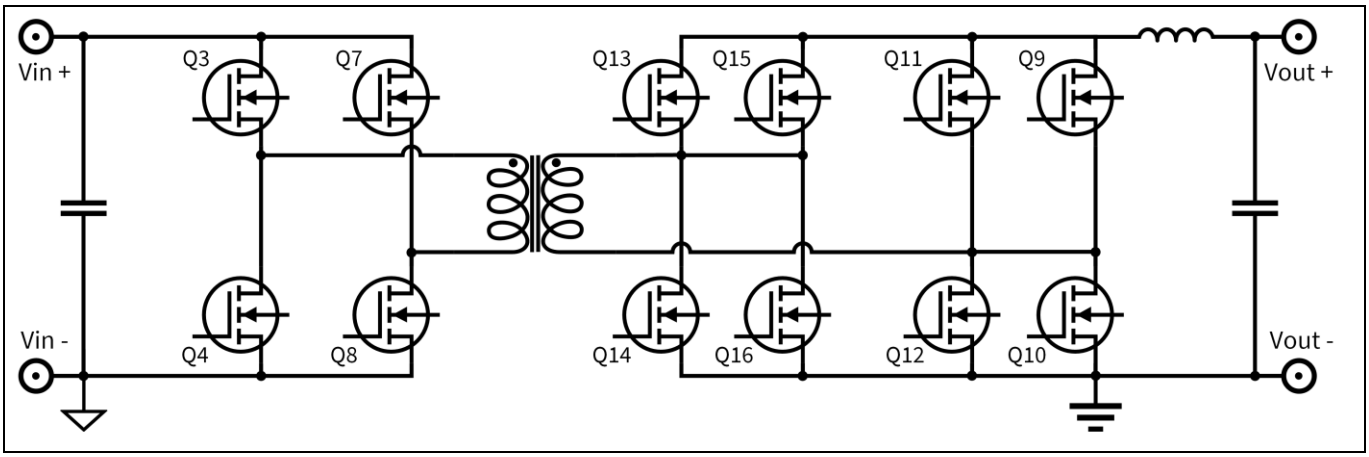

Figure 2 Topology of the FB-FB rectifier

This FB-FB topology is controlled with PWM, where the duty-cycle is adjusted in order to regulate the output voltage (V_{out}) around the set-point (e.g., 12 V) in case of input voltage (V_{in}) change – line regulation, and in case of load change – load regulation. A voltage mode control loop can be implemented by sensing the output current and voltage, as shown in **Figure 1**. Furthermore, the input voltage is derived by measuring the transformer secondary winding.

Figure 3 illustrates the duty-cycle modulation and the dead-time setting for this topology. As shown, the FB converter applies a positive voltage to the transformer during a period equivalent to half of the duty-cycle (D/2) through Q3 and Q8 switches, and then a symmetric negative voltage through Q4 and Q7 switches. The duration

of these two pulses should be exactly the same in order to keep the flux balance[1] and avoid DC flux walk-out in the transformer.

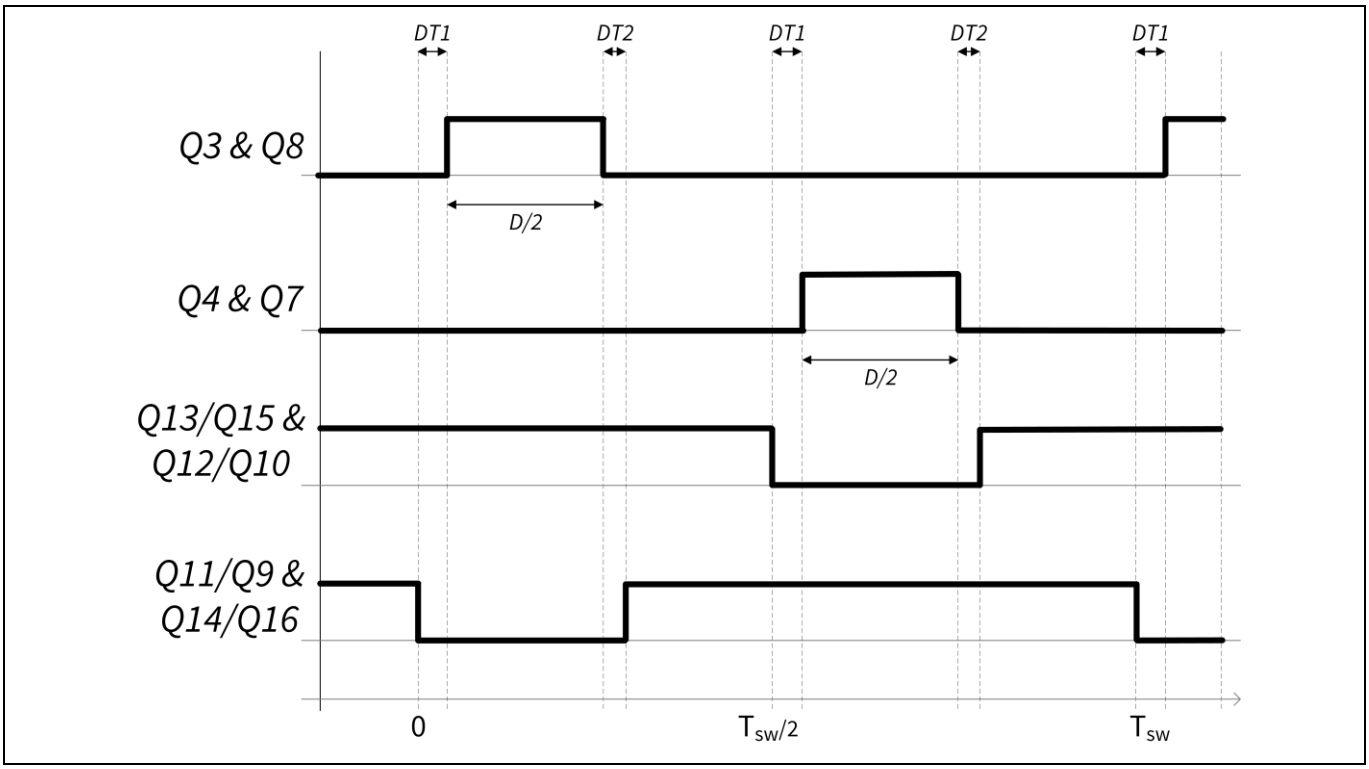

Figure 3 Modulation and dead-time setting

The FB rectifier works in synchronous mode by selectively turning the switches on and off according to the respective primary-side switch pair: Q13/Q15 and Q12/Q10 with Q3 and Q8; Q11/Q9 and Q14/Q16 with Q7 and Q4. When all the primary-side switches are off, the FB synchronous rectifier keeps all their transistors conducting to increase efficiency by minimizing the body diode conduction losses. When one of the primary-side switch pair is turned on, then only the respective FB rectifier MOSFETs conduct.

In order to avoid overlaps that can provoke very large primary-side currents and consequent failure of the power MOSFETs, a proper dead-time should be added to the modulation of both primary- and secondary-side FBs. Dead-time can be set by adding a delay to the rising or falling edge of each PWM output. In this case, the dead-time is added to the rising edge of the PWM signals that came from the controller: DT1 for the FB converter and DT2 for the FB synchronous rectifier.

1.3 Driving the primary- and secondary-side power MOSFETs

The gate driving circuit is a key element in the QB design because it can have a direct impact on the conversion efficiency. The main parameters that should be considered during the gate driver IC selection are:

- **Peak source/sink output current**: higher currents result in fast turn-on and turn-off of power MOSFETs, which reduces the switching losses and improves efficiency
- **Source/sink output resistance**: lower internal resistance generates less undesired power dissipation in the gate driver IC

[1] The XDPP1100 digital controller implements a volt-second-based flux balancing algorithm. More details about its implementation and the experimental results obtained with the 600 W QB 48 V to 12 V FB-FB rectifier evaluation board can be found in application note AN_1910_PL88_1912_032904.

- **Propagation delay variance**: tight propagation delay variance enables dead-time reduction, which improves efficiency by increasing the effective power transfer period
- **Propagation delay mismatch between output channels**: tight propagation mismatch allows smaller dead-time, which improves efficiency by increasing the effective power transfer period
- **Common-Mode Transient Immunity (CMTI)**: higher CMTI ensures there is no false output toggle due to the transient noise produced by fast switching speeds

Table 1 shows a comparison between the EiceDRIVER™ **2EDF7275K** and the next best competitor alternatives. As can be seen, with an 8 A sink output current, the **2EDF7275K** gate driver IC is able to turn-off the power MOSFETs faster and so reduce the switching losses and improve efficiency. Furthermore, since the source/sink output resistance is significantly lower than the competition, it enables this driver to run cooler due to less undesired power dissipation in the IC [8]. The tight propagation delay variance and mismatch between output channels enables programming of narrow dead-times that improve efficiency by increasing the effective power transfer period. Efficiency measurements for different dead-time combinations on the 600 W QB 48 V to 12 V FB-FB evaluation board will be presented in section 3. Finally, the superior CMTI of the **2EDF7275K** driver guarantees a higher system robustness against transient noise produced by fast switching speeds of power MOSFETs.

Table 1 Main parameters for gate driver IC selection: 2EDF7275K vs. competition

Parameter	2EDF7275K	Competitor B	Competitor C	Competitor D	Competitor E
Peak source/sink output current	**4 A/8 A**	4 A/6 A	4 A/4 A	4 A/4 A	1.8 A/4 A
Source/sink output resistance	**0.85 Ω/0.35 Ω**	1.4 Ω/0.55 Ω	1.0 Ω/4.2 Ω	0.95 Ω/0.6 Ω	2.7 Ω/1.0 Ω
Propagation delay variance	**+7 ns/-6 ns**	+11 ns/-5 ns	+11 ns/-9	+20 ns/-19 ns	+30 ns/-15 ns
Propagation delay mismatch between output channels	**3 ns**	5 ns	5 ns	8.5 ns	N.A.
CMTI	**150 V/ns**	100 V/ns	125 V/ns	25 V/ns	200 V/ns

For all these reasons, the EiceDRIVER™ **2EDF7275K** is particularly well suited to driving low $R_{DS(on)}$ power MOSFETs (e.g., OptiMOS™) in high-power-density telecom bricks and other DC-DC converters. In the next section, this gate driver IC will be introduced and the design guidelines for the bypass capacitors, bootstrap circuit and PCB layout recommendations will be provided.

2 EiceDRIVER™ 2EDF7275K dual-channel isolated gate driver

The EiceDRIVER™ **2EDF7275K** is a dual-channel isolated gate-driver IC providing functional 1.5 kV DC input-to-output isolation by means of Infineon's CT technology [6]. **Figure 4** shows the functional block diagram of the EiceDRIVER™ **2EDF7275K** [9]. The input side is usually powered by the same power supply as the PWM controller (VDDI = 3.3 V or VDDI greater than 3.5 V if SLDO is activated). The output-side gate driver voltages VDDA, VDDB can be generated by isolated auxiliary supplies or by a bootstrapping circuit. Both input and output voltage supply are continuously monitored by an Under-Voltage Lockout (UVLO) protection. INA and INB are digital CMOS/TTL logic signal input for channel A and channel B respectively. The DISABLE pin can be used by the controller to enable and disable both output channels. The two rail-to-rail output stages, realized with complementary PMOS and NMOS transistors, are able to provide the necessary sourcing and sinking current. OUTA and OUTB also have up to 5 A peak reverse current capability and active current limitation, which ensures a robust gate driver circuit design.

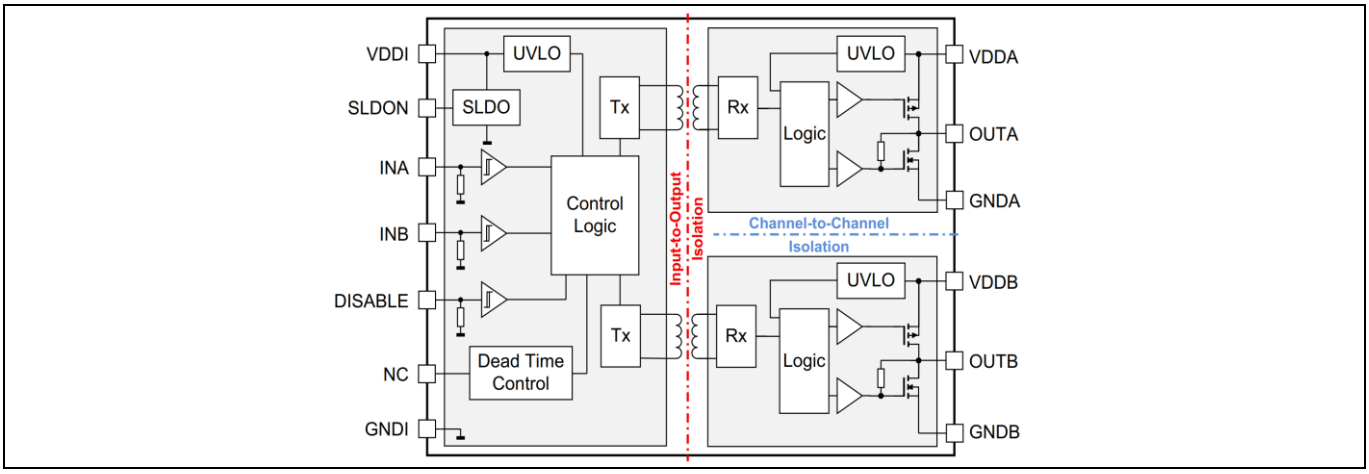

Figure 4 Functional block diagram of the EiceDRIVER™ 2EDF7275K dual-channel isolated gate driver

This gate driver IC is available in a compact LGA-13 5 mm x 5 mm package with 0.65 mm pin pitch, as shown in **Figure 5**. Since there is also channel-to-channel isolation, the two independent driver outputs can be used in a half-bridge, dual LS or dual High-Side (HS) configurations. The functional isolation between the two channels is verified by a sample test with 0.65 kV DC for 10 ms [9]. The 1.0 mm distance over the surface from output pin GNDA to VDDB enables the use of this gate driver IC in applications operating with a DC-link voltage in the range of hundreds of volts.

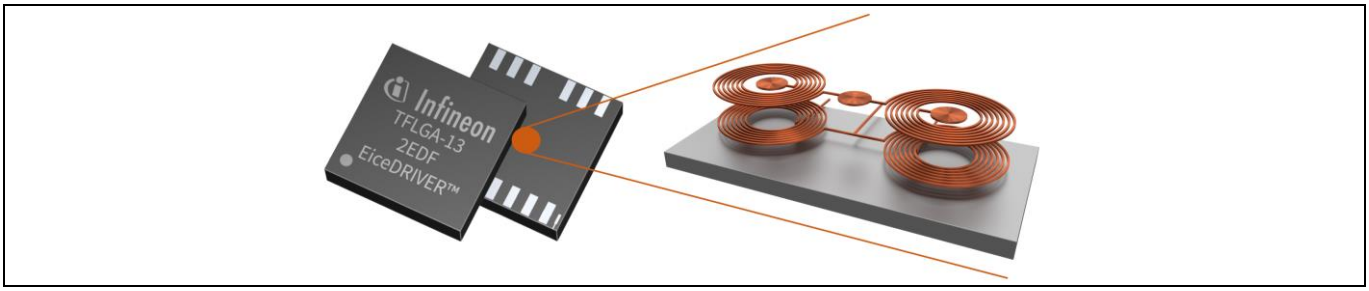

Figure 5 EiceDRIVER™ 2EDF7275K in LGA-13 5 mm x 5 mm with Infineon's CT technology

Figure 6 shows the gate driving circuit for the primary-side FB OptiMOS™ power MOSFETs in the 600 W QB 48 V to 12 V FB-FB evaluation board that will be presented in section 3. As can be seen, each EiceDRIVER™ **2EDF7275K** drives a HB using just a few external components: input and output bypass capacitors and the

bootstrap circuit composed by a diode, resistor and capacitor. The design guidelines for these components and the the PCB layout recommendations will be provided in the following subsections.

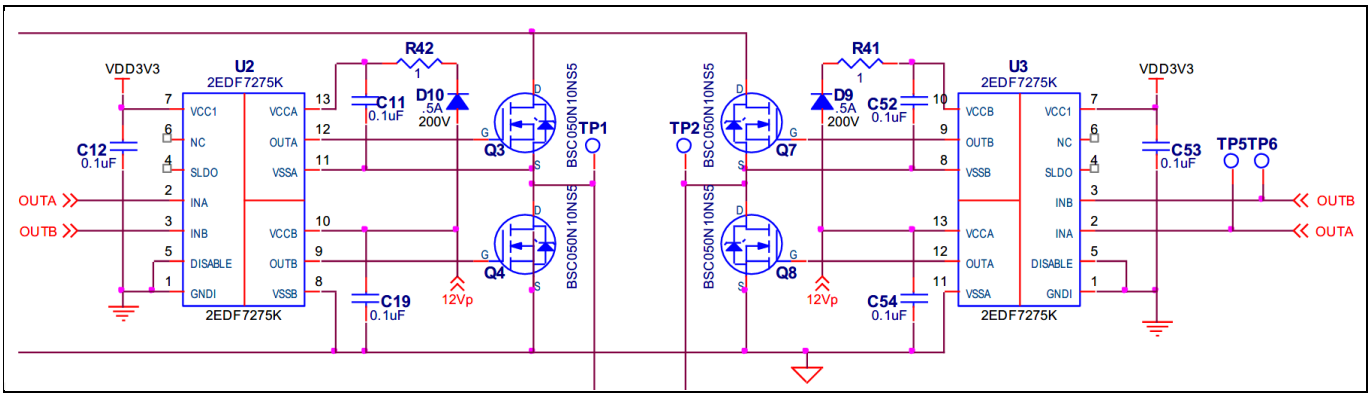

Figure 6 Gate driving circuit for the primary-side FB OptiMOS™ power MOSFETs using the EiceDRIVER™ 2EDF7275K dual-channel isolated gate driver

2.1 Input bypass capacitor dimensioning

Even in non-switching operation the CT is driven by a sequence of 150 mA/2 ns current pulses at a non-constant repetition rate (0.4 to 1.6 µs). Each of these pulses corresponds to a charge ΔQ of 0.3 nC; this causes a voltage ripple on the input bypass capacitance (C_{in}) given by:

$$\Delta V = \frac{\Delta Q}{C_{in}} \quad (1)$$

To keep ΔV sufficiently low (e.g., in the few tens of mV range), a minimum C_{in} of 10 nF is recommended. On the other hand, if the SLDO functionality is activated, C_{in} should not exceed 22 nF for stability reasons. When the SLDO shunt regulator is not needed, instead, 100 nF is a common selection.

2.2 Output bypass capacitor dimensioning

During the turn-on commutation of a MOSFET a short high-current pulse is drained from the driver output bypass capacitance to charge the equivalent input capacitance of the MOSFET (C_{load}). That operation leads to a partial discharge of the bypass capacitance C_{out} by a value ΔV depending on the ratio of the two capacitances involved:

$$\Delta V = V_{DDA} \times \frac{C_{load}}{C_{out} + C_{load}} \quad (2)$$

It is important to distinguish between the equivalent input capacitance C_{load} and the input capacitance C_{iss} as reported in the MOSFET's datasheet. C_{iss} is the instantaneous value of the input capacitance for a certain gate-to-source and drain-to-source voltage; it changes during a switching transient.

The MOSFET equivalent input capacitance C_{load} is, instead, a mean value and can be derived from the total gate charge Q_G necessary to switch the MOSFET according to:

$$C_{load} = \frac{Q_G}{V_{GS}} \quad (3)$$

In MOSFET datasheets Q_G is usually provided in the gate charge characteristics, a graph showing the dependence of gate-to-source charge voltage on gate charge; an example is given in **Figure 7** for a specific Infineon OptiMOS™.

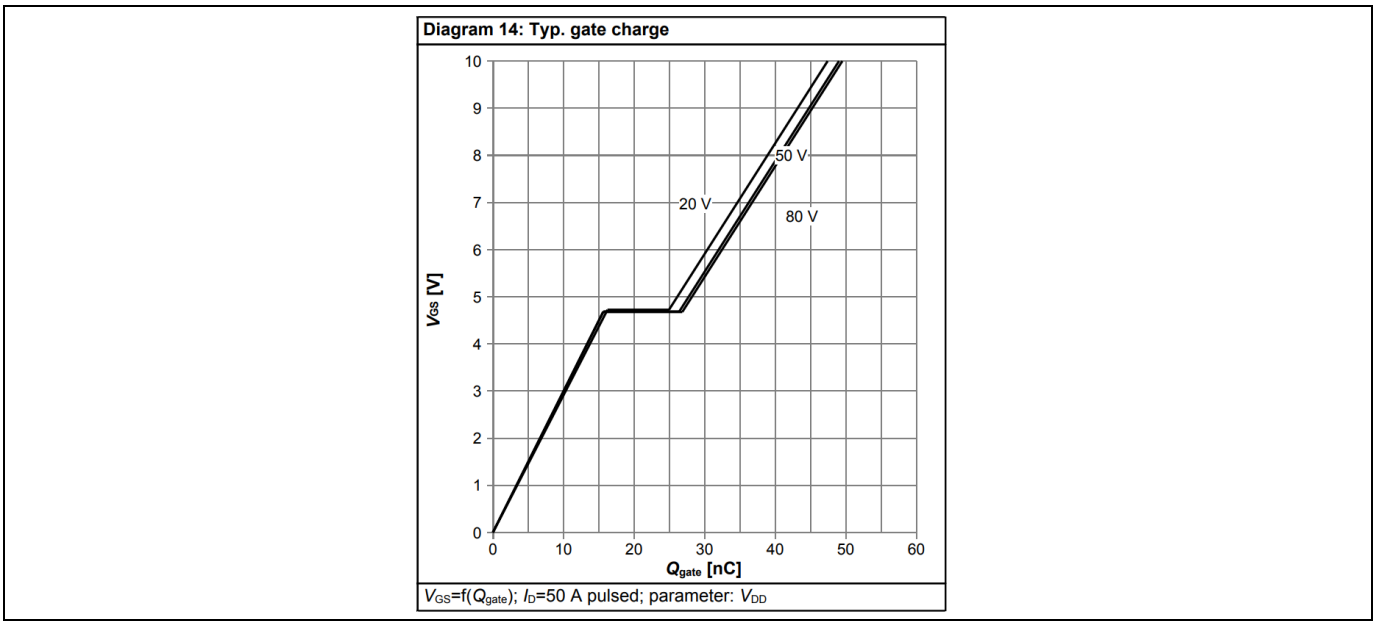

Figure 7 Typical gate charge characteristic of OptiMOS™ BSC050N10NS5

A reasonable output supply voltage ripple below 5 percent would then, from equation (4), result in:

$$\frac{\Delta V}{V_{DDA}} < 5\% \rightarrow \quad C_{out} > 19\, C_{load} \tag{4}$$

A proper dimensioning thus requires you to choose an output bypass capacitance which is at least 20 times larger than the equivalent input capacitance of the MOSFET; a range from 100 nF or 1 µF is common when driving Infineon OptiMOS™ devices. As for the input bypass capacitance, it is suggested to use a ceramic capacitor in SMD 0805 package with 25 V DC voltage rating.

2.3 Bootstrap circuit dimensioning

Bootstrapping is a very cost effective method to create the floating supply voltage for driving HS power MOSFETs in half-bridge topologies.

The bootstrap circuit is highlighted in **Figure 8** and is made up of three components: bootstrap capacitor (C_B), bootstrap resistor (R_B) and fast recovery diode (D_B).

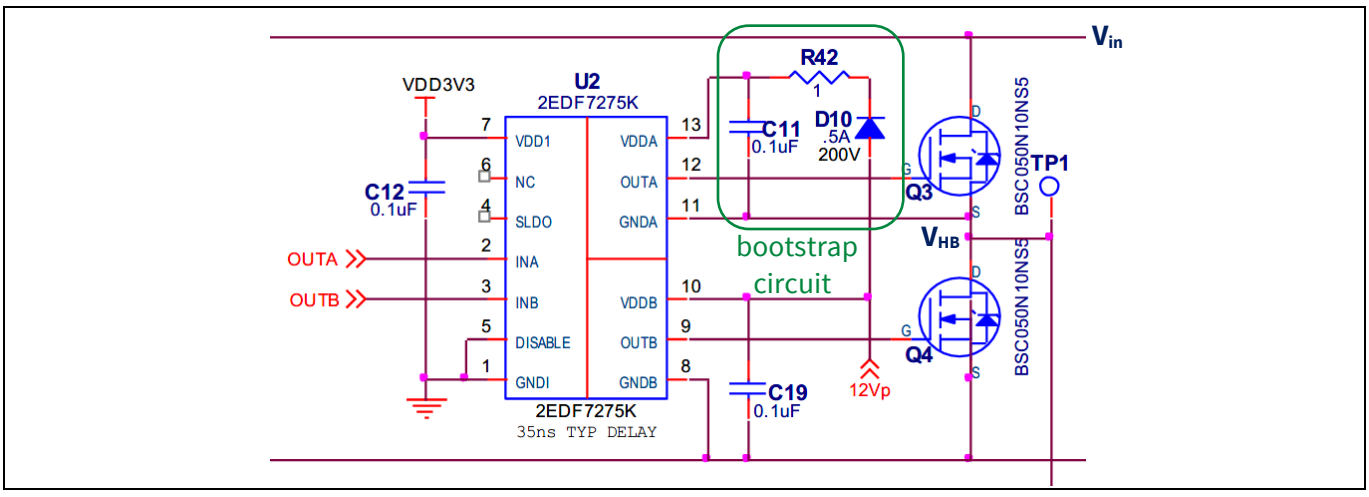

Figure 8 Bootstrap circuit to generate the HV floating supply

The bootstrap circuit operation is defined by two main periods:

- **Charging period**: capacitor C_B is charged while the LS switch is on and the HS switch is off. When the LS MOSFET is on, the diode D_B is forward-biased ($V_{HB} \cong 0$ V) and the current flows from the isolated LS voltage source VDDB (+ 12 V) into C_B through the bootstrap resistor R_B, diode D_B, and the LS switch that finally closes the loop to ground. Simultaneously, the necessary quiescent current ($I_{VDDAqu2}$) is supplied to the driver.
- **Sourcing period**: when the LS switch is turned off and/or the HS switch starts conducting, the source voltage of the HS switch (V_{HB}) quickly rises until it approaches the HB supply voltage (V_{in}). As a consequence, the bootstrap diode D_B gets reverse biased and disconnects the ground supply from C_B. The capacitor C_B must be dimensioned to store the required energy to keep the HS switch on until the next commutation; in this way, a supply voltage of V_{in} + VDDA (+ 12 V) is ensured during the sourcing period for proper HS MOSFET driving.

The bootstrap circuit requires careful design to ensure robust and safe operation. More specifically, the charging period must be sufficiently large to charge C_B, and the ripple on the supply voltage due to C_B discharge during the sourcing period must fulfill the specifications (e.g., 5 percent maximum ripple).

Additional discharge situations must be also taken in account; burst mode in particular is critical from the C_B dimensioning point of view. Burst mode is characterized by extended non-switching times with duration t_{SKIP} (e.g., 1 ms) during low-load operation. The driver quiescent current discharges the capacitance C_B during t_{SKIP}; the risk is that, for very long t_{SKIP}, C_B is discharged below the UVLO level of the driver. The dimensioning of C_B, based on burst mode consideration, is then more restrictive than normal PWM mode operation to avoid any false triggering of UVLO.

The dimensioning of C_B must guarantee a voltage ripple (ΔV_{CB}) within specifications; ΔV_{CB} depends on the charge Q_{CB} that has to be provided by C_B as follows:

$$\Delta V_{CB} = \frac{Q_{CB}}{C_B} \tag{5}$$

C_B can thus be dimensioned by calculating the charge Q_{CB} and considering the limitation on the maximum ripple ΔV_{CB}.

During normal PWM mode, the Q_{CB} is given by the gate charge Q_g transferred in order to turn-on the HS MOSFET and the quiescent current drawn by the driver during the sourcing period. The worst case in terms of C_B discharge has to be considered: longest sourcing period and maximum HS MOSFET duty cycle (D_{MAX}):

$$Q_{CB} = Q_g + D_{MAX} \times I_{\mathrm{VDDAqu2}} \frac{1}{F_{PWM}} \tag{6}$$

In systems with burst mode operation at low-load, the discharging during t_{SKIP} must be considered by adding the term ($I_{\mathrm{VDDAqu2}} \times t_{\mathrm{SKIP}}$) to (6).

The capacitor C_B is defined by the maximum ripple ΔV_{CB}. A common criterion is to accept a maximum ripple of 5 percent of VDD. Considering burst mode operation, the dimensioning is more critical and must always guarantee a supply voltage above the driver UVLO level.

The value of the bootstrap resistor R_B can be determined from the requirement to ensure full charge of C_B during the charging period. Assiming five times constants as a proper duration for full charging:

$$\mathrm{t_{min}} = \frac{(1 - \mathrm{D_{MAX}})}{\mathrm{f_{PWM}}} \geq 5\ \mathrm{R_B\ C_B} \tag{7}$$

Then the equation for R_B design results as follows:

$$R_B \leq \frac{1 - D_{MAX}}{5 \times C_B \times f_{PWM}} \quad (8)$$

After dimensioning of C_B and R_B, the selection of the proper bootstrap diode D_B can follow. D_B should have a current rating ($I_{F(AV)}$) greater than or equal to $I_{AV,max}$:

$$I_{AV,max} = \frac{Q_{CB}}{1 - D_{MAX}} \times f_{PWM} \quad (9)$$

$I_{AV,max}$ is the maximum average current through the diode; the largest value is given by the shortest charging period.

The voltage rating of D_B must be sufficiently high to block V_{in} during the sourcing period. Finally, the diode must have a sufficiently fast reverse recovery time to avoid that its reverse current discharges the capacitor C_B.

2.4 PCB layout recommendations

The impact of PCB parasitics is particularly critical in fast-switching power systems and requires a proper layout. Therefore, the designer must pay attention to the PCB layout in order to achieve optimum performance when using the EiceDRIVER™ **2EDF7275K**. **Figure 9** provides a layout recommendation for a two-layer PCB and a bootstrap circuit to supply the HS output channel.

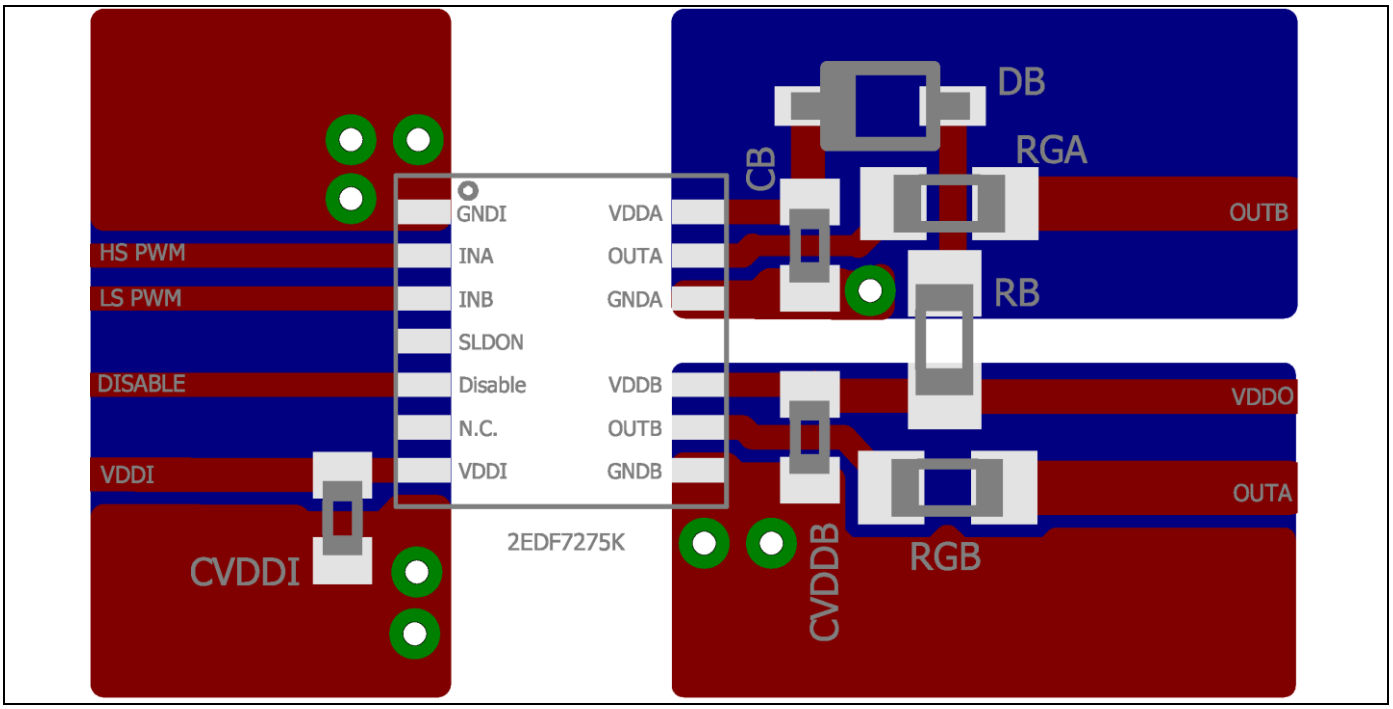

Figure 9 Layout recommendation for the EiceDRIVER™ 2EDF7275K

The following tips are to optimize the layout of a gate driving circuit using the **2EDF7275K**:

- Use low-ESR and low-ESL decoupling capacitors for each input (VDDI) and output (VDDA, VDDB) supply and place it as close as possible to the driver IC to bypass noise and support high peak output currents.
- Place the driver IC and the gate resistor[2] as close as possible to the power MOSFET in order to minimize the gate loop inductance and the noise on the gate terminals of the transistors.

[2] In telecom bricks, it's usual to avoid the gate resistor in order to speed up the switching transitions and obtain the highest efficiency.

- Minimize the high-current path of the bootstrap circuit (bootstrap capacitor, bootstrap diode, bypass capacitor of the LS channel, and the LS transistor/diode) to ensure reliable operation in particular during the short recharging time intervals that are associated with a high peak current.
- To ensure a proper input-to-output isolation, no PCB traces or copper should be placed below the driver IC in the area between the input and output pins.
- To minimize cross-talk between the HS and LS output channels due to parasitic coupling to the switching node, the space between the two PCB planes of the output channels should be maximized.
- In a PCB with more than two layers, it is recommended to connect the output power and ground pins (VDDA, VDDB, GNDA and GNDB) to internal ground or power planes through vias of adequate size; several vias in parallel can be used to reduce the resistance of connections.
- Use GND planes to reduce the parasitic inductance of ground connections.

3 Evaluation board

A 600 W QB 48 V to 12 V FB-FB rectifier evaluation board is used as an application example for the EiceDRIVER™ **2EDF7275K** dual-channel isolated gate driver IC. In this section, the specifications for the converter along with the schematic and board layout will be presented. To enable practical access to the evaluation board, the QB is mounted on a test fixture that will also be described later on. A GUI design tool is available to make the controller reconfiguration process easier for the designers and programmers. This tool enables changing of the dead-time settings, which will be then used in section 4 to assess their impact on the efficiency.

3.1 Specifications

The specifications of the 600 W QB FB-FB evaluation board are listed in Table 2.

Table 2 Specifications of the evaluation board

Parameter	Value
Input voltage range, V_{in_range}	36 to 75 V DC
Nominal input voltage, V_{in}	48 V DC
Maximum peak input current, I_{in_max}	16 A at P_{out} and V_{in} = 42 V DC
Isolation voltage	1500 V
Nominal output voltage, V_{out}	12 V DC at V_{in} = 42 V to 75 V DC
Maximum output current, I_{out_max}	50 A
Maximum output power, P_{out}	600 W
Output voltage ripple (max. peak to peak)	240 mV_{pk-pk} at P_{out}
Recommended output capacitor	1000 to 10000 µF
Switching frequency	250 kHz
Efficiency at 48 V, half load	95.5 percent
Operating temperature (ambient)	-40°C to 80°C

3.2 Schematic

Figure 10 shows the schematic of the power stage of the 600 W 12 V/50 A QB FB-FB converter. Primary power MOSFETs are Infineon's OptiMOS™ 100 V/5 mΩ **BSC050N10NS5** in SuperSO8 package. The secondary synchronous rectifier uses two OptiMOS™ 40 V/1 mΩ **BSC010N04LS6** in parallel for each switch, also in SuperSO8 package.

Both primary and secondary OptiMOS™ power MOSFETs are driven by Infineon's EiceDRIVER™ **2EDF7275K** dual-channel isolated gate driver. As described in section 2, the **2EDF7275K** provides 4 A/8 A source/sink current capability combined with very low impedance output stages and highly accurate timing over both temperature and production. The gate driving circuit for the synchronous rectifier does not require galvanic isolation since the controller is on the secondary side. However, the **2EDF7275K** is also used in this stage to simplify the BOM and ensure a perfect propagation delay matching between the two FBs.

A planar transformer with a turns ratio of 3:1 is used to achieve the lowest board profile; this transformer is based on the core ML95S EQ25 + plate from Hitachi Metals.

An Infineon-designed Capacitor-Diode-inductor Lossless (CDL) resonant clamp snubber is used on the secondary-side FB.

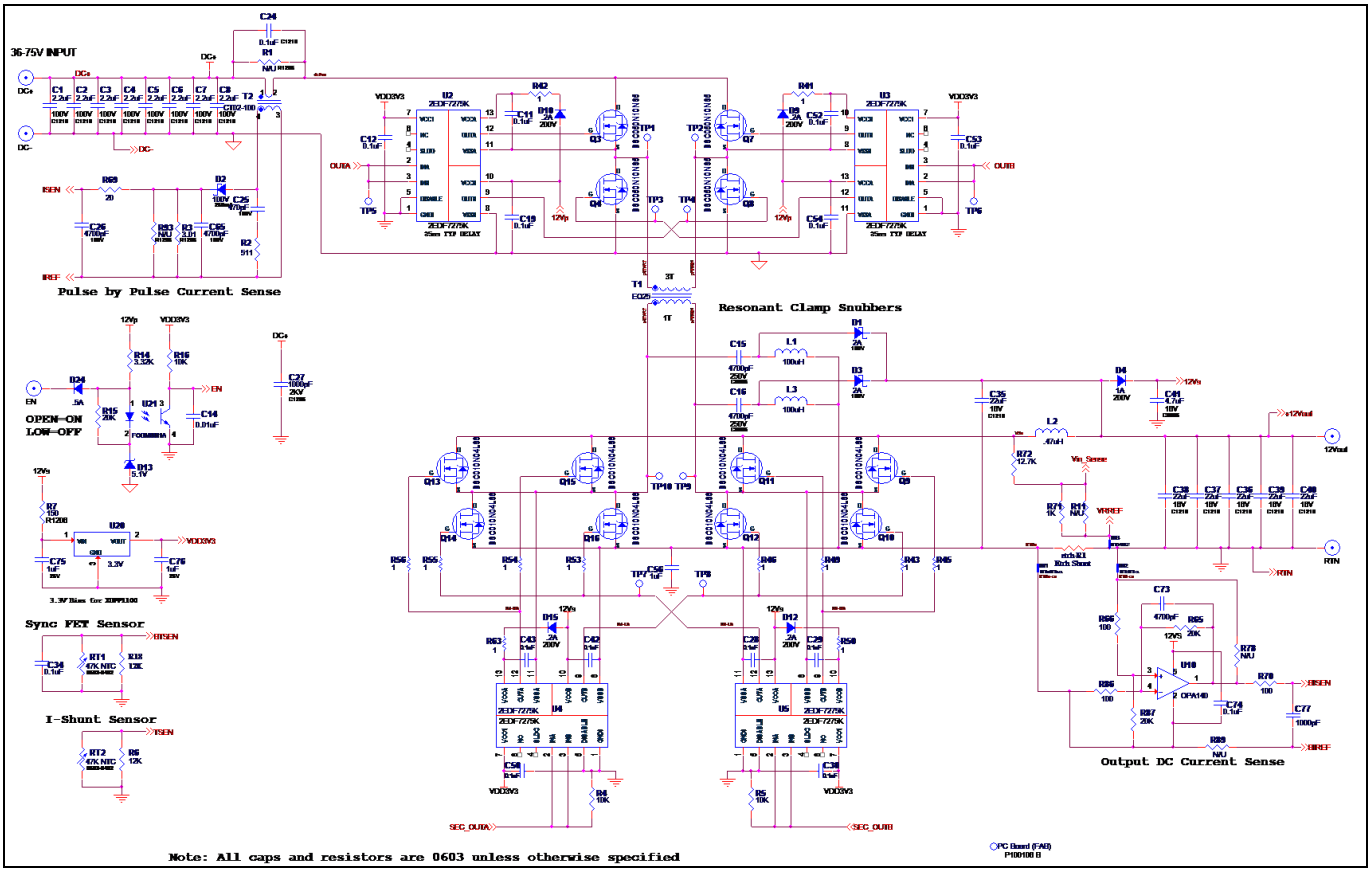

Figure 10 600 W 12 V/50 A QB FB-FB power stage schematic

As already shown in **Figure 1**, the XDPP1100 [4, 5] digital controller sits on the secondary side and generates the PWM signals for all the power MOSFETs. It is a digital power supply controller based on a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microprocessor with analog/mixed-signal capabilities, on-chip memories and communication peripherals. The device is specifically optimized to enhance the performance of isolated DC-DC applications and to reduce the solution component count in telecom brick converters. XDPP1100 supports up to two high-speed digital control loops. Each loop consists of a dedicated Voltage Analog-to-Digital Converter (VADC), high-resolution current ADC (IADC), a PID-based digital compensator, and DPWM outputs with 78.125 ps pulse-width resolution. The device also offers six channels of 9-bit, 1 Msps general-purpose ADCs (TS ADCs), timers, interrupt control, PMBus and I^2C communication ports.

3.3 Board layout and the test fixture

In order to enable practical access to the evaluation board, the QB is mounted on a test fixture, as can be seen in **Figure 11**.

The test fixture provides power connection terminals, PMBus and I^2C communication and debugging ports, as well as a cooling fan. The fan should be biased with external DC power supply, in the 5 V to 12 V range for different air flow levels. A 3.3 V LDO regulator on the test fixture provides pull-up voltage to the SDA/SCL I^2C communication bus.

The XDPP1100 controller, the primary MOSFETs and the SR MOSFETs are mounted on the top layer of the QB PCB. The EiceDRIVER™ **2EDF7275K** gate driver ICs and the output inductor are assembled on the bottom layer of the PCB. The planar transformer is built using all 10 PCB layers. For more details, please refer to [2].

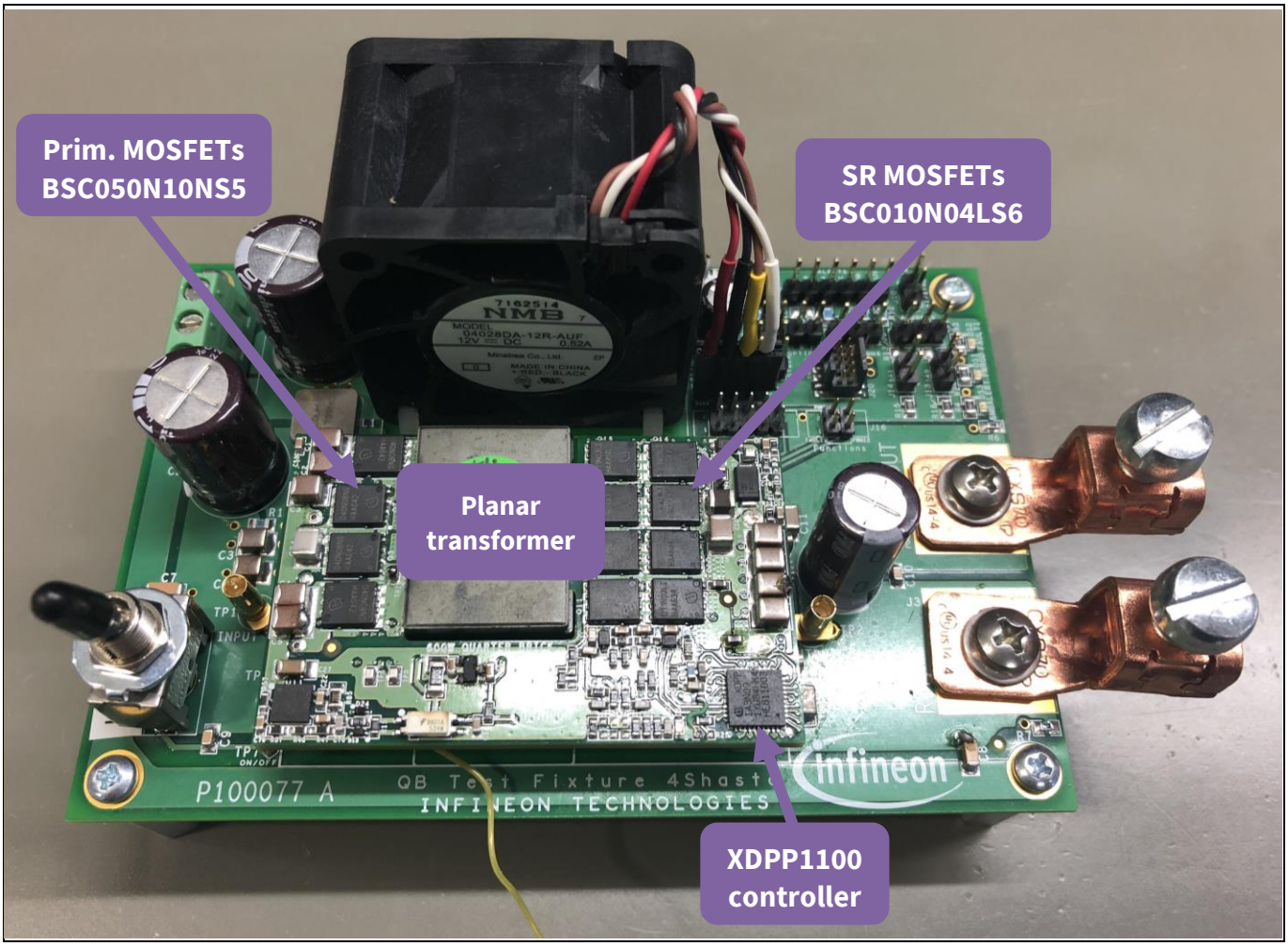

Figure 11 600 W 12 V/50 A QB FB-FB evaluation board mounted on the test fixture; the four EiceDRIVER™ 2EDF7275K are mounted on the bottom side of the QB

3.4 GUI design tool

The XDPP1100 controller can be used in a broad range of applications. Several topologies are supported, such as HB and FB center-tapped converter, FB converter with FB rectification (FB-FB), Active Clamp Forward (ACF) converter, HB converter with current doubler, buck, boost, and inverted buck-boost converter. In order to enable all this flexibility, a Graphical User Interface (GUI) is available to make the controller reconfiguration process easier for the designers and programmers. **Figure 12** shows the design tools available in the GUI. Dead-time can be set in the Device Topology tool. As can be seen in the right-hand picture, dead-time can be configured separately and added to the rising edge and/or falling edge of the PWM signal. The maximum dead-time can be set to 318.75 ns with a resolution of 1.25 ns. As described in section 1, for this QB FB-FB evaluation board, the dead-time is set by adding a delay to the rising edge of each PWM signal.

When setting the dead-times, the propagation delay that will be added by the gate driver or digital isolator to transmit the signals across the isolation barrier should be taken in account and defined in the “Isolation delay” field. If not, the whole waveforms on the primary side will be shifted to the right (delayed), which can provoke very large primary-side currents and consequent failure of the power MOSFETs. In this evaluation board, since we are using the same gate drivers on both the primary and secondary sides, this is not a problem, and perfect propagation delay matching is ensured by the EiceDRIVER™ **2EDF7275K**.

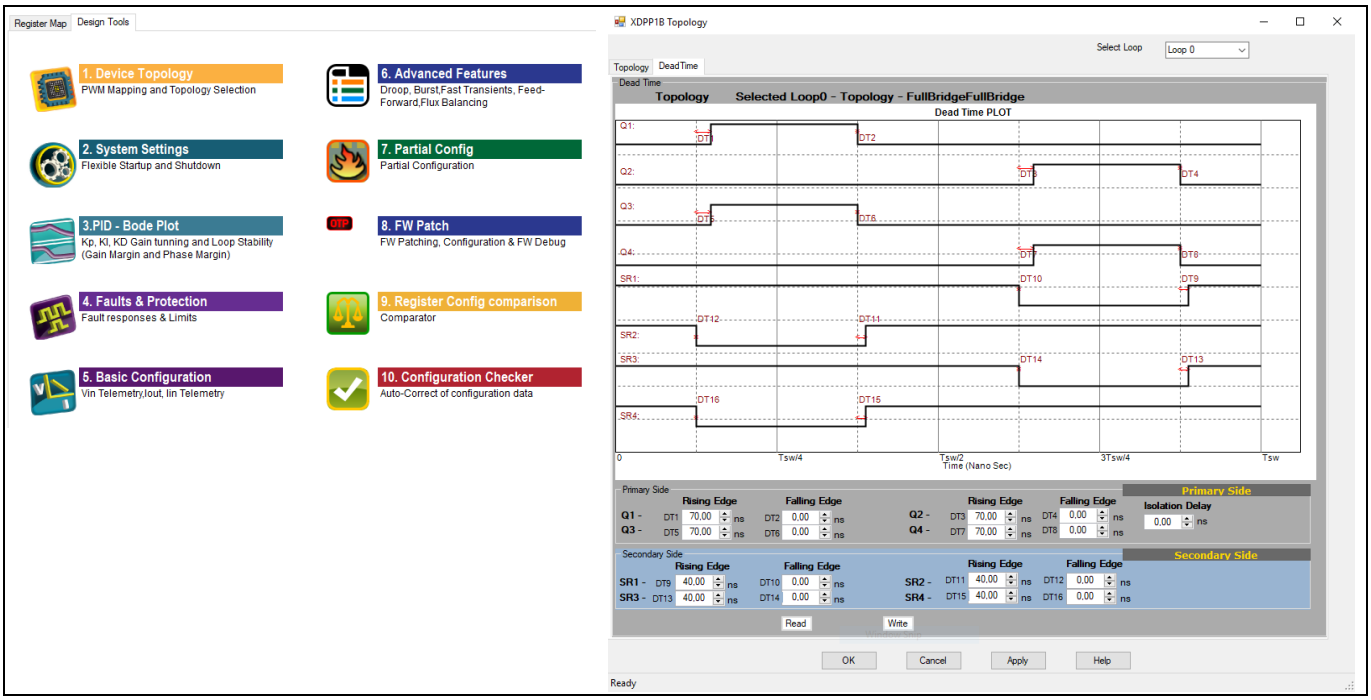

Figure 12 GUI design tool and dead-time settings

4 Performance measurement results

The evaluation board was tested to assess the performance in terms of efficiency for different dead-time settings. The purpose is to compare the impact of different propagation delay variance and propagation delay mismatch between output channels on the conversion efficiency.

4.1 Gate driver input-to-output propagation delay

According to the EiceDRIVER™ **2EDF7275K** specifications [9], the input-to-output propagation delay is in the range from 31 ns to 44 ns, with 37 ns being the nominal value. **Figure 13** shows the measurements of the time difference between the PWM input and the gate driver output during turn-on and turn-off transitions. Figures 13 (a) and (b) illustrate the input-to-output propagation delay measurement for transistor Q8 during turn-off and turn-on transitions, respectively. Figures 13 (c) and (d) show the input-to-output propagation delay measurement for transistor Q14 for turn-off and turn-on transitions, respectively. As expected, the input-to-output propagation delay is within the specified range and with 37 ns as a typical value.

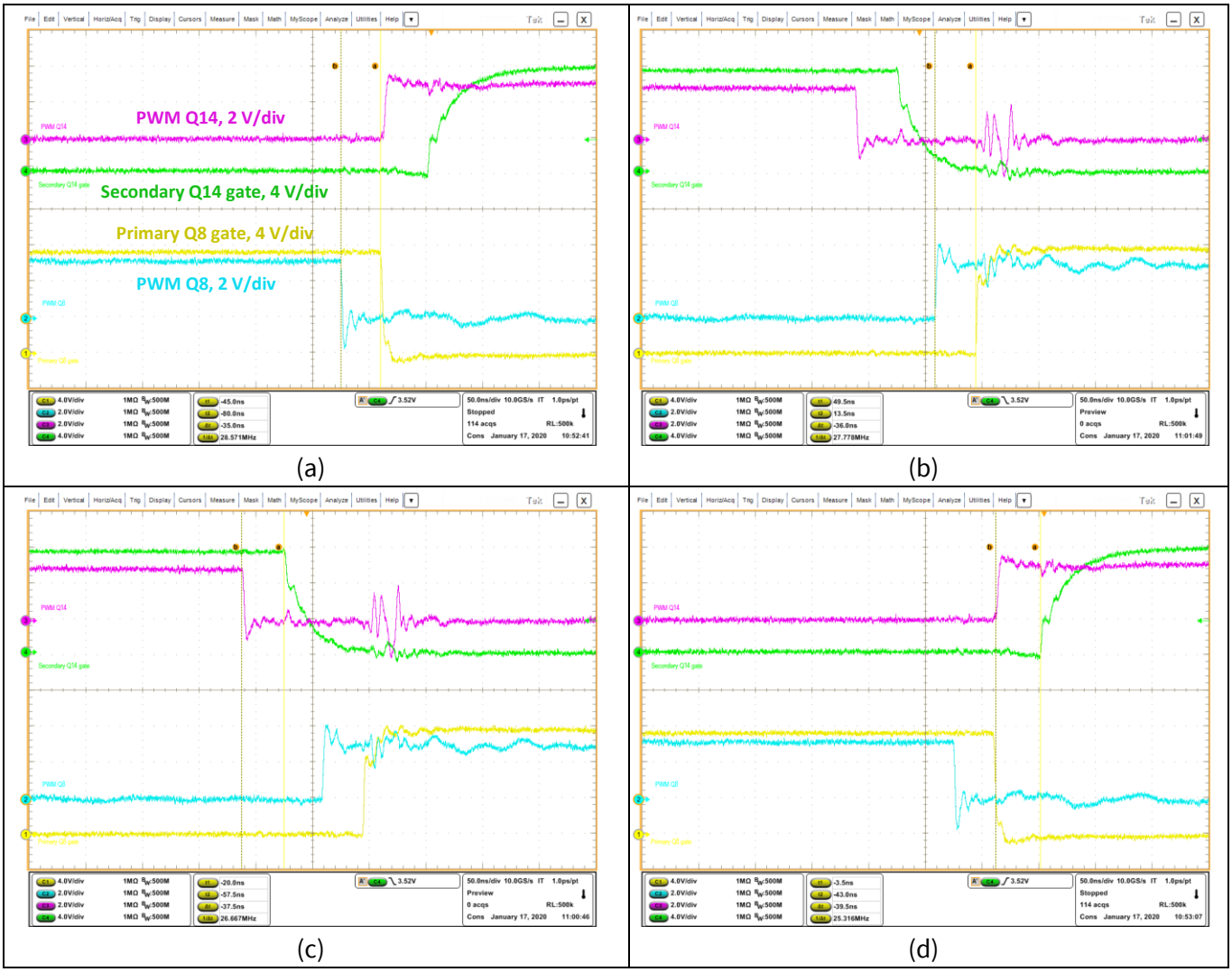

Figure 13 Gate driver input-to-output propagation delay

4.2 Modulation and dead-time setting

The gate voltages (V_{gs}) were measured to show the modulation period and the dead-time setting between the primary- and secondary-side power MOSFETs. Figures 14 (a) and (b) show, respectively, two cycles and one cycle of the modulation period. For this operating condition with 48 V input and 25 A load, the duty-cycle D/2 is around 37 percent. By comparing with Figure 3, it is clear that the PWM signals of the primary-side FB are also not overlapping the Synchronous Rectifier (SR) waveforms. As can be seen in Figures 14 (c) and (d), the dead-time between the SR gate and the diagonal primary gate is minimized to 70 ns, while the dead-time between the primary gate and the respective diagonal SR gate is minimized to 40 ns in order to achieve the best efficiency.

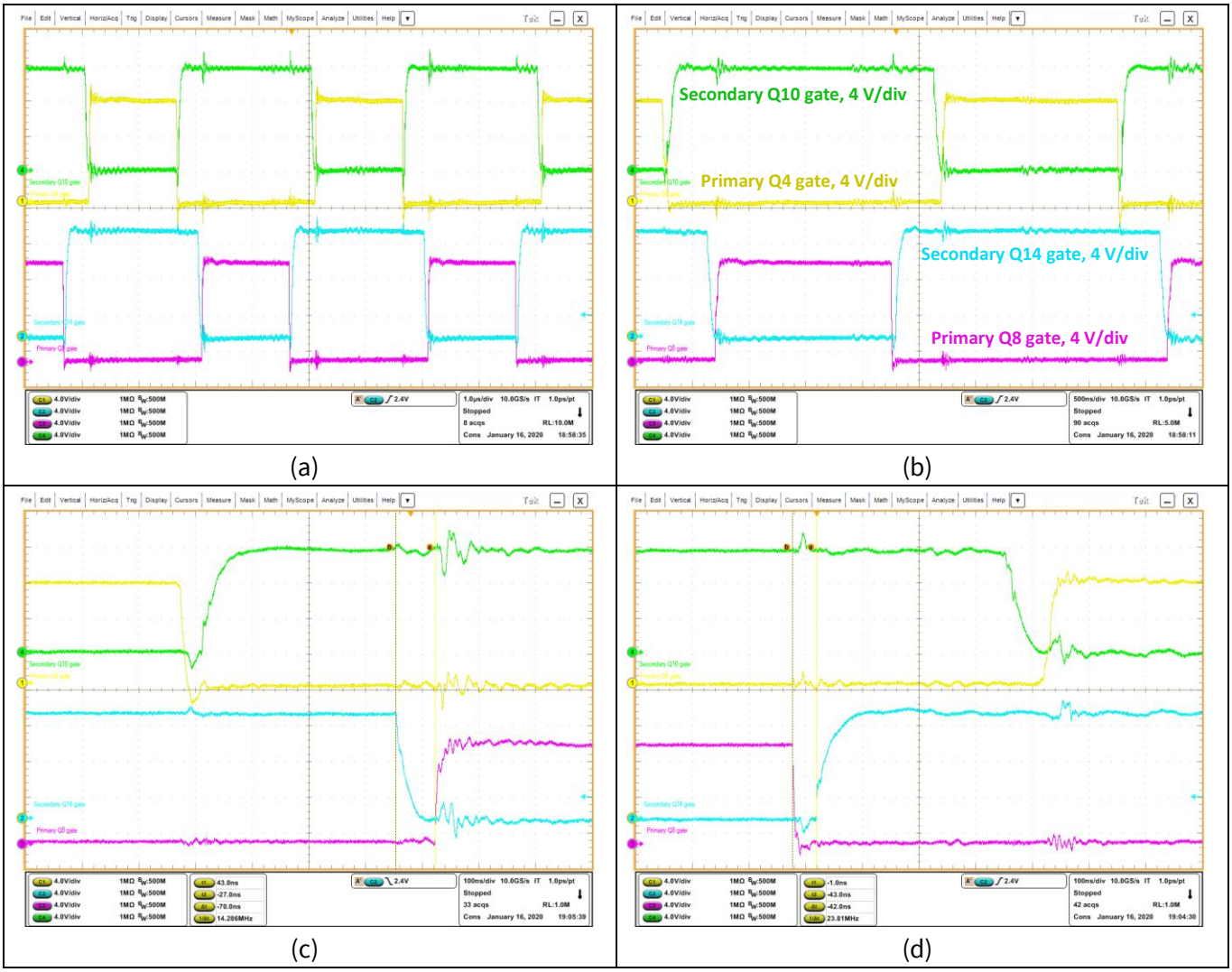

Figure 14 Primary- and secondary-side gate voltages at 48 V input and 25 A load

4.3 Efficiency

Different factors can affect the conversion efficiency by having an impact on the switching losses and/or conduction losses of the power MOSFETs. As discussed in section 1.3, tight propagation delays enable dead-time reduction, which improves efficiency by increasing the effective power transfer period. The gate driver IC plays a key role in terms of possible dead-time optimization. As shown in Table 1, the EiceDRIVER™ **2EDF7275K** has a better timing accuracy when compared with the next best competitor alternatives.

When defining the dead-time between the primary- and secondary-side full-bridges (please refer to **Figure 3**), the input-to-output turn-on and turn-off propagation delay must be considered. These parameters are commonly specified in the datasheet as t_{PDon} or t_{PDLH} for the turn-on, and as t_{PDoff} or t_{PDHL} for the turn-off transition. The propagation delay mismatch between output channels Δt_{PD} must also be taken into account. The propagation delay spread can be determined simply by calculating the difference between the maximum and the minimum value specified in the datasheet for the input-to-output propagation delay and then adding the propagation delay mismatch between output channels. For example, the EiceDRIVER™ **2EDF7275K** has a maximum t_{PDon} of 44 ns and a minimum of 31 ns; the maximum Δt_{PD} is 3 ns; thus, the propagation delay spread corresponds to 16 ns. The same exercise can also be done for the other gate driver ICs listed in Table 1. The additional propagation delay spread of the competitor drivers compared with the **2EDF7275K** is listed in the last column of Table 3. Considering the optimized dead-times presented in section 4.2, with DT1 = 70 ns and DT2 = 40 ns, this can be used as the reference configuration setting for the efficiency measurement with the EiceDRIVER™ **2EDF7275K** (Config_A). Table 3 also shows the dead-time configuration settings Config_B to Config_E used for the efficiency measurements considering the propagation delay spread of the next best alternative gate driver ICs from competition listed in Table 1, Competitor_B to Competitor_E, respectively.

Table 3 Dead-time configuration settings for the efficiency measurements

Configuration	DT1	DT2	Difference to Config_A
Config_A	70 ns	40 ns	-
Config_B	75 ns	45 ns	+ 5 ns
Config_C	79 ns	49 ns	+ 9 ns
Config_D	101 ns	71 ns	+ 31 ns
Config_E	108 ns	78 ns	+ 38 ns

The evaluation board was tested in order to measure the efficiency for the different dead-time configuration settings. The purpose is to compare the impact of the propagation delay variance and propagation delay mismatch between output channels on the conversion efficiency. The volt-second-based flux balancing algorithm implemented in the XDPP1100 digital controller was deactivated during the efficiency measurements.

Test conditions:

- Automatized test bench with measurement inaccuracy less than 0.1 percent for output current greater than or equal to 15 A
- Output voltage is measured at the power pin 12 V_{out} and RTN of the brick to exclude voltage drop loss due to contact resistance
- Fan is supplied externally with 7.5 V; the consumption is not included in the measurements
- Room temperature between 25.5°C and 26.5°C
- 5 minutes' Equipment Under Test (EUT) warm-up and 2 minutes' interval between acquisitions

Table 4 shows the efficiency measurement results of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input voltage for the different dead-time configuration settings. These results are also plotted in **Figure 15**. As expected, Config_A provides the best efficiency results due to smaller dead-times when compared with the other configuration settings. The peak efficiency of 95.6 percent is obtained in the 60 percent to 70 percent load range, and the efficiency stays above 95 percent from 40 percent up to full load.

Figure 16 represents the differential efficiency measurement, taking Config_A (EiceDRIVER™ **2EDF7275K**) as a reference. It is clear that the dead-time has a higher impact in the low to mid load range, but it affects the

efficiency in the whole load range. From curve Config_E, it can be concluded that the efficiency is reduced by 0.27 percent in the 30 percent to 45 percent load range due to the higher propagation delay variance and propagation delay mismatch between output channels of the Competitor E gate driver IC. Furthermore, an efficiency improvement of at least 0.2 percent in the whole load range can be obtained simply by using the **2EDF7275K** instead of the competitor gate driver IC, due to better timing accuracy over both temperature and production.

Table 4 Efficiency measurement of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input for the different dead-time configuration settings

Output current (A)	Efficiency (%)				
	Config_A	Config_B	Config_C	Config_D	Config_E
15	94.25	94.22	94.19	94.04	93.98
20	95.09	95.05	95.02	94.86	94.82
25	95.45	95.42	95.38	95.22	95.19
30	95.61	95.58	95.55	95.40	95.36
35	95.60	95.56	95.54	95.39	95.35
40	95.47	95.44	95.41	95.28	95.24
45	95.29	95.26	95.22	95.11	95.07
50	95.06	95.03	95.00	94.88	94.85

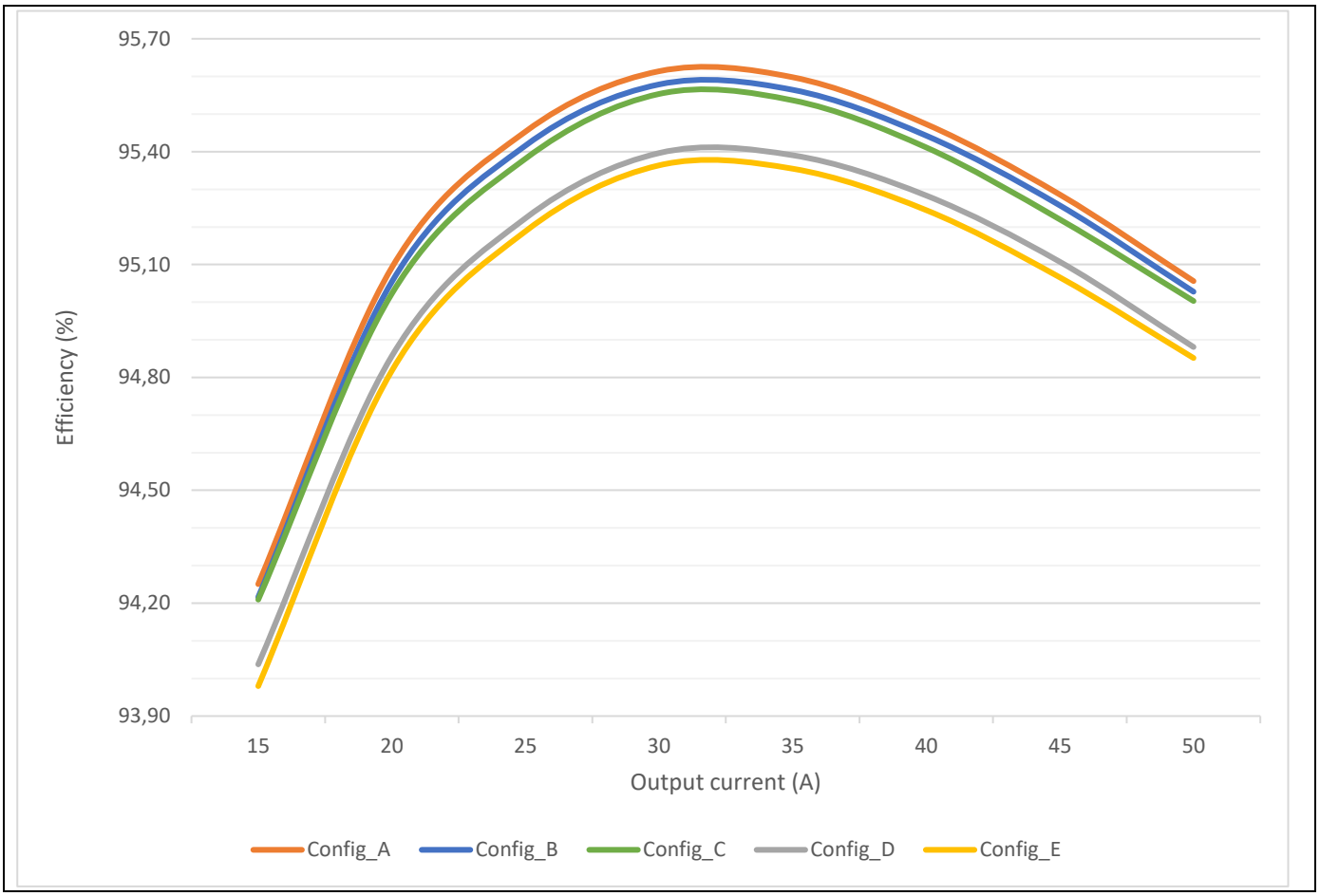

Figure 15 Efficiency measurement of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input voltage for the different dead-time configuration settings

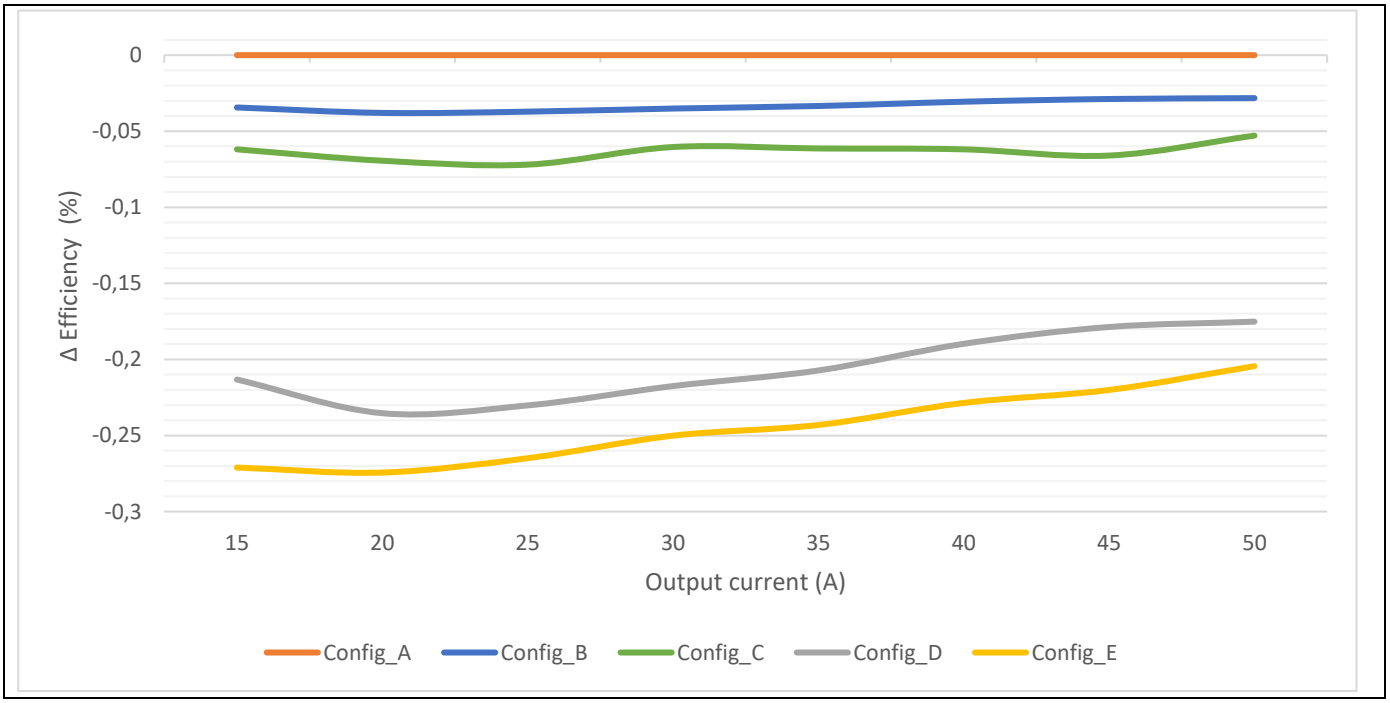

Figure 16 Differential efficiency measurement of the 600 W QB 48 V to 12 V FB-FB evaluation board at 48 V DC input voltage for the different dead-time configuration settings

5 Summary

The dual-channel isolated EiceDRIVER™ **2EDF7275K** is well suited to increasing the system efficiency, power density and robustness of DC-DC converters in telecom bricks. The 4 A/8 A source/sink output currents, combined with a low 37 ns propagation delay and the highly accurate timing over both temperature and production, are the perfect fit for high-frequency PWM control with tightest possible dead-time windows, delivering highest conversion efficiency. Furthermore, since the source/sink output resistance is significantly lower than the competition, it enables this driver to run cooler due to less undesired power dissipation in the IC. This dual-channel isolated gate driver IC is available in a small form-factor LGA-13 5 mm x 5 mm package, which enables significant PCB area saving in high-density DC-DC converters. The efficiency improvement by reducing the dead-times due to better timing accuracy are demonstrated using a 600 W QB 48 V to 12 V FB-FB rectifier evaluation board. An efficiency improvement of at least 0.2 percent in the whole load range and 0.27 percent peak efficiency increase can be obtained simply by using the EiceDRIVER™ **2EDF7275K** instead of one of the competitor gate driver ICs, due to better timing accuracy over both temperature and production.

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