Quick-reference guide to driving CoolGaN™ GIT HEMTs 600 V

RC interface

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About this document

Scope and purpose

This application note introduces the RC interface configuration for Infineon CoolGaN™ gate injection high electron mobility transistor (GIT HEMT) 600 V gate driving. First a brief introduction of Infineon’s CoolGaN™ GIT HEMT 600 V ohmic p-GaN structure and typical driving circuit is given. By using a dedicated/standard gate driver, CoolGaN™ GIT HEMTs can be driven easily through the RC interface. A step-by-step RC interface tuning guide is then given. Finally, typical RC interface configuration values are given in the form of look-up tables for different slew-rate requirements and target applications.

This application note is intended to be used as a quick-reference guide for RC interface design in driving Infineon CoolGaN™ GIT HEMTs (Figure 1). For a more in-depth explanation of the driving mechanism, please refer to Driving CoolGaN™ GIT HEMT 600 V high electron mobility transistors [1]. In addition, to get more insights on the gate drive requirements and driving solutions for CoolGaN™ GIT HEMTs, check out the available Whitepaper [4].

Figure 1  CoolGaN™ GIT HEMTs and CoolGaN™ IPS products

Intended audience

This application note is mainly targeted at application engineers and circuit designers using CoolGaN™ GIT HEMTs 600 V [2] and CoolGaN™ Integrated Power Stage (IPS) [3].
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What are CoolGaN™ GIT HEMT and RC interface?

1 What are CoolGaN™ GIT HEMT and RC interface?

Infineon’s CoolGaN™ GIT HEMT is a highly efficient GaN transistor technology for power conversion in the voltage range up to 600 V. CoolGaN™ GIT HEMT 600 V adopts an ohmic p-GaN gate structure. Relevant advantages of this construction include:

Positive gate threshold voltage

CoolGaN™ GIT HEMT is a normally-off device, and its improved figure of merit (FOM) makes it an ideal replacement for a silicon MOSFET in SMPS applications.

Robust and reliable gate drive

CoolGaN™ GIT HEMTs have diode-like input characteristics. This provides voltage clamp and helps avoid any overvoltage damage to the transistor gate.

Highly stable $\text{R}_{\text{DS(on)}}$ over drain current

During the CoolGaN™ GIT HEMT on-state, constant gate current enables independence of $\text{R}_{\text{DS(on)}}$ over drain current.

Although CoolGaN™ GIT HEMTs are robust enhancement mode devices, their gate module differs from a MOSFET, which behaves like a diode with a forward voltage $V_F$ of 3 to 4 V. Therefore, a continuous gate current $I_{ss}$ of a few mA is needed during the steady on-state, and high gate charging currents $I_{on}$ and $I_{off}$ up to 1 A are needed for fast-switching transients. Since the switch is normally-off with a low threshold voltage $V_{th}$ around 1.2 V, a negative gate bias during the off-state is needed to prevent false gate triggering in hard-switching applications.

To avoid a dedicated driver with two separate on-paths and bipolar supply voltage, the RC interface is the gate drive circuit recommended by Infineon for CoolGaN™ GIT HEMTs 600 V GIT, which is shown in Figure 2.

Three components in the RC interface are included in the gating circuit:

$R_{ss}$: steady-state gate current tuning resistor

$R_{tr}$: transient switching speed $\text{dv/dt}$ tuning resistor

$C_C$: coupling capacitor as charge pump to provide fast-switching transient as well as negative gate bias

![Figure 2 Typical gate drive RC interface for Infineon CoolGaN™ GIT HEMT 600 V](image-url)
2 RC interface advantages

Key advantages of the RC interface scheme include:

Ease of use

Negative gate voltage can be directly tuned with the RC interface configuration. No level-shift circuit is needed in the gate driver. The RC interface is compatible with dedicated/standard gate drivers.

Controllable dv/dt transient control

Turn-on/-off speed, on-state gate current and off-state reverse gate bias voltage are controllable thanks to the RC interface, which can be fine-tuned for EMI control, common-mode noise reduction and motor-drive applications.

Efficient drive

Negative gate bias is gradually discharged after the turn-off transient, which is beneficial for power loss reduction during operation in the third quadrant.

The typical gating waveform of the Infineon RC interface and piecewise analysis of the gating procedure of CoolGaN™ GIT HEMTs are given in Figure 3 and Figure 4 respectively. During the gate-on transient, the fast-charging path is formed by Rr and Cc. After that, constant current is injected into the CoolGaN™ GIT HEMT gate through Rr during the transistor steady on-state. During the gate-off transient, gate charge is discharged through Rr and Cc. During the off-state, charge stored in the coupling capacitor Cc is gradually discharged, which contributes to negative gate voltage -Vn and then gradually decreases to -Vnf.

![Figure 3](image3.png)

**Figure 3** Typical gate voltage of CoolGaN™ GIT HEMT

![Figure 4](image4.png)

**Figure 4** Typical gating procedure of CoolGaN™ GIT HEMTs
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RC interface

Tuning the RC interface

3 Tuning the RC interface

3.1 General tuning rules

\( R_{\text{ss}} \) tuning

\( R_{\text{ss}} \) is tuned according to gate voltage \( V_{\text{DD}} \), gate diode forward voltage drop \( V_F \) (3~4 V), and desired on-state gate current \( I_{\text{ss}} \). Reference \( R_{\text{ss}} \) selection in different \( R_{\text{DS(on)}} \) devices is given in Table 1.

It should be noted that reference \( I_{\text{ss}} \) and \( R_{\text{ss}} \) values are given to maintain the device at low \( R_{\text{DS(on)}} \) in typical applications. In low source current applications, dependence of device \( R_{\text{DS(on)}} \) on \( I_{\text{ss}} \) is low. In this case, a higher \( R_{\text{ss}} \) value can be chosen to lower gate driver loss and achieve higher overall efficiency. In high source current applications, a lower \( R_{\text{ss}} \) value should be used to maintain the device at the lowest \( R_{\text{DS(on)}} \).

Please always refer to typical drain-source on-resistance curve in the CoolGaN™ GIT HEMT and CoolGaN™ IPS product datasheet for fine-tuning in different source current use cases.

\[
I_{\text{ss}} = \frac{V_{\text{DD}} - V_F}{R_{\text{ss}}}
\]  

(1)

<table>
<thead>
<tr>
<th>( R_{\text{DS(on,typ)}} )</th>
<th>55 mΩ</th>
<th>100 mΩ</th>
<th>140 mΩ</th>
<th>200 mΩ</th>
<th>270 mΩ</th>
<th>500 mΩ</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{DS(on,max)}} )</td>
<td>70 mΩ</td>
<td>130 mΩ</td>
<td>190 mΩ</td>
<td>260 mΩ</td>
<td>340 mΩ</td>
<td>650 mΩ</td>
</tr>
<tr>
<td>Reference ( I_{\text{ss}} )</td>
<td>10~12 mA</td>
<td>5~6 mA</td>
<td>3~4 mA</td>
<td>~3 mA</td>
<td>~2 mA</td>
<td>~1 mA</td>
</tr>
<tr>
<td>Reference ( R_{\text{ss}} )</td>
<td>470 Ω</td>
<td>860 Ω</td>
<td>1.2 kΩ</td>
<td>1.5 kΩ</td>
<td>2.2 kΩ</td>
<td>4 kΩ</td>
</tr>
</tbody>
</table>

Note: Reference \( R_{\text{ss}} \) values are given with \( V_{\text{DD}} = 8 \) V.

\( R_{\text{tr}} \) tuning

\( R_{\text{tr}} \) is tuned according to the desired switching slew rate in different applications. In hard-switching conditions, low \( R_{\text{tr}} \) is desired to achieve a high slew rate and thus reduce hard-switching loss. A typical \( R_{\text{tr}} \) value for \( R_{\text{DS(on,typ)}} = 140 \) mΩ device is within the range of 20 to 50 Ω with \( V_{\text{DD}} = 8 \) V. This value can be scaled to other ohmic class devices according to the desired slew rate. In soft-switching conditions, selection of \( R_{\text{tr}} \) is uncritical.

Maximum source and sink current can be quantified according to:

\[
I_{\text{on,max}} \sim \frac{V_{\text{DD}} - V_F}{R_{\text{tr}}}, \quad I_{\text{off,max}} \sim \frac{V_{\text{th}} + V_N}{R_{\text{tr}}}
\]  

(2)

\( C_{\text{c}} \) tuning

\( C_{\text{c}} \) is tuned according to the desired negative gate voltage bias \(-V_N\) during the transistor off-state. \( V_N \) must always be positive and can be quantified according to:

\[
V_N = \frac{C_{\text{c}}(V_{\text{DD}} - V_F) - Q_{\text{Geq}}}{C_{\text{c}} + C_{\text{GS}}}
\]  

(3)

with \( Q_{\text{Geq}} \) denoting an equivalent switching gate charge (\( Q_{\text{Geq}} = Q_{\text{GS}} \) for a hard-switching system and \( Q_{\text{Geq}} \sim Q_{\text{GS}} + Q_{\text{GD}} \) for a soft-switching system).

In hard-switching conditions, \( V_N \) is recommended around 4 to 5 V depending on circuit topology and slew rate, which should be designed according to a trade-off between false trigger immunity and third-quadrant
Tuning the RC interface

operation loss. In soft-switching conditions, $V_N$ can be lowered down to 2 V or even close to zero in specific soft-switching topologies.

### 3.2 Reference RC interface tuning for typical applications

#### 3.2.1 Hard-switching and soft-switching

In hard-switching applications, the turn-on slew rate should be well-controlled to achieve a trade-off between switching loss and drain-source voltage overshoot. Typical RC interface designs in hard-switching applications are given in Table 2.

<table>
<thead>
<tr>
<th>$R_{DS(on,typ)}$</th>
<th>$R_{DS(on,max)}$</th>
<th>$R_{tr}$</th>
<th>$R_{ss}$</th>
<th>$C_C$</th>
<th>Turn-on slew rate</th>
<th>$-V_N$</th>
</tr>
</thead>
<tbody>
<tr>
<td>55 mΩ</td>
<td>70 mΩ</td>
<td>5.6 Ω</td>
<td>470 Ω</td>
<td>3.3 nF</td>
<td>~ 105 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>10 Ω</td>
<td>470 Ω</td>
<td>3.3 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 90 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>15 Ω</td>
<td>470 Ω</td>
<td>3.3 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 75 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>10 Ω</td>
<td>470 Ω</td>
<td>3.3 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 90 V/ns</td>
<td>~ -4 V ~ -5 V</td>
</tr>
<tr>
<td>140 mΩ</td>
<td>190 mΩ</td>
<td>20 Ω</td>
<td>1.8 kΩ</td>
<td>1.5 nF</td>
<td>~ 100 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>27 Ω</td>
<td>1.8 kΩ</td>
<td>1.5 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 80 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>47 Ω</td>
<td>1.8 kΩ</td>
<td>1.5 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 60 V/ns</td>
<td>~ -3 V</td>
</tr>
<tr>
<td>20 Ω</td>
<td>1.8 kΩ</td>
<td>3.3 nF</td>
<td>1.3 nF</td>
<td></td>
<td>~ 100 V/ns</td>
<td>~ -4 V ~ -5 V</td>
</tr>
</tbody>
</table>

Note: Reference values are given with EiceDRIVER™ 1EDi/2EDi series gate driver and $V_{DD} = 8$ V. The slew rate in applications is subject to system design and PCB layout.

![Figure 5](image_url)

**Figure 5** Reference RC interface design for CoolGaN™ GIT HEMT in separate gate path applications

When designing a gate driver with a separate gate path, the RC interface can be configured with an independent transient gate-on resistor $R_{tr\_on}$ and gate-off resistor $R_{tr\_off}$, as shown in Figure 5(a). For a gate driver with unified output, a diode in the gate-off loop can be installed to independently control the turn-on and turn-off speed as shown in Figure 5(b). In hard-switching applications, a larger $R_{tr\_on}$ is selected to avoid transistor drain-source voltage overshoot and a smaller $R_{tr\_off}$ is selected to guarantee sufficient damping of oscillations in the gate loop.

In soft-switching applications, simultaneous high current and high voltage in the power switching is avoided, which yields much slower voltage transients with typical slopes of only a few V/ns. Negative gate voltage bias ($-V_N$) should be chosen to be as low as possible, recommended within -2 V. $R_{tr\_on}$ and $R_{tr\_off}$ are obviously less critical in soft-switching applications and can be chosen to be higher than in hard-switching applications.
3.2.2 CoolGaN™ IPS products

![CoolGaN™ IPS single-channel](image1)

Figure 6 RC interface configuration in CoolGaN™ IPS products

The RC interface circuit is also compatible with CoolGaN™ IPS products. The same tuning circuit and methodology can be configured in half-bridge and single-channel products, as shown in Figure 6.

3.2.3 Motor-drive applications

CoolGaN™ GIT HEMTs are advantageous in motor-drive applications for their low switching loss, small form factor and high temperature stability characteristics. Considering the physical limitations of motor winding, the slew rate of CoolGaN™ GIT HEMTs should be largely reduced. To achieve this goal, the RC interface shown in Figure 7 should be configured.

![CoolGaN™ half-bridge](image2)

Figure 7 Reference RC interface configuration for CoolGaN™ GIT HEMTs in motor-drive applications

Table 3 Reference RC interface design for CoolGaN™ GIT HEMTs in motor-drive applications

<table>
<thead>
<tr>
<th>$R_{DS(on,typ)}$</th>
<th>$R_{DS(on,max)}$</th>
<th>$R_{tr_{on}}$</th>
<th>$R_{tr_{off}}$</th>
<th>$C_C$</th>
<th>$R_{ss}$</th>
<th>$C_{gd_{ext}}$</th>
<th>$R_{damp}$</th>
<th>$C_{gs_{ext}}$</th>
<th>Slew rate</th>
</tr>
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<tbody>
<tr>
<td>270 mΩ</td>
<td>340 mΩ</td>
<td>200 Ω</td>
<td>20 Ω</td>
<td>3 nF</td>
<td>2 kΩ</td>
<td>5~9 pF</td>
<td>50 Ω</td>
<td>100 pF</td>
<td>~5 V/ns</td>
</tr>
<tr>
<td>270 mΩ</td>
<td>340 mΩ</td>
<td>200 Ω</td>
<td>20 Ω</td>
<td>3 nF</td>
<td>2 kΩ</td>
<td>w/o</td>
<td>w/o</td>
<td>2 nF</td>
<td>~10 V/ns</td>
</tr>
</tbody>
</table>

Note: Reference values are given with EiceDRIVER™ 1EDI/2EDI series gate driver and $V_{DD} = 8$ V. The slew rate in applications is subject to system design and PCB layout.

The RC interface values shown in Table 3 are given as reference design for motor-drive applications. A large gate-on resistor $R_{tr_{on}}$ is selected to slow down the switching speed. A low gate resistance path formed by $R_{tr_{off}}$.
and D_{off} provides safe turn-off conditions. Extra capacitance $C_{gs_{-}ext}$ and $C_{gd_{-}ext}$ is paralleled to the transistor input to slow down the switching speed to 5 V/ns and prevent false triggering. $R_{damp}$ is installed to the external $C_{gd_{-}ext}$ path to prevent unwanted gate ringing. For space-constrained applications, a high blocking voltage $C_{gd_{-}ext}$ capacitor is not wanted. In this case, a larger $C_{gs_{-}ext}$ can be selected to reduce slew rate down to 10 V/ns.
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References

4 References

[1] Application note: Driving CoolGaN™ GIT HEMT 600 V high electron mobility transistors


List of abbreviations

HEMT ....................................................................................... high electron mobility transistor
CoolGaN™ IPS......................................................................... CoolGaN™ Integrated Power Stage
MOSFET ..................................................................................... metal-oxide semiconductor field-effect transistor
SMPS .......................................................................................... switch-mode power supply
$R_{DS(on)}$ .................................................................................. transistor on-state resistance
$R_{DS(on,typ)}$ ............................................................................... transistor on-state resistance typical value
$R_{DS(on,max)}$ ................................................................................ transistor on-state resistance maximum value
$V_{F}$ ............................................................................................ gate diode forward voltage drop
$V_{th}$ ............................................................................................. gate threshold voltage
$I_{on}$ .............................................................................................. gate-on current
$I_{off}$ ............................................................................................ gate-off current
$R_{ss}$ ............................................................................................ steady-state gate current tuning resistor
$R_{tr}$ ............................................................................................. transient switching speed $dv/dt$ tuning resistor
$R_{tr,on}$ ......................................................................................... transient gate-on resistor
$R_{tr,off}$ ........................................................................................ transient gate-off resistor
$C_{C}$ ............................................................................................... gate coupling capacitor
$-V_{N}$ ............................................................................................. negative gate voltage at the start of transistor off-state
$-V_{NF}$ ........................................................................................ negative gate voltage at the end of transistor off-state
$V_{DD}$ ............................................................................................ gate-supply voltage
$V_{GS}$ ............................................................................................. gate-source voltage
$I_{ss}$ .............................................................................................. on-state gate current
$I_{on,max}$ ..................................................................................... transient maximum gate-on current
$I_{off,max}$ .................................................................................... transient maximum gate-off current
$Q_{ges}$ ......................................................................................... equivalent switching gate charge
$C_{GS}$ ............................................................................................ gate-source capacitance
$Q_{GS}$ ............................................................................................ gate-source charge
$Q_{GD}$ ............................................................................................ gate-drain charge
$C_{gd,ext}$ ....................................................................................... external gate-drain capacitor
$C_{gs,ext}$ ....................................................................................... external gate-source capacitor
$R_{damp}$ ........................................................................................ damping resistor in external gate-drain capacitor path
## Revision history

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<th>Document version</th>
<th>Date of release</th>
<th>Description of changes</th>
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<td>V 1.0</td>
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<td>First release</td>
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<tr>
<td>V 1.1</td>
<td>2021-12-02</td>
<td>Updated denomination of CoolGaN™ GIT HEMTs</td>
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