Driving GaN made easy by Infineon
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CoolGaN™ concept and standard gate drive

Gallium Nitride (GaN) switches on silicon substrates belong to the most promising candidates for next-generation power systems. The combined effort of researchers and manufacturers during the last years has led to mature and reliable devices with some very attractive features when compared with silicon superjunction MOSFETs: zero reverse recovery charge (no intrinsic body diode) and 90 percent lower gate and output charge. This enables operation in hard-switched half-bridge topologies as well as high switching frequency and short dead time.

In the high-voltage (600 V) arena, four different GaN switch concepts can be found on the market today. Two of them use the natural, intrinsic GaN/AlGaN heterojunction transistor with its negative gate threshold voltage, but operate the resulting “normally-on” device in a series connection with a low-voltage silicon MOSFET. In the classic cascode configuration the MOSFET is switched, whereas direct-driven concepts control the GaN gate; this requires a negative gate drive voltage.

The alternate approaches use a p-doped GaN gate to shift the threshold voltage to positive values. If this gate is contacted through a Schottky contact, the resulting device is compatible with standard driving, but the gate is highly sensitive to overvoltages, and it is difficult to keep the optimum drive voltage over current and temperature variations. So it is the final concept, combining a pGaN gate with an ohmic contact that Infineon chose for its CoolGaN™ 600 V e-mode HEMTs [1].

In the equivalent circuit of Figure 1a and the gate charge curve Figure 1b the main differences with respect to a Si MOSFET are highlighted.

- The ohmic pGaN gate can be modeled as a diode between gate and source with a threshold voltage $V_G$ of about 3.5 V. The best way to drive such a gate is by applying a continuous small current of a few mA in the “on”-state.
- The intrinsic transistor lacks a physical body diode and as a consequence, there is zero reverse recovery charge. In reverse operation S and D interchange their functionality and the transistor conducts, if $V_{GS}$ exceeds the threshold voltage. Any negative $V_{GS}$ adds to the “diode” voltage drop $V_D$.
- Due to the lateral structure, a certain part of the channel resistance (~ 20%) is located within the gate loop – if driven by a constant voltage, the effective gate voltage would decrease with current and cause an increase in $R_{DS(on)}$. With the proposed current drive, however, the gate voltage adapts itself to the optimum value.

Although the total gate charge is very low (~ 5 nC), a gate drive current up to 1 A is required during the switching transients (Figure 1d).

Figure 1 Equivalent circuit of CoolGaN™ and gate drive (a), gate charge curve (b), gate voltage (c) and current waveform (d)
This is why the most simple driving concept depicted in Figure 1a consists of a standard gate driver (switches S1, S2) and two parallel gate current paths to provide the high transient currents \( I_{on}/I_{off} \) via \( R_{gs}/R_{off} \) and coupling capacitance \( C_{cc} \), while \( R_{ss} \) is used to set the small on-state current Iss. In this context, all gate drivers out of Infineon’s EiceDRIVER™ family can be regarded as nearly ideal due to their low output impedance and fast signal propagation. Several possible configurations with isolated (2EDF7275K, 2EDF7275F, 1EDB7275F) and non-isolated (1EDN7550B) drivers are described in [2].

Another typical GaN feature is evident in Figure 1b as well. The low \( V_{th} \) together with a relatively high \( Q_{gs}/Q_{off} \) ratio in some cases (hard-switched half-bridge) requires the availability of a negative gate drive voltage \( V_N \) to keep the device safely “off” and avoid unintended turn-on effects. Fortunately, the coupling cap \( C_c \) not only provides the high current path but also generates a negative gate voltage \( V_N \) after any switching-off event. The reason is that during the preceding “on”-state (S1 closed), \( C_c \) has been charged to the difference of driver supply \( V_G \) and gate clamp voltage \( V_H \). Thus, when the “off” switch S2 is closed, \( C_c \) acts as a charge-pump driving the gate to a negative voltage \( V_N \). Figure 1c. The resistors define the gate current levels, and with proper dimensioning of the components, all gate drive parameters can be easily adapted to transistor size and application.

This drive concept is simple, versatile, and flexible – but what are the drawbacks? The most important one is probably the so-called “first-pulse” effect. For a hard-switching transient happening, soon after having switched “off” the passive switch in a half-bridge, the negative \( V_{gs} \) will prevent any erroneous turn-on. However, in situations with a much longer dead time, e.g. during start-up, in burst-mode operation, or in case of non-complementary switching, spurious turn-on may happen and increase the voltage/current stress on the switches – in extreme cases, even dangerous oscillations can result. This is why dedicated GaN driver ICs have been developed to address and eliminate the adverse “first-pulse” effects.

**Dedicated CoolGaN™ driver: The GaN EiceDRIVER™ family**

Figure 2a explains the implemented concept. The output stage consists of two half-bridges, connected to gate and source of the GaN switch, respectively. In normal operation, an external RC network defines the gate drive parameters, very similar to the standard drive. However, by closing switches S1 and S4, a negative gate voltage \( -V_{gs} \) can be applied even with completely discharged \( C_{cc} \).

**Figure 2b** depicts a full switching sequence including a “first-pulse” situation. In normal operation the initial “off”-level \( V_{gs} \) is defined by \( C_c \) and \( V_H \). However, instead of discharging \( C_c \) via \( R_{ss} \), the “off”-voltage is switched back to zero after a programmable fixed time \( t_1 \) (typically some 100 ns). This on the one hand means identical conditions for all switch -“on” events (independent of “off”-state duration), on the other hand minimizes reverse conduction losses during the dead times. A “first-pulse” situation is assumed if the “off”-state lasts longer than a time \( t_2 \) (typically 32µs). Then the “off”-level is switched to \( -V_{gs} \) thereby effectively avoiding any unintended turn-on when the opposite switch starts switching again.

**Figure 2** New differential gate drive concept for CoolGaN™ (a) and associated control signals (b)

The GaN EiceDRIVER™ ICs have been developed to optimally drive and protect Infineon’s CoolGaN™ 600 V e-mode HEMTs. As depicted in Figure 3, these drivers are available in three package versions, enabling an easy adaptation to different requirements in terms of power density, PCB space, and isolation rating [2].

**Figure 3** GaN EiceDRIVER™ product family

**Table 1** summarizes the main specifications of Infineon’s GaN EiceDRIVER™ ICs. The functional isolated 1EDF5673K is available in the LGA-13 5x5 mm² package, whereas the 1EDF5673F comes in a DSO-16 150-mil package. If the PWM control signals have to cross the safe isolation barrier, as in the secondary-side controlled resonant LLC converter, the 1EDS5663H with reinforced isolation is the appropriate choice. In the DSO-16 300-mil package, it is compliant with the safety requirements of the VDE 0884-10 and UL 1577 standards.

Despite the different packages and input-to-output isolation classes, ratings, and certifications, these gate drivers are based on the same rail-to-rail driver output stage. It is realized with complementary MOS transistors that are able to provide a typical 5.4 A sourcing and 9.8 A sinking current. Although these current levels are neither needed nor reached when driving GaN HEMTs (due to their low gate charge of only a few nC), the low on-resistance coming together with the high driving current is
nevertheless beneficial. With an R<sub>s</sub> of 0.85 Ω for the sourcing pMOS and 0.35 Ω for the sinking nMOS transistor, the driver can be considered as a nearly ideal switch, enabling cooler operation due to less power dissipation in the IC.

<table>
<thead>
<tr>
<th>Product</th>
<th>Package</th>
<th>Input-to-output isolation (VDE 0884-10)</th>
<th>UL 1577</th>
<th>Peak source/ sink output current</th>
<th>CMTI (min.)</th>
<th>Prop. delay (ns)</th>
<th>Prop. delay accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1EDF5673F</td>
<td>LGA-13</td>
<td>functional 1.5 kV&lt;sub&gt;pk&lt;/sub&gt;</td>
<td>8 kV</td>
<td>5 A / -5 A</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
<tr>
<td>1EDF5673F</td>
<td>DSO-16</td>
<td>functional 1.5 kV&lt;sub&gt;pk&lt;/sub&gt;</td>
<td>8 kV</td>
<td>5 A / -5 A</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
<tr>
<td>1EDS5663H</td>
<td>DSO-16</td>
<td>reinforced V&lt;sub&gt;CE&lt;/sub&gt; = 8 kV&lt;sub&gt;pk&lt;/sub&gt;</td>
<td>8 kV</td>
<td>5 A / -5 A</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
</tbody>
</table>

The timing performance of the driver is also of particular importance to fully exploit the potential of GaN HEMTs. The low input-to-output propagation delay (37 ns) combined with high accuracy (-6 ns / +7 ns) over both temperature and production variations, allows for usage of a short dead time between the two PWM signals of the half-bridge; this improves efficiency by increasing the effective power transfer period.

The GaN EiceDRIVER™ products feature a minimum 200 V/ns CMTI capability which by far exceeds the requirements for the majority of fast-switching GaN applications, ensuring high robustness and reliability.

The GaN EiceDRIVER™ product family is optimized for high-frequency switching CoolGaN™ transistors above 1 MHz can be ensured by the GaN EiceDRIVER™ gate driver ICs.

**Switching CoolGaN™ HEMTs at frequencies above 1 MHz**

Thanks to significantly reduced parasitic capacitances, Infineon’s CoolGaN™ technology is the ideal choice when switching at frequencies in the MHz range, as required for example in wireless charging applications. For testing CoolGaN™ switches together with the dedicated GaN EiceDRIVER™ ICs, the half-bridge evaluation board EVAL_1EDF_G1_HB_GAN has been designed [3]. The generic topology, a fundamental building block in nearly all converter and inverter applications, can be configured for boost or buck operation, pulse testing, or continuous full-power operation. The power circuit of this evaluation board is composed of two IGBT60R070D1 CoolGaN™ 600 V e-mode HEMTs with 70 mΩ R<sub>DS(on)</sub> and two 1EDF5673K GaN EiceDRIVER™ ICs. The output and bus voltage of this evaluation platform can range up to 450 V, limited by the capacitor rating. Furthermore, it is able to switch a continuous current of 12 A as well as a peak current up to 35 A, and can be configured for hard- or soft-switching. The switching frequency can go up to several MHz, depending on transistor power dissipation (limited to about 15 W per device with appropriate heatsink and airflow).

**Figure 4** shows the top-side view of the GaN EiceDRIVER™ half-bridge evaluation board and the gate-to-Kelvin-source voltages of the two CoolGaN™ transistors. As explained, the V<sub>GS</sub> voltage is clamped by the intrinsic gate-to-source diode to around 3.5 V. Additionally, the negative voltage after every turn-off is defined by the gate driver supply voltage and the coupling capacitance C<sub>GS</sub>. Typically 200 ns after turn-off, V<sub>GS</sub> is actively switched to zero in order to reduce the reverse conduction losses during the subsequent dead time. As can be seen from the measured waveforms in **Figure 5b**, reliable commutation of the CoolGaN™ transistors above 1 MHz can be ensured by the GaN EiceDRIVER™ gate driver ICs.

**Figure 5a** shows the measured waveforms of the GaN EiceDRIVER™ half-bridge evaluation platform featuring GaN EiceDRIVER™, Infineon Technologies AG, Application Note AN_1811_PL52_1811_234307, 2019

**References:**

