Benefits of GaN e-mode HEMTs in
WIRELESS POWER TRANSFER

GAN POWER DEVICES IN RESONANT CLASS D AND CLASS E RADIO FREQUENCY POWER AMPLIFIERS

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Abstract

Wireless charging for portable devices dispenses with the need for conventional adapters/chargers with their associated cables and connectors. Although the technology has existed for some time and some smartphones support wireless charging for a while, only recently have tablets and notebooks had this capability. It is expected to become widely adopted within the next few years for other applications as well. The following paper demonstrates the advantages of gallium nitride (GaN) enhancement mode (e-mode) HEMT devices over MOSFETs in two power amplifier topologies that have been proposed for wireless power transfer according to the baseline specification of the AirFuel Alliance.

Introduction to resonant wireless charging

Currently, the most commonly used wireless charging standard is the inductive (Qi). Wireless charging systems that rely on the Qi standard operate by inductive coupling at frequencies in the 100 to 300 kHz range. This system allows charging of a single device only that needs to be placed very close to the charger in a specific orientation. With the increased interest in wireless applications for transmitting power in the consumer and industrial market, alternative implementations such as class D and class E resonant inverter topologies gain the attention of power conversion designers to leverage the advantages of resonant coupling. These topologies are not new and are already used successfully in radio frequency (RF) applications where the terminology "amplifier" is widely used to describe them. The main appeal for these topologies employed in the transmitter section of the wireless charging system - as showed in Figure 1 - is the achievable high efficiencies at operating frequencies in the 1 to 10 MHz range. The AirFuel Alliance (formed in 2015) proposes a method switching at 6.78 MHz in the ISM (industrial, scientific and medical) frequency band that uses resonant inductive coupling in which high Q factor resonators enable power transfer over much greater distances using the much weaker magnetic fields in the peripheral regions. This enables the charging of several devices at the same time placed in any orientation. Faraday's law states that an electric potential is generated by a coil of wire when the magnetic flux in this coil varies. In wireless power transfer an RF power amplifier drives a power transmitting unit (PTU) consisting of a coil in a tuned circuit to produce a varying magnetic flux. A power receiving unit (PRU) also consisting of a coil in a circuit tuned to the same frequency, intersects the magnetic field so that a voltage is induced. This voltage depends on the rate of change of flux and number of turns. Output from the receiver coil is rectified and converted to the desired level for the portable device being charged. Coupling depends on the separation between the two coils, defined by the coupling factor k. A k of less than 0.5 represents a loosely coupled system as used in magnetic resonance coupling. Figure 1 shows the system blocks of the PTU and PRU. Microcontrollers with Bluetooth communication (according to AirFuel standard, in-band communication also possible) are used to request and regulate the amount of power transmitted as required by the devices being charged.
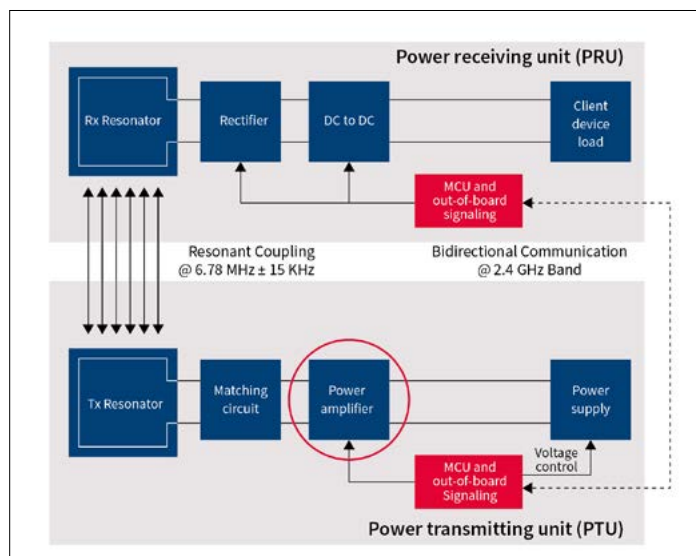

Figure 1 Wireless power transfer system blocks

Gallium nitride versus silicon technology

GaN technology is relatively new compared to silicon. Its merits have been already proved in RF systems and it is now gaining attention for many power applications due to the significant improvements in the figures of merit (FOM) that have been achieved
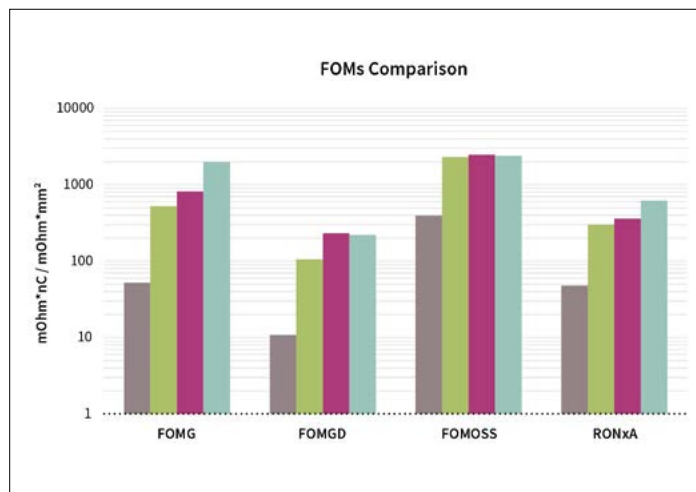

Figure 2 FOM comparison between gallium nitride (grey) and silicon technology (different vendors; green, pink, cyan)

Figure 2 shows the improvements of GaN technology in comparison to the state of the art silicon technologies coming from different vendors. The logarithmic scale helps to understand the quantum leap that GaN technology is offering, almost one order of magnitude for all FOMs.

2 Class D power amplifier

2.1 Topology overview

Figure 3 shows a simplified schematic for a class D amplifier which is very similar to an inverter that converts a DC input to an AC output.
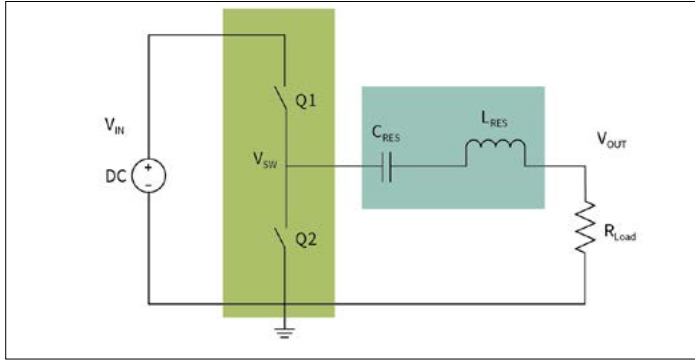
Figure 3 Class D power amplifier simplified schematic

In order to understand the class D functionality it is useful to divide the schematic into two main blocks:
1. **The switches:** these will create a rectangular periodic waveform with VIN amplitude.
2. **The filter:** LC filter will create a sinusoidal waveform, removing as much as possible the harmonics, at the same frequency of the incoming squared waveform. The further operation of the LC resonator is to block the DC voltage, therefore across the load there will be only an AC signal around the zero level.

Given this simple understanding the voltage across the load can be easily calculated considering a sinusoidal current given by the first harmonic of the filter. At the resonant frequency the LC impedance is zero.

The output voltage (peak to peak) at the load, considering the first harmonic, will be:

$$V_{OUT} = \frac{V_{IN}*2}{\pi}$$ **Equation 1**

The output power will therefore be:

$$P_{OUT} = \frac{V_{OUT}^2}{R_{LOAD}}$$ **Equation 2**

In the design phase of a wireless charging transmitter normally the output power of the transmitting coil is one of the inputs (which is here indicated with POUT), meanwhile the input voltage is one of the design parameters.
Equation 3 provides, once the output power is known, a method to determine the input voltage necessary to reach that power (assuming 100% efficiency).

$$V_{IN} = \left(\frac{\pi}{2}\sqrt{P_{OUT}R_{LOAD}}\right)$$ **Equation 3**

2.1.1 Class D ZVS transition

The class D topology works in ZVS turn on commutation since the operating frequency is 6.78 MHz, therefore the commutation losses could be very high leading to low efficiency. This also depends on the input voltage but normally, since the transmitting antenna is not capable of high current operation (typical currents for transmitting antennas are in the range of 1-2 A) in order to be able to transmit a significant power, relatively high input voltages (50-100 V) have to be used. So the combination of high voltage and high switching frequency requires ZVS operation. One of the most common methods to implement ZVS operation is to use an additional series LC network to create a triangular shaped current higher than the load current.
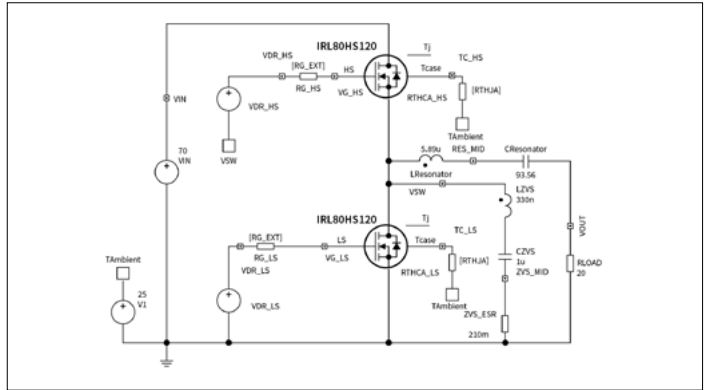

Figure 4 Class D simulation schematic with ZVS network

In order to guarantee the ZVS operation the current created in that way has to ensure the transition of the middle point of the half bridge (VSW in Figure 4) before the dead time is expired. This gives the following design rule for the class D topology:

$$T_{COM} = \frac{Q_{OSS}}{\Delta I}$$ **Equation 4**

Where the QOSS is the output charge of the switch evaluated at the input voltage and the ΔI is the ripple current generated by the ZVS network (LZVS + CZVS). Equation 4 shows that the lower the output charge of the switch the lower will be the ZVS ripple current, or in other words if the ripple current is fixed the lower is the QOSS the easier will be to guarantee the ZVS transition.

The power losses related to the ZVS network are the dominant losses (see simulation results). They can be calculated as:

$$P_{ZVS} = I_{ZVS\_RMS}^2 ESR_{ZVS}$$ **Equation 5**

Where the IZVS_RMS is the RMS current through the ZVS network and the ESRZVS is the parasitic equivalent resistance of the ZVS network, which is predominantly concentrated in the ZVS inductor.

ZVS operation depends on the load appearing resistive which requires a suitable impedance matching network to be included. The system will maintain ZVS operation within a defined set of corner impedance values known as an impedance box. It is preferable to use switches with low QGD to yield lower losses in case of non-ZVS operation.

2.2 Advantages of GaN in class D

At system level the largest loss contribution is the DC resistance of the ZVS inductor and other resistances inserted in the ZVS path accounting for more than 50%. Once the ZVS inductor is chosen, these losses are related to the ripple current and therefore to the QOSS device parameter. Reducing QOSS will greatly improve the losses. The remaining losses are equally distributed between the upper and lower switches

since this topology works with 50% duty cycle. At device level the highest contribution comes from the gate charge (QG), therefore a device with lower gate charge is essential but also a lower threshold voltage is desirable since this will lower the driving voltage allowing for further reduction of the driving losses. The simulations above were run with a pure resistive load, however considering that ZVS might is not guaranteed under all working conditions the switching losses are also considered. Low QGD is desirable in this case to avoid excessive losses.

2.2.1 Silicon versus GaN comparison
It is possible simulate a class D topology complete with ZVS network to check the performance (based on device models) and see the improvements expected using GaN technology to replace silicon.
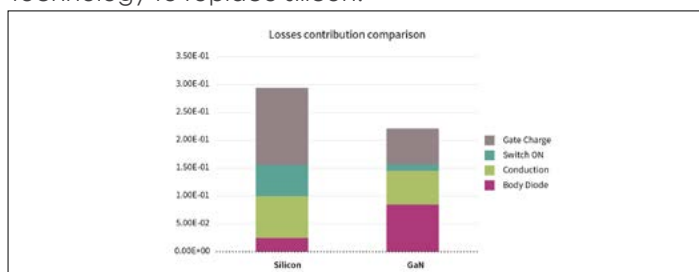

Figure 5 Loss comparison between GaN solution and silicon solution

As visible in Figure 5, the reduction of power losses between silicon and GaN is in the range of 30%. The simulations were run with equal dead times, however dead time optimization would further reduce the losses for GaN; for instance half of the dead time will reduce the losses by half as well. It is also noticeable that the device area is half for the GaN solution, creating an increase of power density of more than double.

Class E power amplifier

3.1 Topology overview
The single ended class E RF power amplifier topology consists of an RF inductor L1, which supplies an approximately DC current to the switching FET Q1, a resonant circuit and a load (see Figure 6). Q1 switches at 6.78 MHz with a fixed 50 percent duty cycle. When the circuit is tuned to the same frequency a half sinusoidal voltage appears at the drain which peaks at 3.56 times the DC input voltage (VIN), and
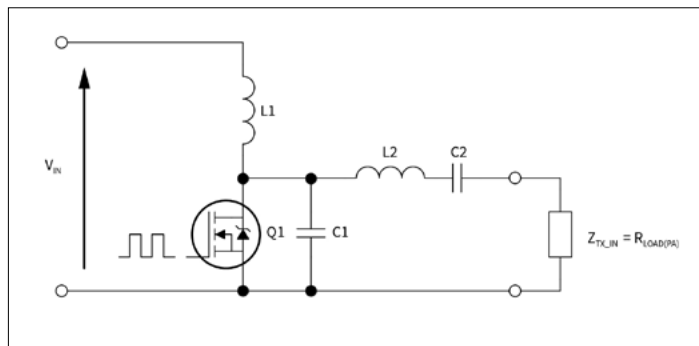

Figure 6 Single-ended class E amplifier main circuit elements

falls back to zero just before the start of the next switching cycle thus operating with zero voltage switching (ZVS). In order for this to be possible, the load impedance must be purely resistive. An impedance matching network is placed between the power amplifier and the transmit resonator, designed to cancel out all reactive elements.

The values of L2, C1 and C2 are determined according to the resonant frequencies of the two switching states. When the switch is off, C1 in parallel with the drain to source capacitance of Q1, contributes to the higher resonant frequency. When it is on the lower resonant frequency is determined by L2 and C2 only. For ZVS operation the switching frequency must lie between the higher and lower resonant frequency, and the sum of the periods of one half cycle of each resonant frequency must be approximately equal to the period of the switching frequency.

If the circuit resonance is higher than the switching frequency the drain voltage rings to a higher peak, which can be up to 7 times VIN, and it will fall to zero before the start of the next switching cycle so that body diode conduction occurs during the intervening period. If on the other hand the circuit resonance is lower than the switching frequency, the drain voltage will not be zero at the start of the next switching cycle. This creates hard switching with very high losses at 6.78MHz. To attain high power amplifier efficiency the circuit must be correctly tuned and in addition the output current should not be too high since this creates power loss in L2 resulting from conduction losses and eddy current losses due to the skin effect which is significant at 6.78MHz. The PRU and impedance matching network should then be designed to develop a high ZTX_IN for the power amplifier load.

3.2 Advantages of GaN in class E
A class E power amplifier rated up to 16W was tested using a 200 V, 125 mΩ OptiMOS™3 switch, the BSC12DN20NS3. To evaluate power amplifier performance and efficiency a resistive load was used and measurements taken at 25 Ω, 15 Ω and 5 Ω. The efficiency was measured at 91-92 percent in each case. The operating waveforms for 25 Ω are showed as follows:
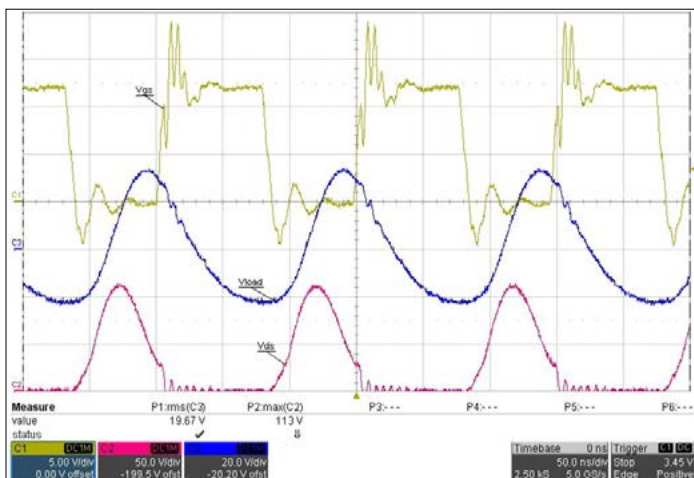

Figure 7 Single-ended class E amplifier operating waveforms with Silicon MOSFET

In Figure 7 the red trace shows the drain voltage waveform. It is observed that the shape is not a pure half sinewave, displaying a spreading characteristic at lower voltages which prevents it from falling all the way to zero before the next switching cycle resulting in some hard switching. This effect is caused by the effect of the MOSFET COSS on the upper resonant frequency of the circuit. In silicon MOSFETs COSS increases considerably at lower voltages which creates this distortion. Although the circuit is able to operate with acceptable efficiency and the switching losses caused by the small amount of hard switching are not high, this is still problematical. The circuit has to be retuned resulting in a higher peak voltage, which reduces the maximum power capability and output impedance range over which the power amplifier can operate without reaching the MOSFET avalanche rating BVDSS.

A GaN HEMT with the same BVDSS and RDS(on) ratings was also tested in the same circuit. Figure 8 shows the comparison of the COSS characteristics for the two power switches plotted on a logarithmic scale revealing that in the GaN device the increase is much less, though the quoted value at VDS of half BVDSS is very similar.

The drain waveform for the GaN based is seen to be much more sinusoidal than in the MOSFET example. The hard switching is not present and the peak voltage is equal to 3.56 times VIN indicating that the circuit is operating at the theoretical optimum. This allows operation over a wider range. Furthermore in practice the circuit is easier to tune and led prone to drift caused by tolerance and temperature.

It is clear that GaN enables the class E circuit to operate in the optimum manner where silicon does not, therefore offering improved efficiency and able to support a wider load impedance range.
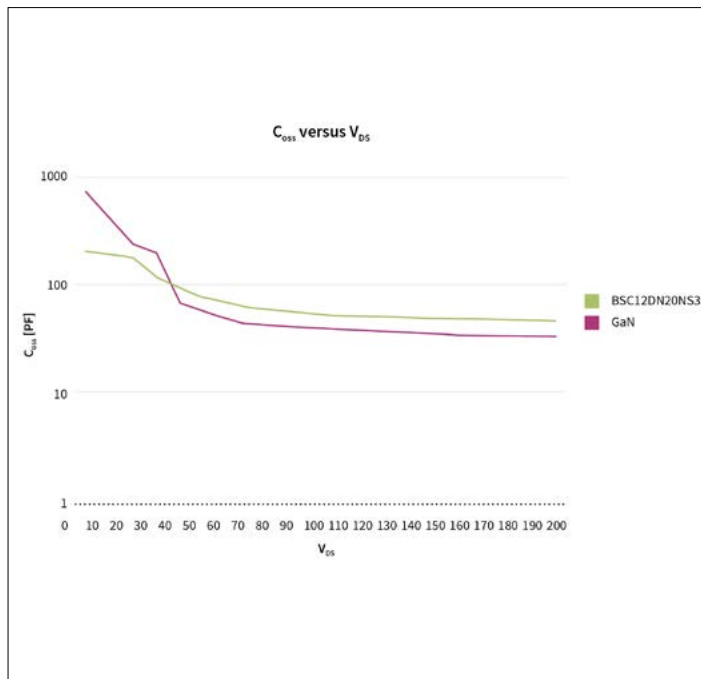

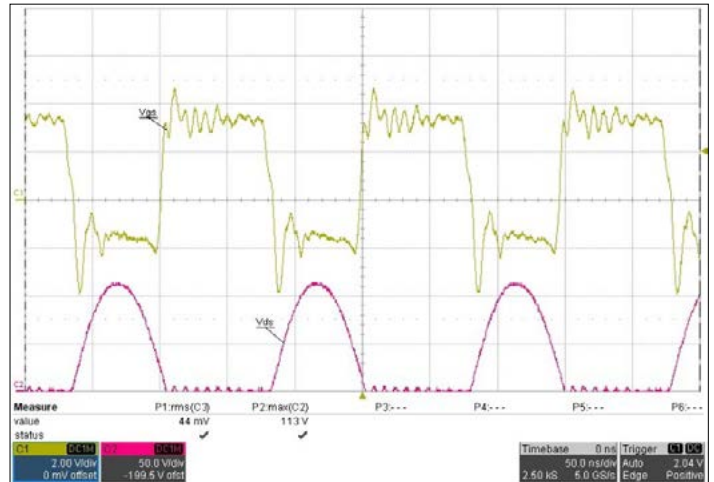*Figure 8 COSS versus VDS of a silicon and a GaN HEMT*

Figure 9 Single-ended class E amplifier operating waveforms with GaN HEMT

Conclusion

The advantages of GaN devices in wireless power transfer, which apply for both topologies discussed are summarized as follows:

4.1 Lower gate charge loss

GaN devices are typically driven with 5 V gate drive voltage as opposed to standard silicon MOSFETs that are typically driven around 10V. The gate charge (QG) for the GaN device is about one fifth of that for a MOSFET or similar RDS(on) and VBRR, which results in significantly lower gate drive current and far lower losses in the gate driver IC. In order to minimize gate charge loss it is preferable not only to choose low QG but also to use device technology with low gate threshold voltage allowing the designer to use lower driving voltage, therefore decreasing the overall losses related to the driving circuitry.

The gate charge losses can be calculated as:

$$P_{GATE} = \left(Q_{G\_SYNC} * f_{SW} * V_{dr} \right)$$

Equation 6

Where the QG_SYNC is the gate charge at voltage Vdr without the QGD (since it is assumed a ZVS transition), fSW is the switching frequency, and Vdr is the driving voltage.

4.2 Body diode losses

Though GaN HEMT devices do not have an actual body diode like a MOSFET, they do exhibit a diodelike behavior. Another important source of system losses is the body diode forward voltage which is, in fact, higher in GaN devices. Losses occur due to the ZVS commutation during turn on which can become relatively high if long dead times are chosen. To obtain best performance with GaN, dead time should be reduced to avoid body diode conduction.

$$P_{DT} = \left(V_{SD} * I_{OUT} * f_{SW} * T_{DT} \right)$$

Equation 7

In the evaluation of the body diode losses it is important to compute the correct VSD value which will vary with current and temperature.

4.2.1 Reverse recovery
Another source of the losses which is difficult to quantify is the reverse recovery charge (QRR) associated with the body diode conduction during the dead time. Since GaN devices do not include an actual body diode structure in their structure, they have zero QRR. The reason why it is difficult to quantify these losses is mainly related to the fact that the QRR is highly dependent on the following operating conditions: forward current of the diode, di/dt, reverse voltage and temperature. The values provided in device datasheets are references for designers, measured under specific test conditions, and these may have little relevance in the real application. Nevertheless, with the relatively high switching frequency used in magnetic resonance power transfer it is clear that a lower QRR will produce lower losses. The only question is related to the relative importance of these losses since the operating current and therefore the operating QRR are not high in this application.

4.3 GaN devices: good practice
In the previous paragraph it has been explained why GaN technology provides many opportunities to increase the overall efficiency of the system. However, this does not come for free. GaN technology has some attributes that need to be considered during system design.

4.3.1 Driving voltage accuracy
As specified in the datasheet, the absolute maximum rating for the VGS of a MOSFET is typically +/- 20V. This provides the designer some freedom to keep the voltage regulator of the driving stage relatively simple and cheap. For GaN this is not the case. The absolute maximum rating is limited to roughly 5 V- 6 V. This is mainly due to the diode nature of the gate structure. If during the operation the gate source voltage exceeds this limit in worst cases this could create severe damage to the device and at best reduction of the lifetime. For this reason the design of the voltage regulator used to create the driving voltage has to be done very carefully as the solution that works for silicon may not be suitable for GaN. The difficulties related to the capability of keeping the gate source voltage below the absolute maximum rating are not only related to the driving voltage regulator accuracy, but also to the operation during the dead time and the recharge of the bootstrap capacitor for driving the upper switch in the class D implementation. During the dead time operation the bootstrap capacitor is recharged through the body diode of the lower switch. In the case of the GaN devices the body diode with high forward voltage provides an extra charge to the boot capacitor which could exceed both with spikes and with steady state the absolute maximum rating of the device. This overcharge depends on many parameters (i.e., boot diode forward voltage, drain to source diode forward voltage, dead time, temperature) which have to be carefully evaluated.

4.3.2 Gate current
Differently from the silicon based products which drive the gate control through a gate oxide isolator, the gate connection for GaN devices takes the form of a Schottky barrier. The leakage current in the gate is consequently not in the range of nA but mA. This requires careful selection of the gate drive voltage and network components.

Device area
As seen in the previous paragraph, GaN technology provides greater power density resulting from the low RDS(ON) x area figure. This is related to the high conductivity of the electron gas (2DEG). This is a very attractive feature to designers who want to increase the power density of their applications but it also creates some challenges. The fact that the area is smaller implies that there will be less contact area to extract the power dissipated inside the device. During the layout phase the design of the power connections between the device(s) and PCB will be more challenging, and the thermal resistance of the device could suffer. Since the most important thermal resistance is junction to ambient which is mainly dictated by the PCB characteristics, the smaller dimensions of the GaN device package should not create too much additional thermal resistance. In any case particular care should be taken during the design of the PCB to minimize this thermal resistance since the smaller area of the GaN might partially counteract the advantage of the technology.
For Infineon's CoolGaN™ portfolio of switches and dedicated GaN EiceDRIVER™, please visit www.infineon.com/gan and www.infineon.com/gan-eicedriver.

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