Gate drive solutions for CoolGaN™ GIT HEMTs

Exploiting the full potential of GaN

Abstract

This paper explains the gate drive requirements for Infineon’s CoolGaN™ gate injection transistor (GIT) technology, which is based on a hybrid-drain high electron mobility transistor (HEMT) with a p-GaN gate. Various driving solutions are discussed, ranging from the standard RC-coupled driver to a new differential drive concept utilizing dedicated EiceDRIVER™ gate driver ICs optimized for CoolGaN™ GIT HEMTs. In half-bridge topologies, a hybrid configuration combining isolated and non-isolated driver ICs could be an exciting alternative. Practical application examples and circuit schematics complement the paper.

by

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1 Introduction

Although known for a long time as a promising material for power semiconductors, the need for exotic and expensive substrate materials limited the useful application areas for gallium nitride (GaN). In recent years, however, worldwide efforts have led to significant progress in the fabrication of reliable GaN transistors on cheap silicon substrates as a key for their economic success.

GaN belongs to the so-called wide-bandgap (WBG) semiconductor materials. It enables higher electric field strengths and thus results in significantly smaller high-voltage switches compared to silicon. As a direct consequence, the terminal capacitances of comparable GaN and silicon devices differ typically by almost an order of magnitude.

What is even more important, GaN switches belong to the so-called heterojunction high electron mobility transistors (HEMTs). Here, the conducting channel is formed at an AlGaN/GaN interface by a highly conductive 2-dimensional electron gas (2DEG). A GaN transistor thus is a lateral device and does not contain physical pn-junctions. And that is why GaN transistors can act not only as power switches but also as diodes, i.e., in a reverse direction with negative drain-to-source voltage. This is not possible with high-voltage silicon (Si) superjunction (SJ) MOSFETs due to the high reverse recovery charge \( Q_{rr} \) of their intrinsic p/n body diode and the extreme nonlinearity of their output capacitance [1]. Both effects would cause huge switching current, stress, and losses when operated in hard-switched half-bridges [2]. So the possible substitution of diodes by switches is one of the most important benefits of GaN, allowing the utilization of new power topologies such as e.g., Totem-pole PFC. Furthermore, the lateral structure of GaN transistors basically enables monolithic integration of switches together with other passive or active components (“GaN-ICs”). This trend can be observed for some time now, and it may lead to many attractive new applications (bidirectional switch, half-bridge integration, integrated gate drive, etc.).

However, as with most power switches, the key to getting all the benefits out of GaN is the proper gate control. The physical properties of the switch and the implemented gate concept have a strong impact on the optimum driving scheme. In this paper, the standard RC gate drive concept is explained based on a discussion of the equivalent gate circuit of Infineon’s CoolGaN™ GIT HEMTs with a gate injection transistor (GIT) structure. Although it works well in several applications, an innovative differential driving scheme has been developed and implemented in the dedicated EiceDRIVER™ gate driver ICs for CoolGaN™ GIT HEMTs. Finally, for driving half-bridges, a hybrid configuration combining isolated and non-isolated driver ICs is introduced, based on practical application examples and circuit schematics.
2 High-voltage GaN concepts

2.1 Concept comparison

In the 600 V arena currently we can find four different GaN switch concepts.

The first two use the natural, intrinsic GaN/AlGaN heterojunction transistor with its negative gate threshold voltage but operate the resulting “normally-on” device in a series connection with a low-voltage silicon MOSFET to achieve “normally-off” behavior.

› In the well-known classic cascode configuration only this MOSFET is controlled, and thus this approach is compatible with standard gate driving. Drawbacks are the relatively high switching losses due to the MOSFET reverse recovery charge, complex switching dynamics and high voltage stress on the MOSFET.

› The other concept utilizing “normally-on” GaN switches operates the series MOSFET as a safety switch if no negative voltage is available; it is constantly “on” in normal operation. In this directly-driven approach a dedicated gate driver has to switch the GaN gate between a relatively large negative voltage and zero.

The two alternate approaches use a p-doped GaN gate to modify the band structure and shift the threshold voltage to positive values (“normally-off”).

› If this p-gate is contacted by means of a Schottky contact, the resulting device is basically compatible with standard driving. However, as the gate is highly sensitive to over-voltages, the gate voltage has to be limited very accurately, and it isn’t easy to keep the optimum drive voltage over current and temperature variations.

› So it is the final “normally-off” concept that Infineon chose, known specifically as a hybrid-drain gate injection transistor (GIT), combining a p-GaN gate with an ohmic contact – this leads to a non-isolated gate structure with a diode-like input characteristic that is best driven by a small current, but on the other hand provides a very reliable and robust gate structure and high performance.

Table 1 summarizes key transistor parameters of typical representatives of the above concepts with similar on-resistance $R_{DS(on)}$; the main drawbacks are indicated in red.

The classic cascode is the only concept with an effective non-zero reverse recovery charge ($Q_r$). $Q_r$ is even larger than the output charge $Q_{oss}$ (which itself is the largest of all switches); the result is significantly higher losses in hard-switching topologies compared to the other concepts.

The directly driven GaN in the safety switch concept needs a relatively large negative gate drive voltage of about -15 V that is usually not available in the system and thus requires additional effort.

Another noticeable difference is the significant temperature dependence of $R_{DS(on)}$ for the p-GaN Schottky concept. As explained in the following, this is due to the non-optimum gate drive caused by the overvoltage sensitivity and can be very important in many applications, as it may dictate the use of switches with lower nominal $R_{DS(on)}$ compared to the other concepts.
Table 1  | Key parameters for different high-voltage (HV) GaN switch concepts

<table>
<thead>
<tr>
<th></th>
<th>Classic cascode</th>
<th>Safety switch</th>
<th>p-GaN Schottky</th>
<th>p-GaN ohmic (CoolGaN™)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(on)}$ [mΩ]</td>
<td>49</td>
<td>70</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td>Threshold voltage $V_{th}$ [V]</td>
<td>2.1</td>
<td>-7</td>
<td>1.7</td>
<td>1.2</td>
</tr>
<tr>
<td>Gate charge $Q_g$ [nC]</td>
<td>2.8</td>
<td>~30</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Output charge $Q_{oss}$ [nC]</td>
<td>107</td>
<td>58</td>
<td>57</td>
<td>41</td>
</tr>
<tr>
<td>Reverse recovery charge $Q_{rr}$ [nC]</td>
<td>136</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>150°C/RDS</td>
<td>&lt;sub&gt;(on)&lt;/sub&gt;25°C</td>
<td>2.1</td>
<td>1.9</td>
</tr>
</tbody>
</table>

2.2  Infineon’s CoolGaN™ GIT HEMT concept

Figure 1 depicts a cross-section of Infineon’s CoolGaN™ GIT HEMT.

![Cross-section of the CoolGaN™ GIT power switch](image)

Figure 1  | Cross-section of the CoolGaN™ GIT power switch

It is a p-GaN enhancement-mode hybrid-drain HEMT with an ohmic gate, also called Gate Injection Transistor (GIT). The p-GaN layer at the drain side helps reduce the notorious current collapse effects – which appear after an exposition to high blocking voltages – and hence achieve excellent dynamic $R_{DS(on)}$ behavior [3].

The gate module deserves a closer look. In contrast to MOSFETs, it is not isolated from the transistor bulk; the gate input characteristic, as given in Figure 2a, shows a diode-like behavior with a forward voltage drop of approximately 3.5 V. And it also indicates the best way to drive such a gate reliably, namely by means of a driving source with a relatively high impedance. The resulting stable gate current guarantees constant switch parameters, while a varying voltage drive would cause a large variation of the gate current and the associated parameters. Thus, providing a small constant current during the steady “on”-state is the best-suited concept. However, a higher gate drive current (up to 1 A) must be available during the switching transients, as indicated in Figure 2b.
Yet, there is another benefit of the constant current drive. In Figure 3 we see the $R_{DS(on)}$ dependence on gate current for a CoolGaN™ GIT HEMT (a) and a switch with p-GaN Schottky gate (b), the latter showing a much stronger increase of $R_{DS(on)}$ over drain current. One of the reasons for this behavior is that, due to the lateral device structure, a part of the channel resistance is located within the gate loop (Figure 4). The voltage drop across this resistance subtracts from the constant and limited driving voltage, causing the observed current dependence. So again this confirms: for the same nominal $R_{DS(on)}$, the current-driven gate allows a significantly higher maximum current.

![Figure 2](image1.png)

**Figure 2** CoolGaN™ GIT HEMT gate characteristics (a) and gate drive current (b)

![Figure 3](image2.png)

**Figure 3** $R_{DS(on)}$-dependence on drain current (from datasheets) for CoolGaN™ GIT HEMT (a) and Schottky gate (SG) GaN (b)
3 Driving the gate of CoolGaN™ GIT HEMTs

From the above it is clear: the Ohmic p-GaN gate provides a very attractive solution for high-voltage (HV) GaN switches, but only if controlled appropriately. The key gate driver requirements can be derived from the equivalent circuit of Figure 4.

The main differences with respect to a Si MOSFET are highlighted:

› The ohmic p-GaN gate can be modeled by inserting a diode between the gate and source terminal with a threshold voltage $V_F$ of about 3.5 V.

› All CoolGaN™ GIT HEMTs are operated with a separate Kelvin-source connection SK that eliminates the common source inductance, but on the other hand, requires some kind of input-to-output isolation for the gate driver, as the voltage peaks between pins S and SK can reach several tens of Volts for fast switching.

› The intrinsic transistor lacks a physical body diode, and as a consequence there is zero reverse recovery charge. In reverse operation S and D interchange their functionality and the transistor conducts in case $V_{GD}$ exceeds the threshold voltage. So for zero $V_{GS}$ the “diode” voltage drop is equal to $V_{Miller}$, but any negative $V_{GS}$ is added to this drop.

› Due to the lateral transistor structure, a certain part of the channel resistance is located within the gate loop – this leads to an effective gate voltage that depends on drain current and causes the described increase of $R_{DS(on)}$ with current if driven by a constant voltage. With the proposed current drive, the gate voltage adapts itself to the optimum value.

› There is a significant voltage dependence of $C_{DS}$ on $V_{DS}$. However, it is only one compared to three orders of magnitude for a typical superjunction (SJ) MOSFET.

Figure 4 also depicts the easiest and simplest way to generate a gate current waveform as indicated in Figure 2b. Instead of a single gate resistor, two parallel current paths are combined to provide both the
high transient currents $I_{on}/I_{off}$ via $R_{on}/R_{off}$ and the coupling capacitance $C_C$, while $R_{ss}$ is used to set the small on-state current $I_{ss}$. The gate driver itself can be modeled as two current-limited switches connecting this RC interface to either the positive or the negative node of the driving voltage $V_P$.

![Diagram](image)

**Figure 5 Gate charge curves $V_{GS} = f(Q_G)$ for CoolMOS™ SJ MOSFETs (a) and CoolGaN™ GIT HEMTs (b)**

To also give a feeling for the quantitative differences, Figure 5 compares typical gate charge curves for a CoolMOS™ SJ MOSFET and a CoolGaN™ GIT HEMT. Obviously, GaN is characterized by a significantly lower threshold voltage $V_{th}$ (1.2 V) and an almost 90 percent lower gate charge. The low $V_{th}$, together with a relatively high $Q_{GD}/Q_{GS}$ ratio, may require the availability of a negative gate drive voltage $V_N$ to keep the device safely “off” and to avoid simultaneous conduction of both switches in hard-switched half-bridge topologies (spurious turn-on, “shoot-through”).

And as an impact of the low gate charge, the useful peak gate drive currents are also rather low (below 1 A). That is why the gate driver current limits usually do not affect the possible switching speed.

Finally, due to the internal diode, the gate voltage is clamped to 3 - 4 V. The consequence is the need for a small constant steady-state current $I_{ss}$ on the one hand, but on the other hand, the resulting gate module is very robust and reliable. The additional power dissipation due to the gate current is in the few tens of mW range and thus usually negligible.
4 The standard gate drive concept for CoolGaN™ GIT HEMTs

To summarize the above, driving CoolGaN™ GIT HEMT requires:

- a moderate gate current (< 1 A) during the switching transients
- a low gate current (10 mA) in the steady "on"-state
- a negative gate-to-source voltage (few Volts) during hard-switching voltage transients
- galvanic input-to-output isolation (high-side) and/or
- capability to handle ground voltage differences caused by inductive voltage drops (low-side).

These requirements can most easily be fulfilled by combining one of the fast gate driver ICs of Infineon’s EiceDRIVER™ family (see also Chapter 6) with the already discussed RC interface, as shown in Figure 6a.

![Figure 6 Standard driving scheme for CoolGaN™ GIT HEMTs (a) and resulting VGS waveform (b)](image)

In this configuration the gate driver can be regarded as ideal, and the external components exclusively define switching dynamics. The coupling capacitance $C_C$ not only provides the high current path, but also generates a negative gate drive voltage $V_N$ after a switching-off event, as during the preceding "on"-state (S1 closed) $C_C$ is charged to the difference of driver supply $V_{DDO}$ and gate clamp voltage $V_F$. When the "off" switch S2 is closed, $C_C$ acts as a charge pump driving the gate to a negative voltage with an initial value $V_N$ that is defined by gate driver supply voltage and coupling capacitance (Figure 6b). The resistors determine the gate current levels, and with proper dimensioning of all components this solution is easily adaptable to transistor size and application (Table 2). A quick reference guide about the dimensioning of the RC interface is available in [15].

Table 2 Typical RC component values for the 70 mΩ CoolGaN™ switch

<table>
<thead>
<tr>
<th>$V_{DDO}$ [V]</th>
<th>$C_{C,soft-sw}$ [nF]</th>
<th>$C_{C,hard-sw}$ [nF]</th>
<th>$R_{ss}$ [kΩ]</th>
<th>$R_{on}$ [Ω]</th>
<th>$R_{off}$ [Ω]</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>1.8</td>
<td>3.3</td>
<td>0.56</td>
<td>4.7 … 20</td>
<td>4.7</td>
</tr>
<tr>
<td>10</td>
<td>1.2</td>
<td>1.8</td>
<td>0.82</td>
<td>6.8 … 27</td>
<td>4.7</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>10 … 33</td>
<td>4.7</td>
</tr>
</tbody>
</table>
It should be noted that different \( C_C \) values are proposed for hard- and soft-switching topologies. This is due to the fact that in hard-switched half-bridges a higher negative gate drive of typically -3 to -5 V is required to optimize the trade-off between spurious turn-on (STO) effects and increased reverse conduction losses [4]. The minimum \( R_{\text{on}} \) depends on the total power loop inductance due to the fundamental trade-off between switching speed and overvoltage. The \( R_{\text{on}} \) ranges in Table 2 are valid for fast switching and minimized switching losses; for special purposes (e.g., motor drive, EMI reduction) significantly higher values are also reasonable.

So the standard drive concept is simple, versatile, and flexible – but what are the drawbacks?

First, as the coupling cap discharges during the “off” state via \( R_{\text{SS}} \), the gate voltage when switching “on” again depends on the “off” duration. This leads to a slight dependence of switching dynamics on duty-cycle; however, the practical effect in most applications is very small.

More important could be the so-called “first pulse” effect. The main benefit of the gate voltage waveform shown in Figure 6b is the following: for a hard-switching transient that happens soon after switching “off” one switch in a half-bridge, the negative VGS prevents any erroneous turn-on of this switch during the transient. However, if there are situations with both switches in “off”-state for a much longer time (e.g., during start-up, in burst-mode operation, or for topologies with non-complementary switching), the negative gate voltage decays to almost zero. Then a fast switching transient could cause significant cross-conduction due to STO effects and increase the voltage/current stress on the switches; in extreme cases even dangerous oscillations might result.

So, although the standard RC gate drive concept is a very good choice for many (soft-switching) applications, a dedicated GaN driver has been developed to particularly address and mitigate these “first pulse” effects.
5 Dedicated EiceDRIVER™ gate driver ICs optimized for CoolGaN™ GIT HEMTs

5.1 The differential gate drive concept

Figure 7 explains the implemented new concept. The driver output stage consists of two half-bridges connected to gate and source of the GaN switch, respectively. In normal operation an external RC interface defines the gate drive parameters in a very similar way to the standard drive concept. However, in a “first pulse” situation, a negative gate-to-source voltage can be applied even with completely discharged $C_C$ by closing switches S1 and S4. Then $V_{GS}$ equals $-V_{DDO}$; this can be used to effectively impede spurious turn-on.

![Figure 7](image)

**Figure 7** Differential gate drive concept for the CoolGaN™ GIT HEMTs product family

Figure 8 depicts a full switching sequence, including a “first pulse” situation.

![Figure 8](image)

**Figure 8** Switching sequence of the dedicated GaN driver
In normal operation the initial “off” level $-V_N$ is again defined by $C_C$ and $V_{DDO}$. However, instead of discharging $C_C$ via $R_{ss}$ only, the “off”- voltage is switched back to zero after a programmable fixed time $t_1$ (typically some hundreds of ns). This on the one hand means identical conditions for all switch-“on” events (independent of “off”-state duration); on the other hand it minimizes the reverse conduction losses during the dead-times.

A “first pulse” situation is assumed if the “off”-state lasts longer than $t_2$ (typically 32 µs). Then the “off”-level is switched to $-V_{DDO}$, thereby effectively avoiding any STO when the opposite switch starts switching “on” again.

### 5.2 Eice DRIVER™ for CoolGaN™ GIT product family

To optimally drive and protect Infineon’s CoolGaN™ GIT HEMTs, a family of dedicated single-channel galvanically isolated gate driver ICs has been developed. These products implement the differential gate drive concept described in the previous section. As depicted in Figure 9, three package versions are available for an easy adaptation to different requirements in terms of power density, PCB space, and isolation rating [5].

![Figure 9 The product family of the EiceDRIVER™ gate driver ICs for CoolGaN™ GIT HEMTs](image)

Table 3 summarizes the main specifications of the EiceDRIVER™ product family dedicated to CoolGaN™ GIT HEMTs.

<table>
<thead>
<tr>
<th>Product</th>
<th>Package</th>
<th>Input-to-output isolation</th>
<th>Typ. peak source / sink output current</th>
<th>CMTI (min.)</th>
<th>Propagation delay (typ.)</th>
<th>Propagation delay accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1EDF5673K</td>
<td>LGA-13 5x5 mm²</td>
<td>functional</td>
<td>$V_{IO}=1.5$ kVDC</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
<tr>
<td>1EDF5673F</td>
<td>DSO-16 150 mil</td>
<td>functional</td>
<td>$V_{IO}=1.5$ kVDC</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
<tr>
<td>1EDS5663H</td>
<td>DSO-16 300 mil</td>
<td>reinforced</td>
<td>$V_{IOTM}=8$ kVpk (VDE 0884-10) $V_{ISO}=5.7$ kVrms (UL 1577)</td>
<td>200 V/ns</td>
<td>37 ns</td>
<td>-6 / +7 ns</td>
</tr>
</tbody>
</table>
The products are available in different packages and isolation variants to meet a broad scale of design requirements. The functional isolated EiceDRIVER™ 1EDF5673K is available in the LGA-13 5x5 mm² package, whereas 1EDF5673F comes in a DSO-16 150 mil package. If the PWM control signals have to cross the safe isolation barrier, such as in the secondary-side controlled resonant LLC converter, the 1EDS5663H with reinforced isolation is the appropriate choice. In the DSO-16 300 mil package, it is compliant with the safety requirements of the VDE 0884-10 and UL 1577 standards [6].

Despite the different packages and input-to-output isolation classes, ratings, and certifications, these gate driver ICs are based on the same rail-to-rail driver output stage. It is realized with complementary MOS transistors that can provide a typical 4 A sourcing and 8 A sinking current. Although these current levels are neither needed nor reached when driving GaN HEMTs (due to their low gate charge of only a few nC), the low on-resistance coming together with a high driving current is nevertheless beneficial. Why? Simply because an $R_{on}$ of 0.85 Ω for the sourcing pMOS and 0.35 Ω for the sinking nMOS transistor guarantees near-ideal driver behavior and finally enables cooler operation due to less power dissipation in the IC.

The common-mode transient immunity (CMTI) is crucial to ensure that no signal corruption occurs during the switching transients due to the fast-moving output reference potential in high-side applications. Since the switching voltage transients can easily exceed 100 V/ns, CMTI is one of the key parameters to be considered for the gate driver selection. All EiceDRIVER™ products mentioned in Table 3 feature a minimum CMTI capability of 200 V/ns, ensuring high system robustness and reliability.

The timing performance of the driver is also of particular importance to exploit the full potential of CoolGaN™ GIT HEMTs. The low input-to-output propagation delay (37 ns) combined with high accuracy (-6 / +7 ns) over both temperature and production variations allows the use of a short dead-time between the two PWM signals of the half-bridge; this improves efficiency by increasing the effective power transfer period.

5.3 **A typical application: totem-pole PFC and resonant LLC**

The dedicated EiceDRIVER™ products (Table 3) fully leverage their functionality for high-voltage conversion applications. Figure 10 shows a typical switched-mode power supply (SMPS) with a totem-pole PFC and a secondary-side controlled resonant LLC converter, followed by a full-bridge synchronous rectifier.
As the PFC controller is located on the primary side and thus functional driver isolation is sufficient, the 1EDF5673F or 1EDF5673K gate driver ICs are best suited in the PFC’s hard-switching GaN half-bridge. For driving the CoolMOS™ switches in the phase rectification half-bridge (switching at 50 Hz or 60 Hz only), the dual-channel standard EiceDRIVER™ 2EDF8275F is recommended [7]. However, the DC-DC conversion stage, composed of resonant LLC and full-bridge synchronous rectifier, requires a reinforced isolated driver since the PWM signals have to cross the safe isolation barrier. The recommended 1EDS5663H driver features 8 mm input-to-output creepage/clearance distances and is compliant with the safety requirements of the VDE 0884-10 and UL 1577 standards. For driving the OptiMOS™-based full-bridge synchronous rectifier, the EiceDRIVER™ 2EDF7275K is the best fit.

### 5.4 Switching CoolGaN™ GIT HEMTs at frequencies above 1 MHz

Thanks to its significantly reduced parasitic capacitances, the CoolGaN™ technology is the ideal choice when switching at frequencies in the MHz range, as required for example in wireless charging applications [8]. For testing CoolGaN™ GIT HEMTs together with the dedicated EiceDRIVER™ for CoolGaN™ GITs, the half-bridge evaluation board EVAL_1EDF_G1B_HB_GAN is available [9]. The generic topology, a fundamental building block in nearly all converter and inverter applications, can be configured for boost or buck operation, pulse testing, or continuous full-power operation. The power circuit is composed of two IGOT60R070D1 CoolGaN™ GIT HEMTs 600 V with 70 mΩ $R_{DS(on)}$ and two 1EDF5673K EiceDRIVER™ ICs for CoolGaN™ GIT. The output and bus voltage range of this evaluation platform is 450 V, limited by the capacitor rating. It is able to switch a continuous current of 12 A as well as a peak current up to 35 A and is configurable for hard- or soft-switching. The switching frequency is
limited by the transistor power dissipation only (about 15 W per device with appropriate heatsink and airflow) and can go up to several MHz.

Figure 11a shows the top-side view of the high-frequency half-bridge evaluation board featuring the EiceDRIVER™ for CoolGaN™ GIT products, and Figure 11b the gate-to-Kelvin-source voltages of the two CoolGaN™ transistors. As explained, the $V_{GS}$ voltage is clamped by the intrinsic gate-to-source diode to around 3.5 V. The negative voltage after every turn-off is defined by the gate driver supply voltage $V_{DDO}$ and the coupling capacitance $C_C$. Typically 200 ns after turn-off, $V_{GS}$ is actively switched to zero to reduce the reverse conduction losses during the subsequent dead-time. The measured clean waveforms in Figure 11b demonstrate reliable switching of the CoolGaN™ GIT HEMTs driven by the EiceDRIVER™ for CoolGaN™ GIT products, even at frequencies above 1 MHz.
6 Standard gate driver ICs for CoolGaN™ GIT HEMTs

6.1 EiceDRIVER™ 2EDF, 2EDS, 1EDB and 1EDN-TDI

As explained in Chapter 4, the simplest driving concept consisting of a standard gate driver and an RC interface can be an alternative to the dedicated EiceDRIVER™ for CoolGaN™ GIT products (see Table 3). Several possible configurations with isolated (2EDF7275K, 2EDF7275F, 2EDF8275F, 2EDS7165H, 2EDS8265H, 1EDB7275F, 1EDB8275F) and non-isolated (1EDN7550B, 1EDN8550B) gate driver ICs out of Infineon’s EiceDRIVER™ family are described in [5]. As shown in Figure 12 and Table 4, they are available in different packages to allow an easy adaptation to different design requirements in terms of power density, PCB space and isolation rating.

Table 4 summarizes the key features of standard gate driver ICs with under-voltage lockout (UVLO) protection suitable for CoolGaN™ GIT HEMTs. For unipolar voltage supply below 10 V, products with UVLO\textsubscript{on} = 4.2 V and UVLO\textsubscript{off} = 3.9 V are the right choices. For unipolar voltage supply above 10 V or bipolar voltage supply (e.g., +8 V / -4 V), products with UVLO\textsubscript{on} = 8.0 V and UVLO\textsubscript{off} = 7.0 V should be preferred to ensure proper detection of supply voltage drop. The dual-channel functional isolated EiceDRIVER™ 2EDF7275K/2EDF8275K is available in an LGA-13 5x5 mm\textsuperscript{2} package, whereas the 2EDF7275F/2EDF8275F come in a DSO-16 150 mil, and the 2EDS7165H/2EDS8265H in a DSO-16 300mil package [7]. These products are well-suited for high-frequency half-bridge applications like totem-pole PFC or resonant LLC [10]. In terms of input-to-output isolation and propagation delay, these two gate driver ICs are equivalent to the respective EiceDRIVER™ for CoolGaN™ GIT products discussed in Chapter 5.
### 6.2 Hybrid gate driving for GaN half-bridges

A hybrid gate drive configuration for a CoolGaN™ GIT HEMT half-bridge (HB) can be implemented based on an isolated gate driver IC for the high-side and a non-isolated gate driver for the low-side switch, as depicted in Figure 13. The single-channel isolated EiceDRIVER™ 1EDB7275F and 1EDB8275F are offered in a DSO-8 150 mil package and feature 3 kV\textsubscript{rms} single protection isolation rating according to the UL 1577 standard [11]. Furthermore, it ensures a minimum of 300 V/ns CMTI robustness, which by far exceeds the requirements for the majority of fast-switching GaN applications. With a high propagation delay accuracy (-4/+6 ns) over both temperature and production variations, the 1EDB7275F and 1EDB8275F ensure accurate timing and reliable operation over a wide temperature range.

<table>
<thead>
<tr>
<th>Product</th>
<th>Package</th>
<th>Input-to-output isolation</th>
<th>Typ. peak source / sink output current</th>
<th>CMTI (min.)</th>
<th>Propagation delay (typ.) and accuracy</th>
<th>UVLO ON / OFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>2EDS7165H</td>
<td>DSO-16</td>
<td>reinforced</td>
<td>1 A / -2 A</td>
<td>150 V/ns</td>
<td>37 ns (typ.) -6 / +7 ns</td>
<td>4.2 V / 3.9 V</td>
</tr>
<tr>
<td>2EDS8265H</td>
<td>300mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.0 V / 7.0 V</td>
</tr>
<tr>
<td>2EDF7275K</td>
<td>LGA-13</td>
<td>functional</td>
<td>4 A / -8 A</td>
<td>150 V/ns</td>
<td>37 ns (typ.) -6 / +7 ns</td>
<td>4.2 V / 3.9 V</td>
</tr>
<tr>
<td>2EDF8275K</td>
<td>5x5 mm²</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.0 V / 7.0 V</td>
</tr>
<tr>
<td>2EDF7275F</td>
<td>DSO-16</td>
<td>functional</td>
<td>4 A / -8 A</td>
<td>150 V/ns</td>
<td>37 ns (typ.) -6 / +7 ns</td>
<td>4.2 V / 3.9 V</td>
</tr>
<tr>
<td>2EDF8275F</td>
<td>150 mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.0 V / 7.0 V</td>
</tr>
<tr>
<td>1EBD7275F</td>
<td>DSO-8</td>
<td>single protection</td>
<td>3 A / 6 A</td>
<td>300 V/ns</td>
<td>45 ns (typ.) -4 / +6 ns</td>
<td>4.2 V / 3.9 V</td>
</tr>
<tr>
<td>1EBD8275F</td>
<td>150 mil</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8.0 V / 7.0 V</td>
</tr>
<tr>
<td>1EDN7550B</td>
<td>SOT-23</td>
<td>non-isolated</td>
<td>CMR ≤ ± 200 V\textsubscript{DC}</td>
<td>n/a</td>
<td>45 ns (typ.) -7 / +10 ns</td>
<td>4.2 V / 3.9 V</td>
</tr>
<tr>
<td>1EDN8550B</td>
<td>6-pin</td>
<td></td>
<td>CMR ≤ ± 400 V\textsubscript{AC}</td>
<td></td>
<td></td>
<td>8.0 V / 7.0 V</td>
</tr>
</tbody>
</table>
The single-channel non-isolated EiceDRIVER™ 1EDN7550B and 1EDN8550B are available in a SOT-23 6-pin package. Thanks to the truly differential inputs (TDI), it is particularly well suited to drive 4-pin transistors with Kelvin-source connection [12]. The unique differential driving concept is able to safely prevent false triggering due to resistive or inductive voltage drops between the controller and driver IC reference potentials even for very fast switching transients [13]. The propagation delay matching between the high-side (HS) and low-side (LS) gate driver IC is also important to avoid cross-conduction in the half-bridge. Since both the 1EDN7550B/1EDN8550B and the 1EDB7275F/1EDB8275F have a typical 45 ns propagation delay and are based on the same output driving stage, it is possible to combine them in a hybrid configuration for half-bridge applications such as totem-pole PFC or resonant LLC. The increased layout flexibility, obtained by employing single-channel gate driver ICs, allows optimizing the driver IC placement on the PCB to minimize the parasitic gate loop inductance.

Furthermore, this hybrid gate drive configuration results in a 28 percent PCB area saving (compared to a dual-channel gate driver IC). It also comes with a competitive bill-of-material (BOM). Both gate driver ICs have non-inverting and inverting inputs (IN+ and IN-) that can be connected as shown in Figure 13 to implement shoot-through protection (STP). This feature provides an additional safety layer in case the controller generates incorrect PWM signals and therefore significantly improves the robustness of the power conversion system.

6.3 A typical application: totem-pole PFC and resonant LLC

Considering again the typical SMPS applications discussed in Chapter 5.3, alternative gate drive solutions based on the standard EiceDRIVER™ ICs listed in Table 4 are possible, too. For the totem-pole PFC stage, the hybrid gate drive configuration with 1EDB7275F and 1EDN7550B is able to drive both high- and low-side CoolGaN™ GIT HEMTs since the controller is located on the primary side. In the secondary-side controlled resonant LLC, the reinforced isolation of the EiceDRIVER™ 2EDS8165H is
used to transfer the PWM signals across the safe isolation barrier and simultaneously provide the required functional channel-to-channel isolation. The 1EDN7550B non-isolated gate driver ICs can be placed close to the respective CoolGaN™ GIT HEMTs to optimize the gate loop layout and minimize parasitic inductances. A bootstrap circuit enables a cost-effective implementation for the high-side driver supply.

![Figure 14 EiceDRIVER™ 2EDS, 1EDB, and 1EDN-TDI (truly differential input) in a typical SMPS application](image)

### 6.4 A CoolGaN™ GIT HEMT HB board with hybrid gate driving

The hybrid gate driving configuration is also applicable in a primary-side controlled resonant LLC converter, used for example in TV power supplies. Figure 15 shows an application schematic with a controller, gate driver ICs, and GaN power switches. The ICE2HS01G is an LLC plus synchronous rectification (SR) controller that can be operated up to 1 MHz switching frequency with the secondary switching current in both CCM and DCM conditions. As this controller provides ground-related output signals only, an isolated gate driver is needed to fulfill the functional isolation requirements for the high-side switch. The proposed hybrid half-bridge configuration then combines an EiceDRIVER™ 1EDB7275F with a 1EDN7550B.

Considering a 15 V supply for the controller, the input resistors of the 1EDN-TDI driver should be 160 kΩ [13]. For a soft-switching application with a 9 V gate drive voltage, the recommended RC interface is given in Figure 15 [4]. The floating supply voltage for driving the high-side CoolGaN™ GIT HEMT is again provided by a bootstrap circuit \( (C_B, D_B, \text{ and } R_S) \).
A CoolGaN™ GIT HEMT high-voltage half-bridge board implementing the power circuit highlighted in Figure 15 has been developed (without a controller). Figure 16 depicts the final board assembly (50 x 60 mm²) with the GaN switches, gate driver ICs and bootstrap circuit. The half-bridge consists of two IGLD60R190D1 CoolGaN™ GIT HEMTs 600 V with 190 mΩ R\textsubscript{DS(on)}. As explained, the EiceDRIVER™ 1EDB7275F and 1EDN7550B are used to drive the high- (HS) and low-side (LS) power switches, respectively. Since this test board was designed for 5 V PWM signals, the 51 kΩ input resistors of the 1EDN-TDI driver ensure a ±150 V AC and ±60 V DC ground-shift robustness [13].

The results obtained with this GaN half-bridge board are published in [14]. As demonstrated there, the 1EDN7550B gate driver with differential inputs can be a robust, space-efficient and cost-effective alternative to a dedicated EiceDRIVER™ for CoolGaN™ GIT HEMTs (see Table 3). Due to the compact footprint, it can be placed close to the CoolGaN™ GIT to prevent false triggering due to DC ground-shift or AC noise between the controller and the driver IC ground potentials. Depending on the system partitioning and control architecture, the non-isolated 1EDN-TDI gate driver can also be used in high-side driving as a replacement of isolated gate driver ICs to increase the power density in fast switching applications.
Figure 16  The CoolGaN™ GIT HEMT half-bridge board (50 x 60 mm) with hybrid gate driving
7 Conclusion

Wide-bandgap semiconductors allow higher electric field strengths and thus result in significantly smaller high-voltage switches compared to silicon alternatives. As a consequence, GaN-based power devices can operate at high switching frequencies without compromising efficiency. Infineon’s CoolGaN™ gate injection transistor (GIT) technology is based on a hybrid-drain HEMT with p-GaN gate resulting in a robust normally-off power switch. To deal with the particularities of this concept, an innovative differential gate-drive concept has been implemented in dedicated gate driver ICs of the EiceDRIVER™ product family optimized for CoolGaN™ GIT HEMTs.

Nevertheless, in many applications, standard gate driver ICs can also be employed when coupled to an RC interface to generate both the required small steady-state current and the turn-on/turn-off peak currents. A hybrid gate driving configuration for half-bridge topologies, composed of two single-channel gate driver ICs, allows optimizing the driver IC placement on the PCB in order to minimize the gate loop parasitic inductances. This results in a 28 percent PCB area saving (compared with a dual-channel gate driver IC) and it comes with a highly competitive bill-of-material (BOM).

To summarize, the 1-channel and 2-channel gate driver ICs of the EiceDRIVER™ family are the best choices to match with Infineon’s CoolGaN™ GIT HEMTs and achieve an optimum combination of efficiency, power density, and robustness in high-performance power conversion applications.

To learn more about Infineon’s CoolGaN™ portfolio of power switches and dedicated GaN-optimized EiceDRIVER™ driver ICs, please visit www.infineon.com/gan and www.infineon.com/gan-eicedriver, respectively.
References


[13] Infineon Technologies AG, “Applications of 1EDNx550 single-channel low-side EiceDRIVER™ with truly differential inputs,” Application Note AN_1803_PL52_1804_112257, 2018


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