POWER ELECTRONICS TECHNOLOGY

GAN-ON-SILICON-BASED POWER SWITCH IN SINTERED, DUAL-SIDE COOLED PACKAGE

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Sponsored by the U.S. Department of Energy, under the Advanced Research Projects Agency for Energy (ARPA-E), Delphi Automotive, International Rectifier (IR) and Oak Ridge National Laboratory have collaborated to produce 600V-rated GaN on Silicon HEMTs (based on IR s GaNpowIR platform) with sintered packaging interconnects (using Delphi s power semiconductor device package featuring dual-side cooling) capable of meeting the demanding power processing, environmental, power density and efficiency requirements for auxiliary and traction power in advanced hybrid and electric vehicles. We will detail construction, performance, initial reliability and modeled benefits in automotive traction application compared to existing IGBT solutions.

GaNpowIR Performance

The GaN-based HEMT technology used in the current effort leveraged the use of IR s GaNpowIR development. This included use of depletion-mode GaN on Silicon (Si) HEMTs configured in cascode connection to a low-voltage, silicon power FET. The 600V GaN devices were fabricated on 6-inch GaN on Silicon wafers and processed in a standard high volume silicon fabrication facility. Likewise, the low-voltage, silicon FET used was optimized for cascoded operation with the GaN HEMTs and also manufactured by IR.

Fig. 1 shows the typical measured room-temperature output characteristics of a 600V GaN on Si based HEMT with an active area of 8 mm^2 and gate width of 278 mm, cascoded with a low-voltage silicon FET in a high performance dual-side cooled package with sintered interconnects (**Fig. 3a** and **Fig. 3b**). As shown, the normally-off cascoded device demonstrates well behaved current handling capability with saturation occurring at about 80 A, providing ~1000 A/cm^2 of current density, significantly higher than that typically provided by the incumbent IGBT technology. **Fig. 2** shows the normally-off transfer characteristics of a typical cascoded device at both room temperature and 150 C. As shown, threshold voltage (extrapolated zero drain current intercept with the x-axis) is approximately 5.4 V at room temperature and approximately 4.4 V at elevated temperature. This demonstrates a substantial advantage of the cascode switch design over other normally-off GaN devices: gate drive requirements are set by the low-voltage FET and not by the GaN HEMT. Therefore, existing gate drivers can be used, so no costly customization or redesign is required.

Further work is ongoing to fabricate much larger devices (gate width = 1320 mm, active area = 37.5 mm^2). These GaN HEMTs yielded at initial electrical test and will be demonstrated in a multi-kilowatt inverter by Delphi.

Dual-Sided Cooling, Sintered Metal Interconnect

A schematic representation of the cascode configured package is shown in **Fig. 3**. **Fig. 3(a)** shows the electrical connection and defines the gate, source and drain of the packaged device. **Fig. 3(b)** shows the mechanical layout in the package to achieve the cascode configuration. **Fig. 3(c)** shows the packaged device. From a user s point of view, the packaged device is a normally-off device.

Both the top cap and the bottom substrate of the package are DBC substrates for enabling dual-side cooling. For power devices, dual-side cooling offers a lower thermal resistance when comparing to a typical wire-bond packaged device, and thereby provides more efficient heat dissipation from the packaged devices. From ANSYS simulations, the thermal resistance of the package was projected to be 0.47 C/W when both sides were liquid-cooled and 0.57 C/W when only the bottom substrate is liquid-cooled.

For dual-side cooling, both sides of the die were sintered to the substrate. To check the bond strength of the sintered die, metallized silicon pieces were tested. A silicon wafer was metalized on both sides of the wafer with front and back side metals identical to the metals used on the GaN on Silicon HEMT and silicon FET devices. This metallized wafer was then diced into 5 x 5 mm squares for the test.

Silver paste was screen printed on the back side of the DBC substrates, using five circular dots, 1 mm in diameter. Both gold and silver-plated DBC substrates were used. The locations of the five dots included four dots centered at the corners of a 3 x 3 mm

square and the fifth dot located at the center of the square. The 5 x 5 mm metalized silicon piece was positioned and centered on top of the five dots. The attached sets were sintered and then underwent a temperature cycle (TC) test to check the TC effect on the bond strength. The TC test ramped the temperature between -40 C and 135 C with 30 minutes ramping up, 35 minutes ramping down and soaking 5 minutes at the end temperatures.

To make sure the effect of sintering pressure on the thermal cycles could be observed, two different pressures (High and Low) were used in the sintering process. After sintering the pieces at 260 C for 5 minutes, several pieces of each condition were shear tested, to provide a pre-cycling baseline. The rest of the samples were put into a chamber for the temperature cycling test. Shear stress measurements were performed after each 250 temperature cycles, until 1250 cycles had been completed.

Fig. 4 shows the shear strength of the bonded silicon chips to the substrates during the temperature cycling test. Each error bar represents plus or minus one standard deviation of the measured values. The data show that after 1000 temperature cycles, there is no significant shear strength degradation in the samples sintered with High Pressure. Even at the end of tests (1250 cycles); measured shear strength is still higher than 50 MPa. The samples that used Low Pressure in the sintering process had their shear stress degrade 30% to 50% by the end of thermal cycle test.

Once initial sintering conditions were determined, cascoded GaN on Si HEMT (active area = 8 mm^2, gate width = 278 mm) and Si FET devices were packaged with dual-side, sintered silver interconnects. Initial long-term intermittent operating life (IOL) testing (power cycling) is ongoing, to compare the reliability of the sintered interconnect technology used in the high performance packages to that of the soldered interconnect packaging typically used in the industry. In prior work, IOL testing on soldered technology has shown that failure in power modules occurs due to bond-wire liftoff typically starting at about 10,000 cycles; secondarily, the die to package solder joint fails at about 40,000 cycles (at delta-T of approximately 100 C) [1]. **Fig. 5** shows the change in $RDS_{(ON)}$ measured initially and again after 18,000 cycles for several cascoded sintered devices. Devices were stressed at a delta-T of 100 C with a cycle time of approximately six minutes. As can be seen, there is relatively little change in performance and no failures have been observed out through 18,000 cycles.

These preliminary results are in line with previously published data (for sintered interconnect packaging) and demonstrate the high current GaN devices fabricated in this work have longer useful life than traditional IGBT modules which employ wire-bonded source and gate interconnect.

Modeling Projects 49% Reduction in Power Loss

A vehicle level traction drive simulator was developed at ORNL to assess the benefits of the initial GaN on Si technology relative to an existing Silicon semiconductor based hybrid vehicle. The simulator contains motor, inverter and battery models.

The motor and inverter models are generic allowing for use of design specific data. The motor model is based upon a commercial, on the road, internal permanent magnet motor, characterized by parameters extracted from benchmarking work performed at ORNL. The model allows for regenerative recovery of the vehicle s excess kinetic energy that is conventionally wasted in the brakes by friction. The motor model takes all or part of the road-power demand as input and computes the frequency, current, voltage and phase angle that will produce the optimal torque required at each time step. In pure electric power mode, the full road-demand is placed on the electric motor. In a hybrid configuration, the fraction of power allocated to the motor can vary from 0% to 100% of the required road-power, depending on the hybridization power-sharing scheme.

In this study, it is assumed that most of power demand of the drive cycle will be supplied by the electric drive train and, in the regions where the demand is more than the maximum power of the electric motor, the engine will generate the power. The available maximum terminal voltage limits the output power of the motor, which is dependent on the dc bus voltage with maximum boost. The terminal voltage is calculated assuming six-step mode of operation of the inverter.

The inverter requires the following data for a particular drive system to be simulated:

1. Number of parallel inverter legs
2. Number of diodes and switches per leg
3. Characteristic data for the diodes and switches such as: heat transfer coefficients, thermal inertias, conduction and switching loss functions with temperature, power factor and modulation index dependencies.

The inverter loss model was implemented with conduction loss models developed using averaging techniques and switching loss equations derived based on general switching energy loss data. The temperature dependent conduction loss parameters, on-state resistance, voltage drops, and switching losses were obtained from actual testing of the devices at Delphi. In addition to the power, current, power factor, and voltage demands computed by the motor model, the conduction loss model requires the modulation index as input. This index was calculated as the ratio of the terminal voltage required by the motor and the dc-link voltage provided by the boost converter. The temperature dependent power losses in the switches and diodes iterates with a thermal model that computes the junction temperatures from the power losses assuming a constant heat sink temperature.

For this study, the speed and power required for the drive were generated using 2008 Toyota Camry-like reference vehicle characteristics. The driving profile followed by the vehicle was the standard US06 drive cycle; a 20 minute, 8 mile long combination of urban and highway driving with 80 miles per hour (mph) peak and 52 mph average moving speeds. Assuming a flat terrain and no wind, the average and peak road-power demands placed on the vehicles motor were 25.1 kW/ 100 kW for propulsion and 19.7 kW / 68.6 kW for braking.

Fig. 6 shows the results of the system simulation, depicting the power dissipation over time for the US06 drive cycle. The simulation was performed with an inverter coolant temperature of 105 C, a dc bus voltage of 325 V, and a switching frequency of 20 kHz. The lower power losses of the GaN system are clearly evident, particularly during peak power demands.

Under the stated operating conditions, the GaN on Si system realizes an increase in average efficiency over the drive cycle of over 2.8%, from 94.21% to 97.03%, which equates to a reduction in losses by 49%.

References:

[1] Reliability Assessment of Sintered Nano-Silver Die Attachment for Power Semiconductors , Matthias Knoerr, Silke Kraft, Andreas Schletz, Fraunhofer Institute for Integrated Systems and Device Technology, published in the proceeding of the 2010 12th Electronics Packaging Technology Conference.

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