Frequently asked questions for TLE92108/4

About this document

Scope and purpose

This document compiles frequently asked questions for the TLE92108/4 and provides solutions to common problems that might occur during development using these devices. This document must be used in conjunction with the device datasheets, which contain full technical details, specifications, and descriptions for operation.

Intended audience

Developers working with the TLE92108 / TLE92104.

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Introduction

The TLE92108/4 are multiple MOSFET drivers, dedicated to controlling up to sixteen/eight n-channel MOSFETs. They integrate eight half-bridge drivers (TLE92108), or four half-bridge drivers (TLE92104) for DC motor control applications, such as automotive power seats, power lift gates, cargo cover, sunroof, door lock, and window lifts.

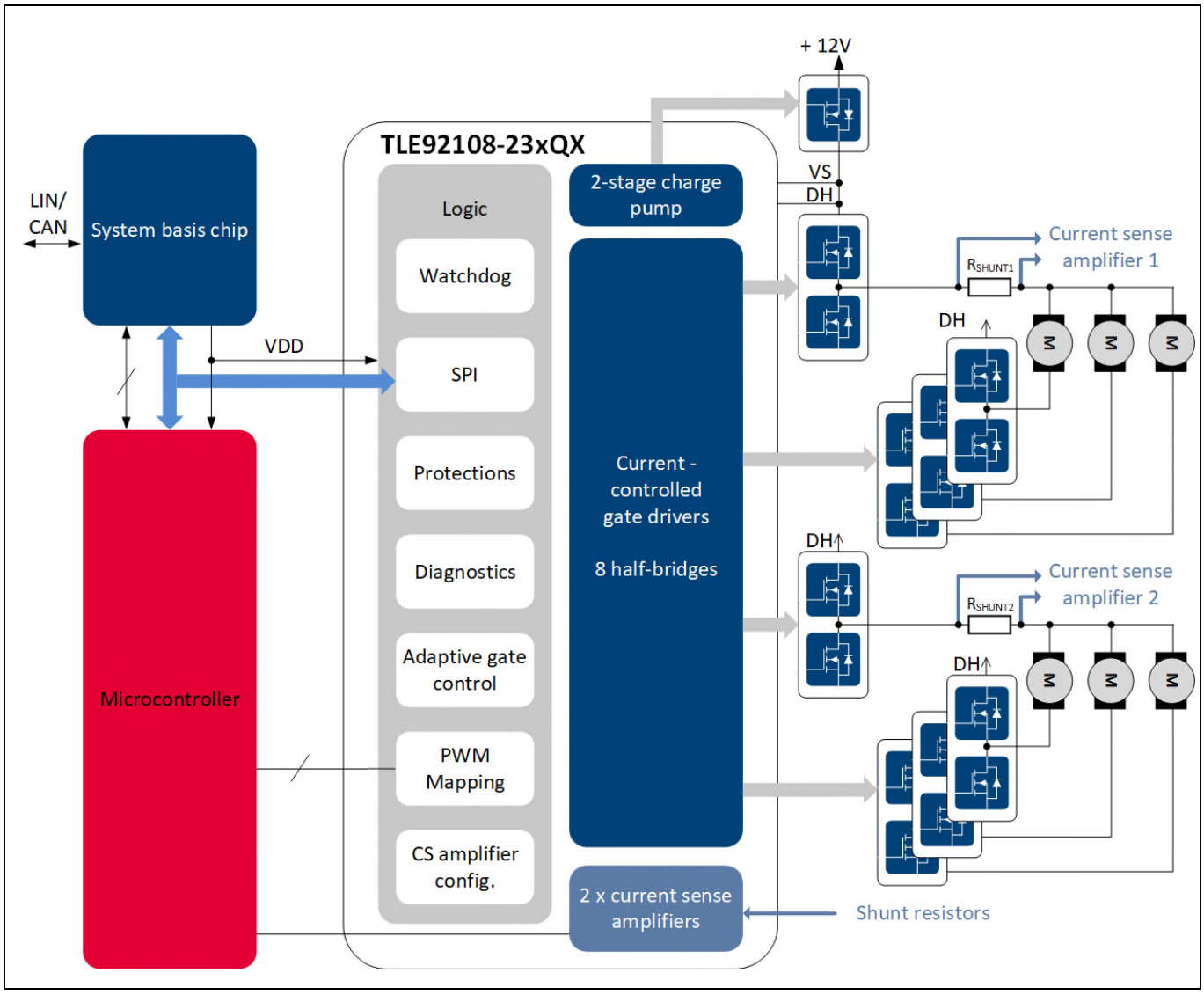

Figure 1 Block diagram of the TLE92108-231/232QX in one of the possible half-bridge configurations

1 Frequently asked questions

1.1 Does the TLE92108/4 support 32-bit SPI frames?

The register definition of the TLE92108/4 is optimized for 24-bit frames. However, it is possible to use 32-bit SPI frames as well.

For 32-bit SPI frames, the four bytes must be sent in the following order (refer to **Figure 2**):

Byte 1: Dummy byte 0x00

Byte 2: Address byte

Byte 3 and byte 4: Data word

The microcontroller receives the following information from the TLE92108-23x SDO in the following order (refer to **Figure 2**):

Byte 1: Global status byte

Byte 2: Dummy byte 0x00

Byte 3 and byte 4: Response word

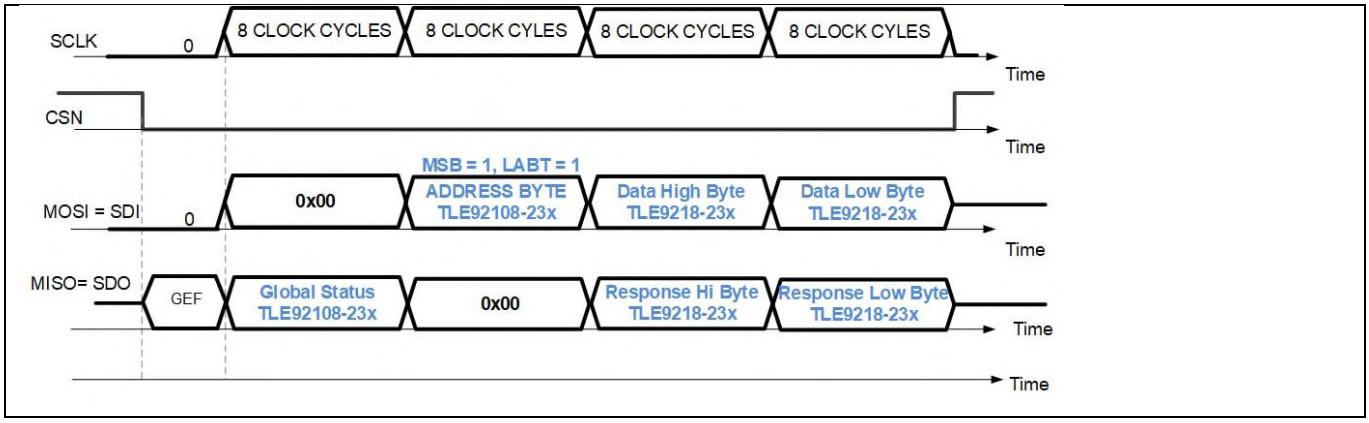

Figure 2 32-bit SPI frame with the TLE92108/4

It is recommended to use the dummy byte 0x00 to prevent the first byte from being wrongly interpreted as an address byte.

1.2 What are the benefits of the active free-wheeling control scheme?

Active free-wheeling (FW) reduces power losses in the FW MOSFET during the pulse width modulation (PWM) operation, therefore reducing costs at system level by:

Allowing the use of smaller MOSFETs and smaller MOSFET packages

Reducing the required PCB cooling surface of the FW MOSFET

1.2.1 Active free-wheeling

During the OFF-phase of the PWM period, the FW MOSFET is turned on. Therefore, the current flows through FW MOSFET instead of the body diode. Note that the current of the FW MOSFET flows from the source to the drain, due to the load inductance.

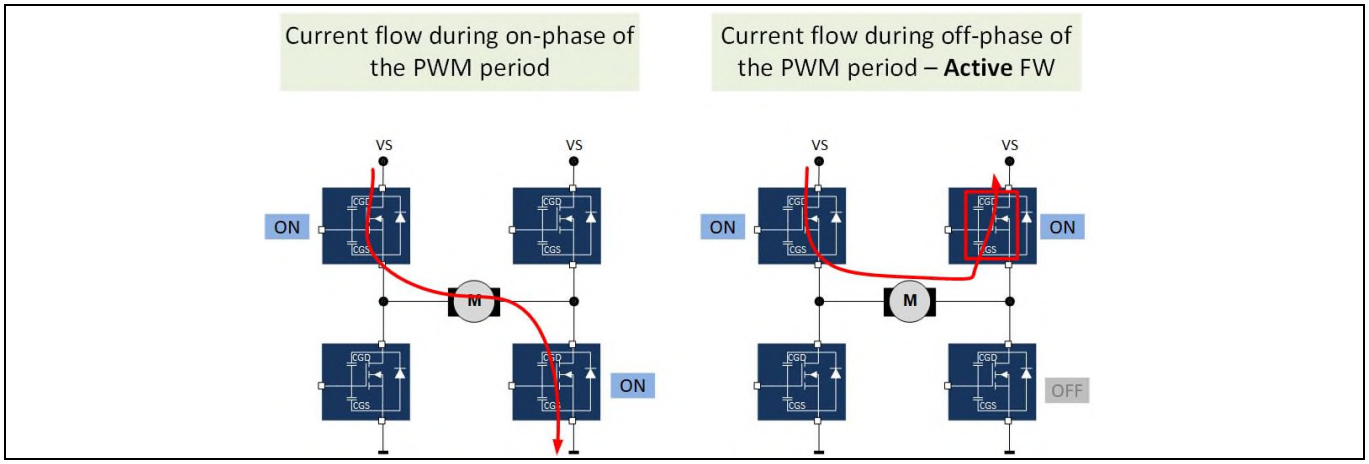

Figure 3 Current flow during off-phase of the PWM period – Active FW (with low-side PWM)

The peak power dissipation in the FW MOSFET during the PWM off-phase is given by (1):

(1) $P_{DISS\_FW\_MOSFET\_INST} = R_{DSON} \times I_{LOAD}^2$

The peak power dissipation in the FW MOSFET is present only during the PWM OFF-phase, therefore, the average power dissipation in the FW MOSFET over a PWM period is:

(2) $P_{DISS\_FW\_MOSFET\_AVR} = R_{DSON} \times I_{LOAD}^2 \times (1 - Duty)$

where Duty is the duty cycle (Ton / (Ton + Toff))

Note: The current ripple during the FW phase is neglected, in other words, it is assumed that the load current is constant over a PWM period.

Note: For the sake of clarity, the passive FW to avoid cross-currents is neglected, due to the short duration of this phase.

1.2.2 Passive free-wheeling

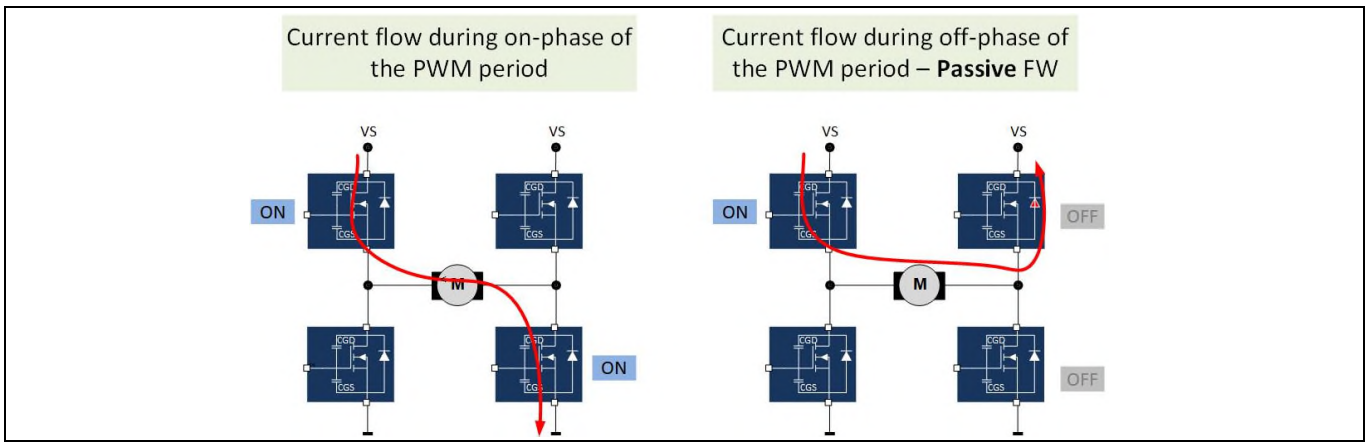

Figure 4 Current flow during the off-phase of the PWM period – Passive FW (with low-side PWM)

The peak power dissipation in the FW diode during the PWM OFF phase and the average power dissipation over a PWM period are given respectively by (3) and (4).

(3) $P_{DISS\_FW\_PEAK} = V_F \times I_{LOAD}$

(4) $P_{DISS\_FW\_AVR} = V_F \times I_{LOAD} \times (1 - Duty)$

where V_F is the forward voltage of the MOSFET body diode

1.2.3 Example

Example: I_{LOAD} = 15 A, duty cycle = 70%, V_F = 1 V, R_{DSON} = 7 mΩ

Power dissipation	Active FW	Passive FW
Peak power dissipation[1] [W]	1.58 ☑	15 ☒
Average power dissipation [W]	0.47 ☑	4.5 ☒

[1] during the PWM off-phase

In this example, the active FW decreases the average power dissipation in the FW MOSFET by 4 W.

Assuming a junction-to-ambient thermal resistance ($R_{TH-JAMB}$) of 25 K/W, the active FW control scheme reduces the average FW MOSFET temperature by 100 K, compared to a passive FW scheme!

This is why the active FW integrated in the TLE92108/4 reduces the system cost, compared to a solution with passive FW.

1.3 What is the purpose of the watchdog?

The watchdog (WD) monitors the SPI communication between the TLE92108/4 and the microcontroller, avoiding uncontrolled motor activations.

Note that the WD can be activated or deactivated by SPI (refer to chapter **1.5** How to disable the watchdog?). By default, the watchdog is enabled.

Case 1: The following sequence occurs:

The motor is turned on by the microcontroller

A local failure on the SPI bus occurs, for example, one of the SPI line is shorted

If the watchdog is deactivated prior to the failure, the SPI failure prevents any communication between the microcontroller and the TLE92108/4, so that the microcontroller cannot disable the gate drivers with an SPI command.

If the microcontroller detects the SPI failure, it is possible to stop the motor by either pulling the EN pin to low, or setting the device to sleep mode.

If the WD is activated prior to the failure, the WD cannot be served due to the faulty SPI bus. After the configured WD timeout (50 ms or 200 ms), a watchdog failure is detected by the TLE92108/4. Then the device goes into fail safe mode and all MOSFETs are turned off.

Case 2: The following sequence occurs:

The motor is turned on by the microcontroller

A failure leads to a microcontroller malfunction

If the watchdog is deactivated prior to the failure: the motor stays ON, unless for example, a safety logic detects a malfunction of the microcontroller and pulls the EN pin to low.

If the watchdog is activated prior to the failure: the WD isn't served due to the microcontroller's malfunction. After the configured WD timeout (50ms or 200 ms), a watchdog failure is detected, the TLE92108/4 goes in fail safe mode and all MOSFETs are turned off. All motors are OFF.

1.4 Does the WDTRIG bit need to be inverted, even when the WD settings in GENCTRL1 register do not need to be changed?

The WDTRIG bit must be inverted every time the GENCTRL1 register is written. Otherwise fail-safe mode is entered. This applies even if the bit settings being written do not affect the WD. That is., if changing the current sense amplifier (CSA) gain setting CSAG1, the WDTRIG bit must still be inverted when the write occurs.

1.5 How to disable the watchdog?

The watchdog is one possible protection against unintentional motor activation or, in the case of system failure such as SPI bus issues or microcontroller malfunction, therefore it is recommended to keep it enabled. However, for convenience, the WD can be disabled during the development phase.

The following sequence disables the watchdog:

1. SPI Frame 1: Set the UNLOCK bit (GENCTRL1)

Note: While setting the UNLOCK bit, the WDTRIG bit must be inverted to avoid a wrong watchdog failure. The default value WDTRIG right after a power-on reset is 0.

2. SPI Frame 2: Set WDDIS (in GENCTRL2)

If an SPI frame is sent between SPI Frame 1 and SPI Frame 2, then the UNLOCK bit is cleared. Consequently, the WD stays enabled despite the SPI Frame 2.

This sequence requiring **two consecutive SPI frames** and involving two different registers, prevents an unintentional deactivation of the watchdog with one single SPI command (for example due to a flipped bit).

1.6 What is the difference between the drain-source overvoltage and the overcurrent detection?

Two complementary protection strategies are implemented in the TLE92108/4 to detect short circuits while a MOSFET is on:

Drain-source (DS) overvoltage (OV) monitoring

Overcurrent detection with the shunt resistor and the current sense amplifier (CSA)

Note: To ensure that the MOSFET does not become active if there is a short circuit, the TLE92108/4 also provides a diagnostic feature when the device is in OFF-state (refer to the dedicated application note and to the datasheet chapter 7.6). With this feature, short circuits can be detected prior to the MOSFET activation.

Table 1 Comparison between the V_{DS} overvoltage and the overcurrent detection

	VDS overvoltage	**Overcurrent detection**
Type of detected short circuits	Hard short circuits (very low impedance)	Soft short circuits / overloads
Precision of the short circuit current detection (that is, current threshold)	Low	High
Reaction time	nominal 0.5 µs to 3 µs	nominal 6 µs to 100 µs

Drain-source overvoltage

The drain-source overvoltage detection is intended to detect hard short circuits, that is, with a low impedance. As described in the datasheet, this protection feature monitors the drain-source voltage of the activated MOSFETs and turns off the impacted MOSFETs when the drain-source voltage (V_{DS}) exceeds the configured threshold for a duration longer than the configured filter time (t_{FVDS} is set by control bit TFVDS).

The drain-source overvoltage detection is fast but not precise:

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$V_{DS} = R_{dson}$ x I_{DS} where R_{dson} is the MOSFET drain-to-source resistance in on-state, I_{DS} is the MOSFET drain-to-source current.

However, the MOSFET R_{dson} has a spread inherent to the production process and varies with the junction temperature of the MOSFET. Depending on the MOSFET technology, the R_{dson} of a given MOSFET can double from - 40 °C to 150 °C

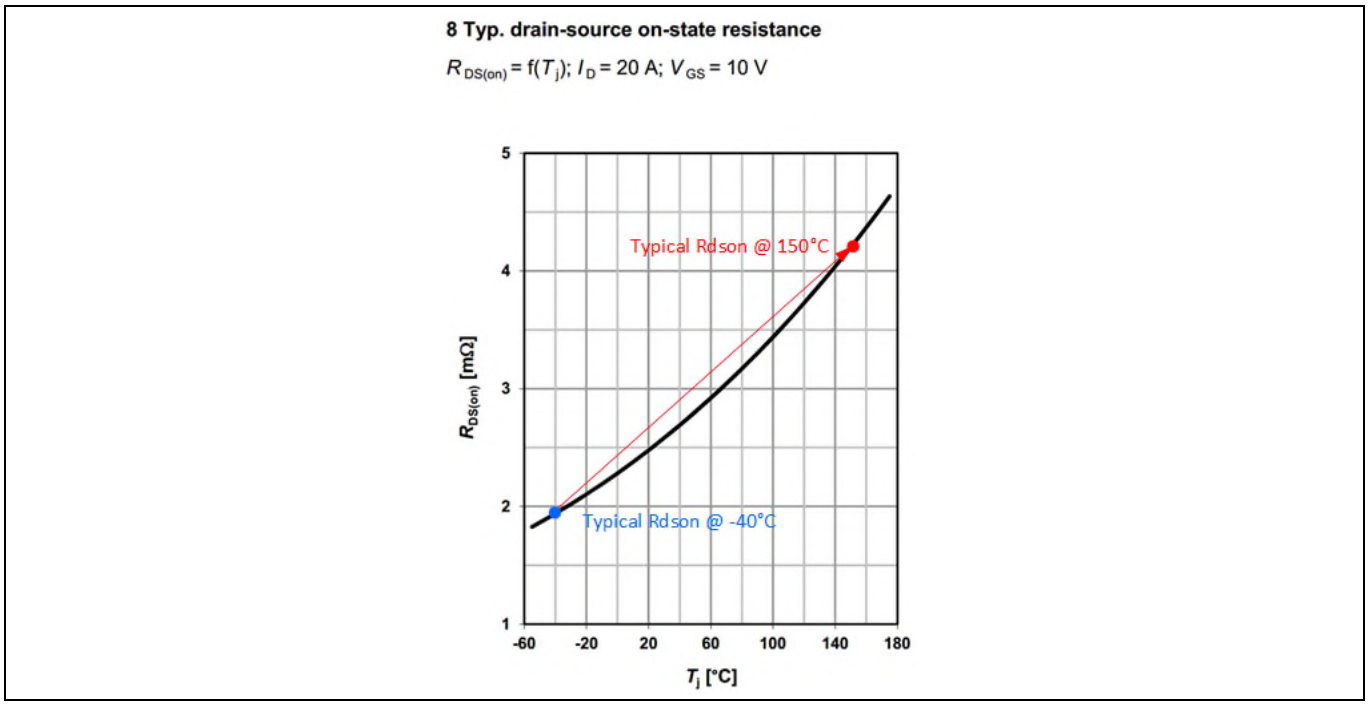

Figure 5 Example of $R_{DS(on)}$ variation with the temperature. Source datasheet: IPZ40N04S3R1

The drain-source overvoltage detection of the TLE92108/4 is optimized for speed (at the expense of the precision). The thresholds are specified with a tolerance of +/- 25 %.

The resulting load current triggers a drain-source overvoltage can be high for example. at low $R_{DS(on)}$, low MOSFET junction temperature, max. VDS overvoltage threshold.

Therefore, the reaction time must be very short to prevent MOSFET damages: t_{FVDS} is 0.5 µs / 1 µs / 2 µs or 3 µs, depending on the SPI configuration.

Due to the tolerance of the short circuit detection, some margin must be taken into account to avoid a wrong short-circuit detection under normal load conditions.

Overcurrent detection

The overcurrent detection is based on the monitoring of the voltage drop across a shunt resistor, which has a much lower thermal coefficient than the R_{DSON} of a MOSFET and a lower tolerance.
These overcurrent thresholds have a tolerance defined in datasheet in Table 25.

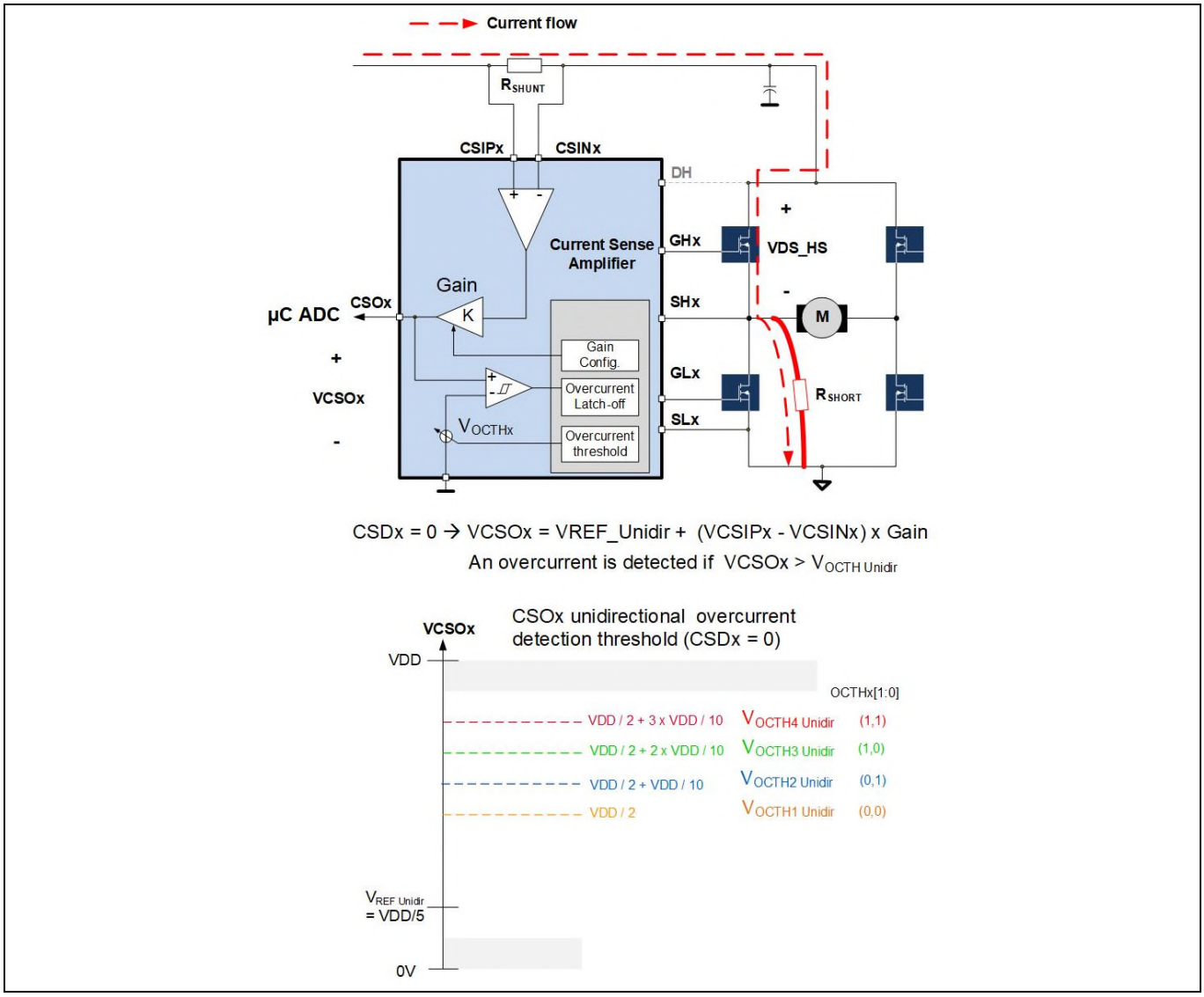

Figure 6 Overcurrent detection with shunt resistor in high-side configuration, current sense amplifier in unidirectional configuration (CSDx = 0)

Due to the higher precision of the overcurrent detection, the overcurrent threshold can be set to a lower level compared to the drain-source overvoltage.

The lower current threshold, which triggers an overcurrent detection, results in lower stress for the MOSFET, and allows the use of longer filter times: t_{FOC} can be typically be set between 6 µs to 100 µs.

1.7 How to configure the sensing of the drain voltage of the high-side MOSFETs?

The TLE92108/4 uses the voltage at the DH pin or at the CSIN1 pin as the drain voltage for each high-side MOSFETs.

The following examples are applicable for the TLE92108. The same considerations can be extended to the **TLE92104 for half-bridges 1-4**.

The correct content of the control bits HBxD depends on the position of the shunt resistors.

A wrong configuration leads to a wrong drain-source overvoltage detection.

Three configurations are considered in this section for the TLE92108.

1.7.1 Both shunt resistors are in high-side configuration

If both shunt resistors are in high-side configuration (refer to **Figure 7**), the drains of the high-side MOSFETs have different voltages due to the voltage drop across the shunt resistors. Therefore, the drain reference for the drain-source overvoltage detection can be set for each MOSFET group:

The drains of HS1-HS4 are connected to CSIN1. The drains of HS5-HS8 **must be** connected to DH

CSIN1 is used as drain voltage reference: HB1D = HB2D = HB3D =HB4D = 1

DH is used as drain voltage reference: HB5D = HB6D = HB7D =HB8D = 0

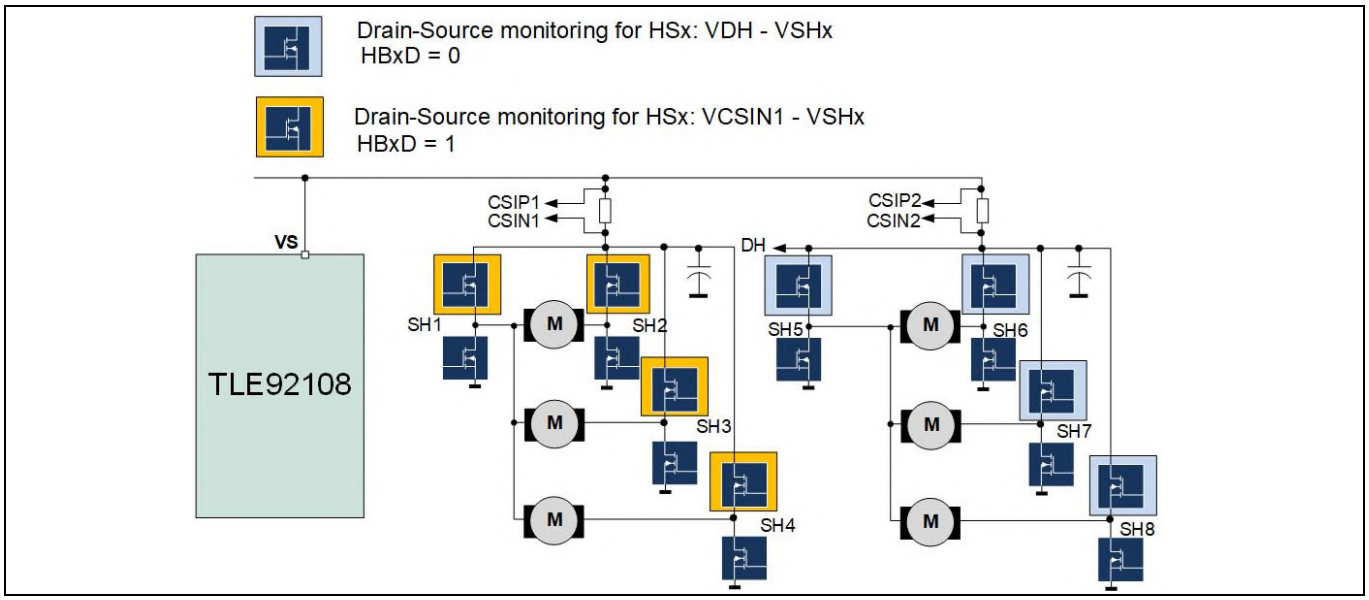

Figure 7 Both shunt resistors are in high-side configuration

1.7.2 Both shunt resistors are in series to the motors

If both shunt resistors are in series to the motors (refer to **Figure 8**):

All high-side drains **must be** connected to DH

HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 0

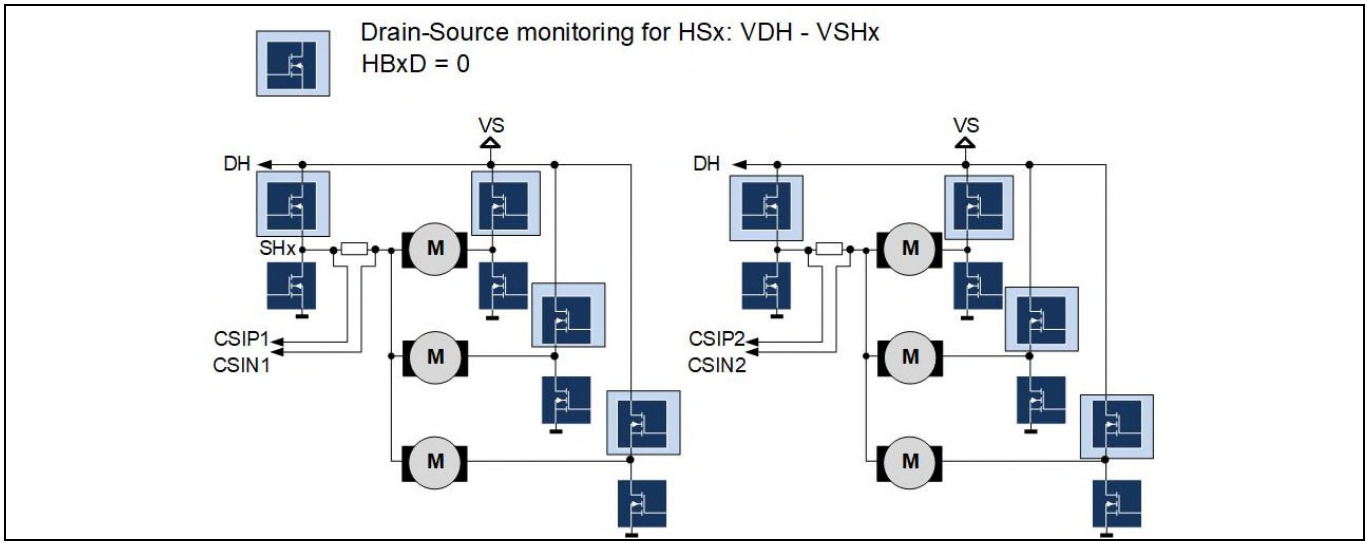

Figure 8 Both shunt resistors are in series to the motor

1.7.3 One shunt resistor is in high-side configuration, one shunt resistor is in low-side configuration

If one shunt resistor is in a high-side configuration, and the other shunt resistor is in a low-side configuration, several solutions are possible. **Figure 9** shows one possibility:

All high-side drains **can be either:**

Connected to CSIN1 and HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 1
or

Connected to DH and HB1D = HB2D = HB3D =HB4D =HB5D = HB6D = HB7D =HB8D = 0

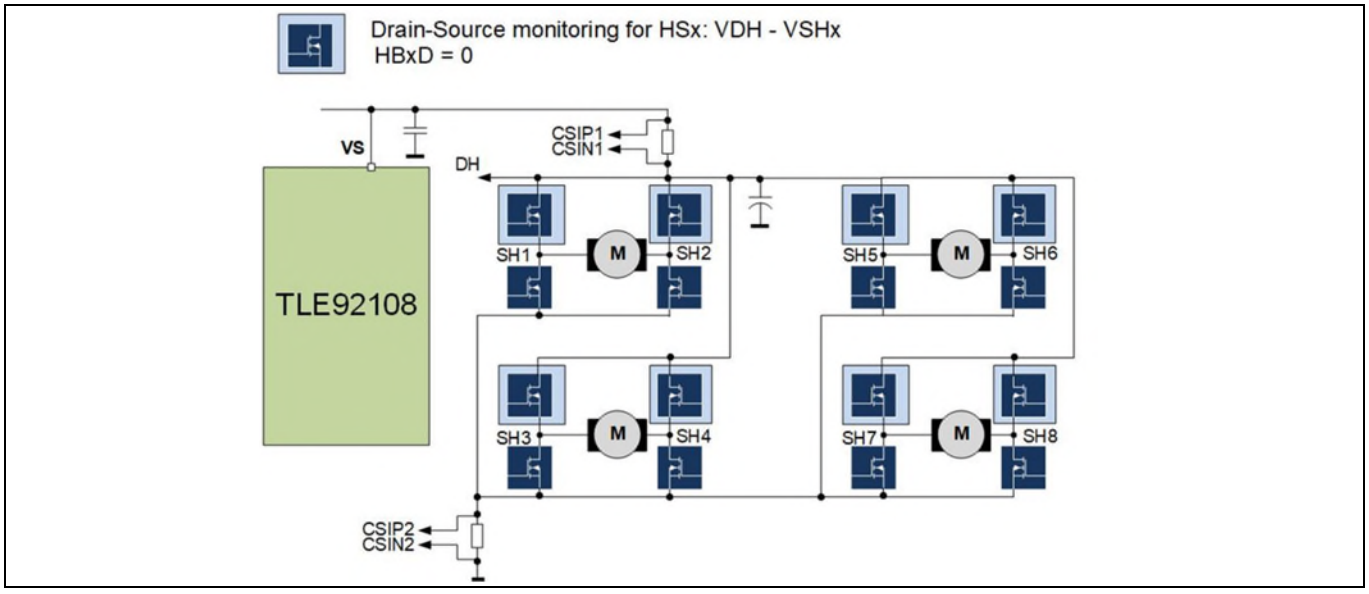

Figure 9 One shunt resistor is in high-side configuration, the other shunt resistor is in low-side configuration

1.8 Why is the gate of the high-side MOSFETs at the VS potential while the MOSFETs are off?

When the bridge driver is **in active mode** (control bit BD_PASS = 0) and both MOSFETs of all half-bridges are off (HBxMODE = 00_B or 11_B), then the MOSFETs are actively turned OFF by the current sinks of the floating gate drivers (refer to **Figure 10**).

Indeed, the current sink between GHx (gate of high-side x) and SHx (source of high-side x) keeps the gate of the high-side MOSFETs discharged, therefore $\boldsymbol{V_{GHx} = V_{SHx}}$.

If no short circuit is present at SHx and the pull-down diagnostic currents are deactivated, then SHx is pulled up to VS by the pull-up diagnostic current (which is also enabled if the bridge driver is in active mode):

$\boldsymbol{V_{GHx} = V_{SHx} = V_s}$, therefore $V_{GHx} \neq 0$ V.

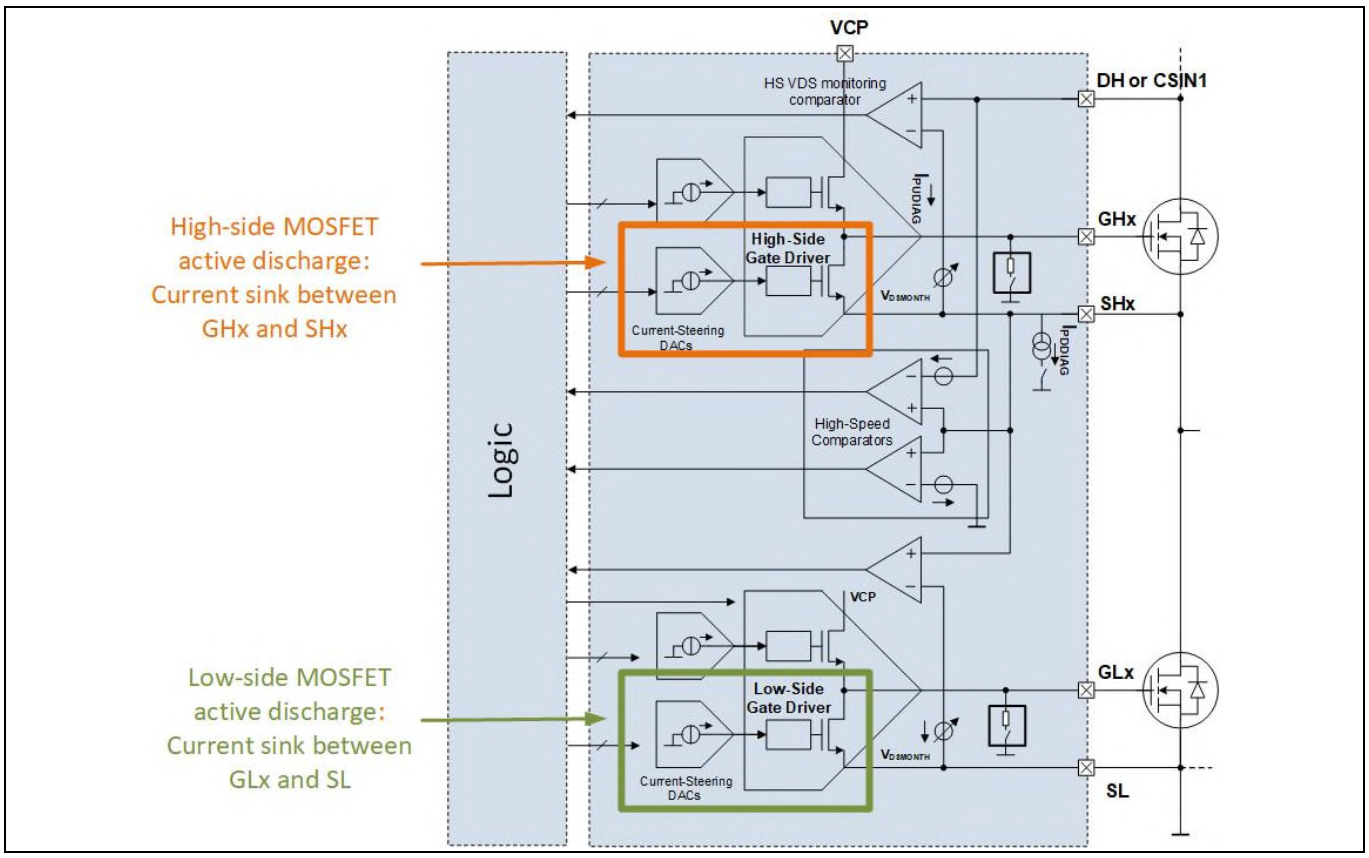

Figure 10 Gate driver active discharge for one half-bridge

Although $V_{GHx} \neq 0$ V, the high-side MOSFET is OFF because $\boldsymbol{V_{GHSx} = V_{GHx} - V_{SH} \sim 0\ V}$

Note: If SHx is pulled down, for example, by a pull-down diagnostic current, then $V_{GHx} = V_{SH}$ = GND. Likewise, a current sink between the GLx and SL pins keeps the gate of the low-side MOSFETs discharged. As V_{SL} is connected to GND, then V_{GLx} = GND.

1.9 What is the difference between active and passive discharge?

The active discharge for the high-side and low-side MOSFETs is described in chapter **1.8** and highlighted in **Figure 10**. In normal mode, the half-bridges are in **passive discharge if BDPASS = 1** and **all HBxMODE = 00_B or 11_B**.

The passive discharge consists of a pull-down resistor:

Between GHx and GND to keep the high-side MOSFETs OFF

Between GLx and GND to keep the low-side MOSFETs OFF

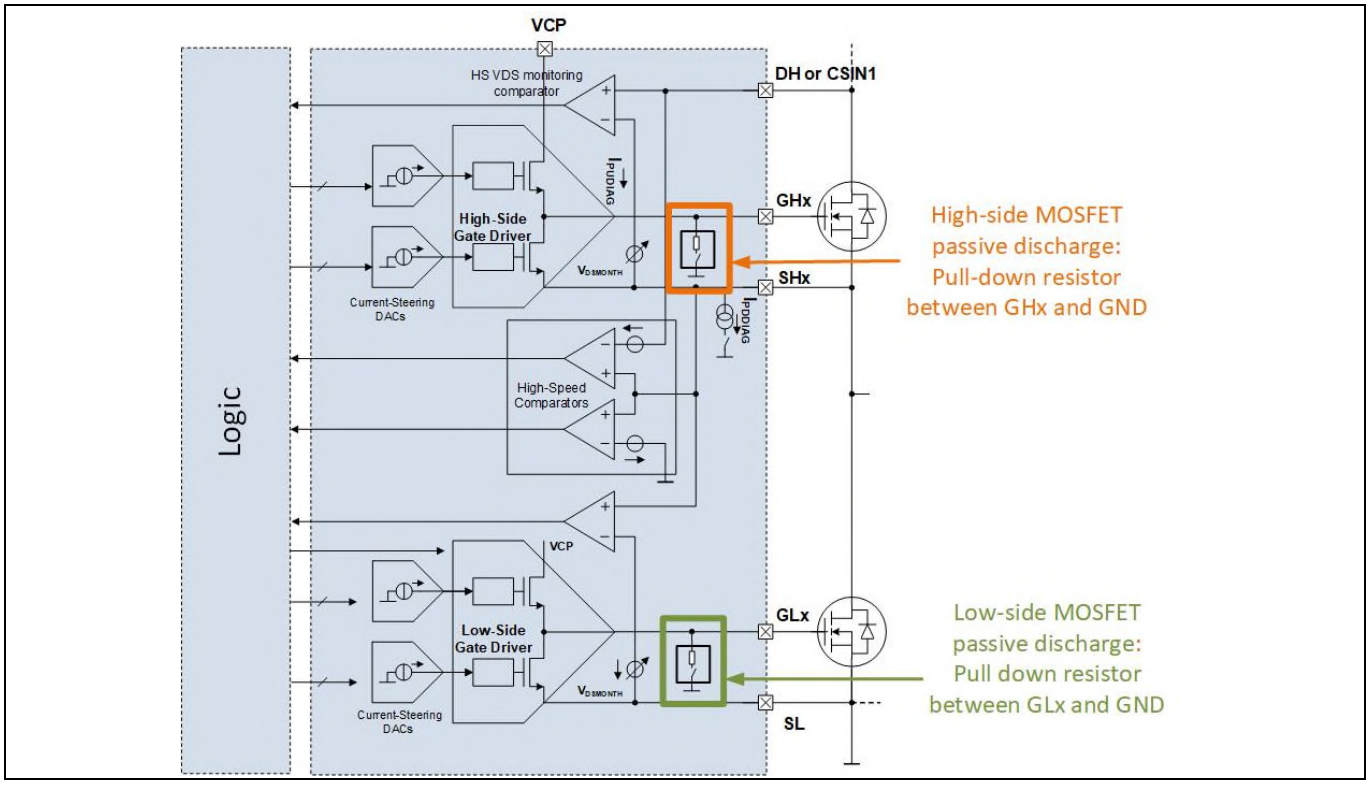

Figure 11 Gate driver passive discharge for one half-bridge

The passive discharge is enabled, for example:

In sleep mode, to reduce the current consumption of the device

In active mode, while no MOSFET is activated, in order to reduce the current consumption

To ensure the termination of GHx and GLx when an active discharge is not possible (for example, when the charge pump is deactivated or if there is charge pump undervoltage):

Over temperature event

VS undervoltage/overvoltage event

Charge pump undervoltage

Fail safe mode

1.10 Why is the power ON reset bit of the global status byte active low?

Unlike other status bits of the global status byte, the (negated) power ON reset (NPOR) bit is active low:

NPOR = 0 after a power-ON reset of the device. NPOR stays 0 until GENSTAT is cleared

NPOR = 1 if GENSTAT is cleared

The arbitrary polarity definition of this bit allows the microcontroller to detect a shorted SDO line to GND: After a clear command on GENSTAT, NPOR = 1(the power ON reset is “cleared”), unless SDO is shorted to GND.

If the SDO line is shorted to GND or the device is in sleep mode, then the microcontroller reads NPOR = 0, despite the attempt to clear the GENSTAT register.

Note: The microcontroller can detect a short circuit to VDD if the most significant bit (MSB) of the Global Status Register is set. According to the SPI protocol of the TLE92108/4, the MSB of the Global Status Register must be 0, unless the serial data input pin (SDI) line is shorted to VDD.

1.11 Are series gate resistors required?

With a classic voltage-controlled gate driver, series resistors or a network of resistors and diodes at the gate of the external MOSFETs are required to control the gate charge and discharge currents, and therefore the MOSFET switching times.

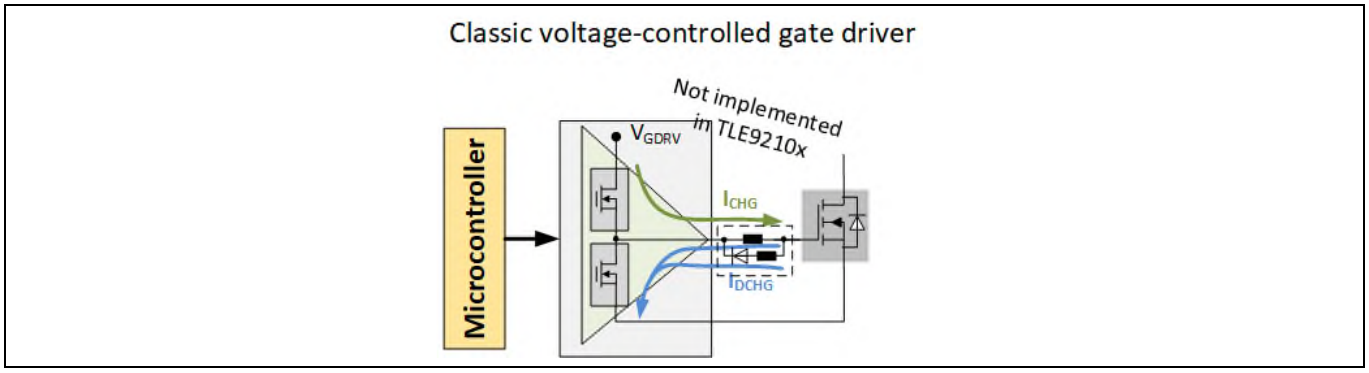

Figure 12 Classic gate driver requiring series resistor or resistor/diode network for the control of the switching times

With the current-controlled gate drivers of the TLE92108/4, series resistors at the gate of the external MOSFETs are not required. This reduces the bill of material and the required PCB area.

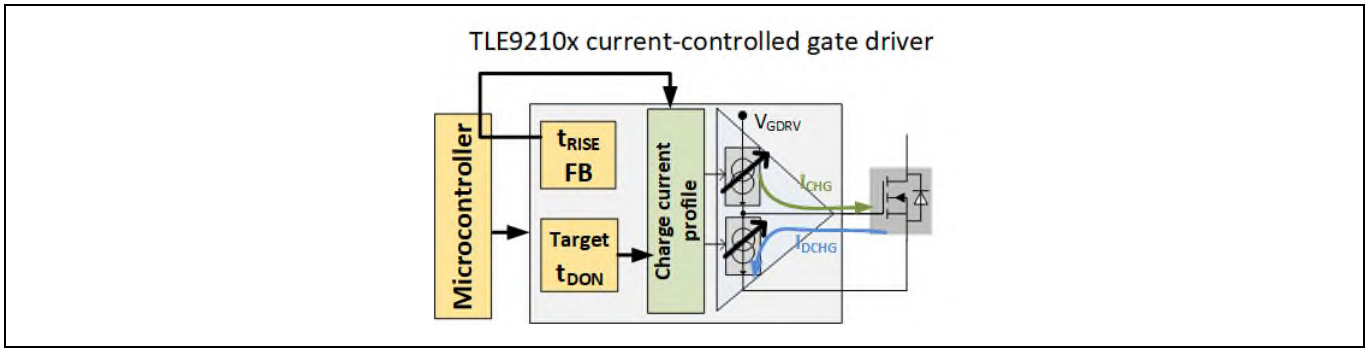

Figure 13 TLE9210x current controlled gate driver without series resistor

If gate series resistors are implemented, it is recommended to keep the resistance below 10 Ω. If the resistance is greater, the voltage drop across the series resistor increases during the turn-ON/OFF of the MOSFET. Meanwhile, the charge/discharge current will be significantly lower than the expected value.

1.12 How to set ICHGST?

It is recommended that the static charge/discharge current ICHGST is high enough to turn ON/OFF the MOSFET within 600 ns to 1 µs.

ICHGST can be roughly calculated. For example: Ichg static = Q_g (tot) / 800 ns

However, verifications must be done in the real application, according to the MOSFET safe operating range and the specified application conditions.

1.13 What is the value of VS quiescent current when VS=13.5V and VDD=0V?

The value of the quiescent current is defined in the product datasheet P_5.5.1, and is valid for VDD in [0.3 V].

1.14 Where should the external series resistor at the input of CSAs be placed?

The filter (including resistors and capacitors) should be placed close to the shunt resistor, so that any noise is filtered directly at the potential source of the disturbance (= shunt).

This prevents the disturbance from spreading through the tracks between the shunt and CSA inputs and couples to other PCB tracks before it is filtered.

It is recommended to define place holders for capacitors close to the device pins, but not populated. Implementing this recommendation can reduce any noise that is coupled from the PCB tracks between the shunt resistor and the CSA inputs.

1.15 Is it possible to drive HS and LS MOSFETs on the same half-bridge independently?

The HS and LS MOSFETs on the same half-bridge cannot be controlled independently by TLE9210x. They are always controlled in pairs as a half-bridge.
For example, during the normal operation of a gate driver, if the HS MOSFET is ON, the LS MOSFET on the same half bridge must be OFF, which applies in both static and PWM modes.

1.16 Is the SDO pin in high impedance during sleep mode?

Yes, SDO is in high impedance during sleep mode.

1.17 Are the charge pumps still working if there is a fault condition?

If there is a fault on a half-bridge driven by the device, the charge pump continues working and supplying other half-bridges that are ON.

The only conditions that deactivate the charge pump are:

- Overvoltage of the supply voltage
- Undervoltage of the supply voltage
- Undervoltage of the CP pin caused by the thermal shutdown

1.18 What SPI sequence is needed to change the rotation direction of a motor?

Initially HS1 and LS2 are enabled:

1. SPI FRAME: 0b 1100 1101 0000 0000 0000 0110

HB1MODE = 10b HS1 ON

HB2MODE = 01b LS2 ON

2. SPI FRAME: 0b 1100 1111 0000 0000 0000 0001

PWM1EN = 1b PWM1 enabled

PWM1_HB = 000b PWM mapped to HB1

Brake before changing direction:

1. SPI FRAME: 0b 1100 1101 0000 0000 0000 0100

HB1MODE = 00b HS1 OFF

HB2MODE = 01b LS2 ON

2. SPI FRAME: 0b 1101 1101 0000 0000 0000 0000

PWM1EN = 0b – PWM disabled

3. SPI FRAME: 0b 1100 1101 0000 0000 0000 0101

HB1MODE = 01b LS1 ON

HB2MODE = 01b LS2 ON

Finally, enable HS2 and LS1:

SPI FRAME: 0b 1100 1101 0000 0000 0000 1001

HB1MODE = 01b LS1 ON

HB2MODE = 10b HS2 ON

It is possible to skip the brake step. In this case, the induced BEMF voltage is added (with the same polarity) to the supply voltage. This will result in doubled inrush current that is observed at switch-ON of the original direction (HS1-LS2). So, the external circuitry and MOSFETs need to be dimensioned accordingly.

1.19 Is there any risk in connecting the EN pin to the VDD pin?

There is no risk in driving the VDD and EN pins together from the same microcontroller I/O pin, because when EN =0, the device is in sleep mode.

1.20 How to set CSAxL if *R*shunt is in series with a motor and the motor changes rotation direction?

If it is not required to optimize the current consumption of the CSA, it is recommended to have CSAxL = 1 (default value). The CSO settling time tSET = 1500 ns (P_7.11.28).

CSAxL must be set to 1 if the shunt is in high-side configuration (that is connected to VS or to an output with an activated high-side), as is shown on the left in **Figure 14**. The PWM is mapped to the low-side MOSFET, and the shunt resistor is connected to VS.

CSAxL must be set to 0 if the shunt is in low-side configuration (that is, connected to GND or to an output with an activated low-side). This configuration helps to optimize current consumption. Wait for about 10µs before sampling ADC, and refer to the datasheet for the value of sinking currents. As shown in the right part of **Figure 14** the PWM is mapped to the high-side MOSFET, and the shunt resistor is connected to GND.

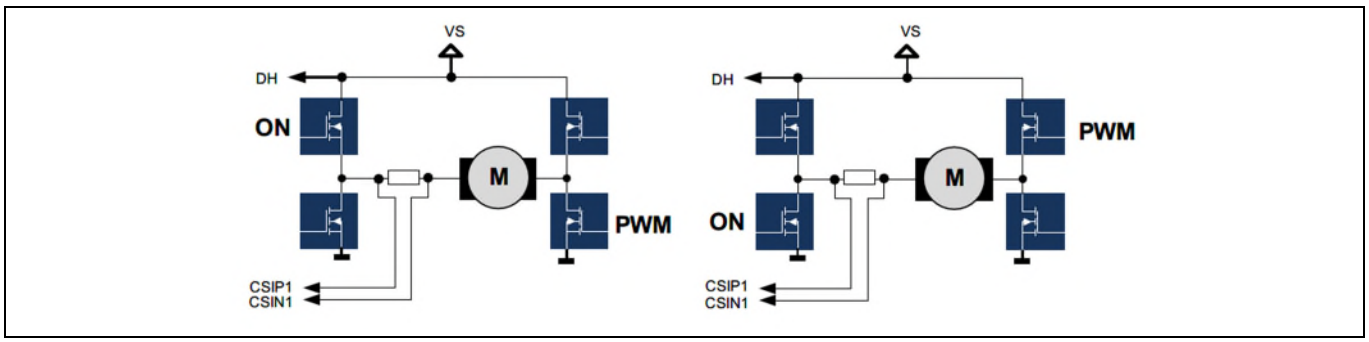

Figure 14 TLE92108 Rshunt in series

1.21 How is the exposed pad connected to GND?

The exposed pad and the substrate of the die are connected through a non-conductive glue.

This exposed pad improves cooling of the device and lowers the power dissipation, which should not be used as an electrical GND.

To achieve the best cooling performance, it is recommended to connect the exposed pad to a GND plane on the PCB.

1.22 What is the purpose of the VS overvoltage brake?

The VS overvoltage brake is designed to protect the device when the motor works as a generator, if:

The motor is in static mode, and an external torque is applied to the rotor, such as the manual closure of the trunk lid or of a sliding door

The motor is running and the active MOSFETs are turned OFF suddenly without any active brake

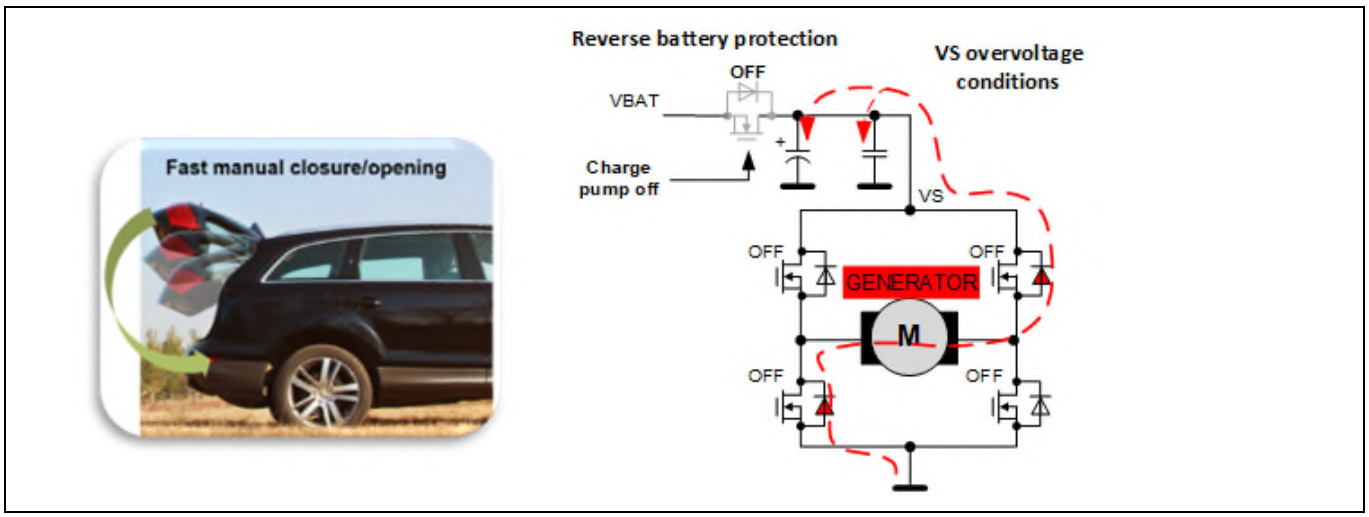

Figure 15 Example of a manually closed trunk lid causing VS overvoltage conditions

In both cases, all half-bridges are OFF, and current flows through the motor and the body diodes of the external MOSFETs. If the charge pump is OFF, the generated current cannot flow back to the battery. The DC link capacitor will be charged and VS voltage increases. Without any protection scheme, some devices might be damaged.

The overvoltage brake feature monitors the VS, and turns on the low-side MOSFETs when VS > $V_{SOV\ PASS\ OFF}$, even if the device is in sleep mode and the charge pump is OFF. As is shown in **Figure 16**, current flows through the motor and the LS MOSFETs.

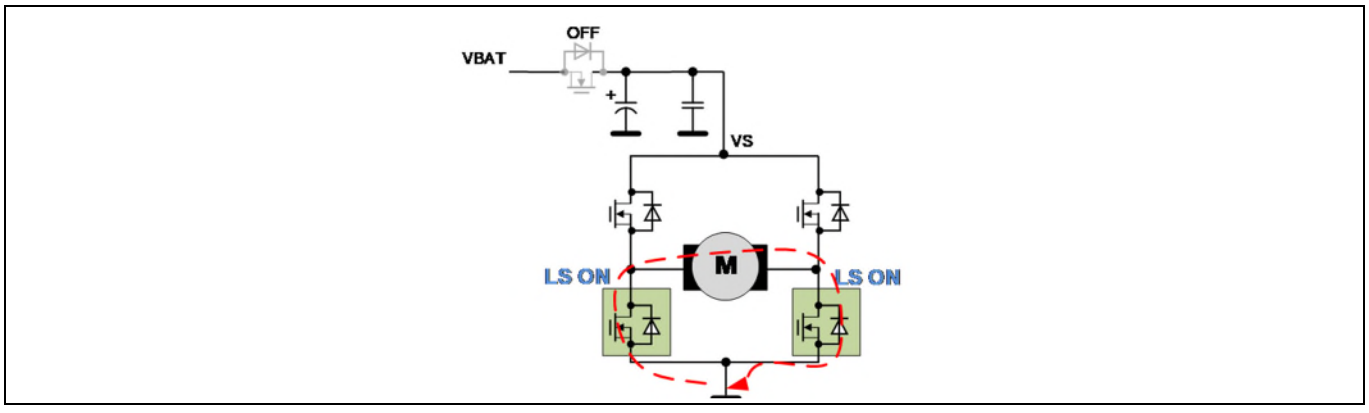

Figure 16 Turn-ON of the low-side MOSFETs during a VS overvoltage brake event

1.23 Does the VS overvoltage brake protect the device when the module is unpowered?

The device is normally not powered during the assembly process of vehicles. If the trunk lid is manually closed, the rotating motor induces BEMF, and the VS will increase.

When the VS is greater than the power-ON reset threshold, the device wakes up and the VS overvoltage brake feature is enabled by default. When the VS overvoltage brake threshold is reached, the LS MOSFETs are turned ON, stopping the increase of the supply voltage.

Therefore, the VS overvoltage brake is available, even if the module is unpowered.

1.24 How to handle the unused gate drivers when the static brake or the VS overvoltage brake is enabled?

SHx must be connected to GND if all the following conditions apply

The half-bridge is not used

The corresponding external MOSFETs are not populated on the board

The VS overvoltage brake or the static brake are used

The passive drain-source overvoltage detection is activated

The SHx of the half-bridges without populated MOSFETs must be connected to GND to avoid an incorrect drain-source overvoltage detection.

Indeed, the device activates all LS MOSFETs during a VS overvoltage with bridge driver in passive mode event or when the static brake is activated.

If an unused SHx is not connected to GND, then SHx is not pulled to low because of the unpopulated MOSFET.

The floating SHx can result in $V_{SHx} - V_{SL} > V_{VDSMONTHx\_BRAKE}$ and a VDS overvoltage error on HBx is detected. Then the device turns OFF all low-side MOSFETs.

GHx and GLx can be left open.

1.25 What is the purpose of the static activation?

The static charge current I_{CHGST} and the static discharge current I_{DCHGST} for static activation are used for two purposes:

To charge and discharge the external MOSFETs, which are not controlled by PWM. These MOSFETs can be turned ON and OFF faster than the MOSFET controlled by PWM, because the single activation is not relevant for the EMC characterization.

I_{DCHGST} is also used to turn OFF the MOSFETs in case of failure.

If a short circuit is detected, two criteria must be considered for the configuration of I_{DCHGST}:

The MOSFETs must be turned OFF fast enough to stay within the safe operating range of the MOSFETs, considering the possible high drain-source current

The MOSFETs must not be turned OFF too fast, because a high current in combination with stray inductances and a fast turn OFF can trigger the MOSFET avalanche

So I_{DCHGST} is individually configurable for each half-bridge driver, and the above-mentioned two criteria can be fulfilled for specific types of MOSFET.

1.26 What is the purpose of the RC filter at the DH pin and what are the recommendations for the dimensioning?

The DH input pin can be configured as the reference voltage for the drain of the high-side MOSFETs. The reference voltage is used for the drain-source overvoltage detection.

The drain-source overvoltage has a digital filter. The low-pass filter R_{DH} and C_{DH} at the DH pin suppresses high-frequency components of the VS voltage and works as an anti-aliasing filter.

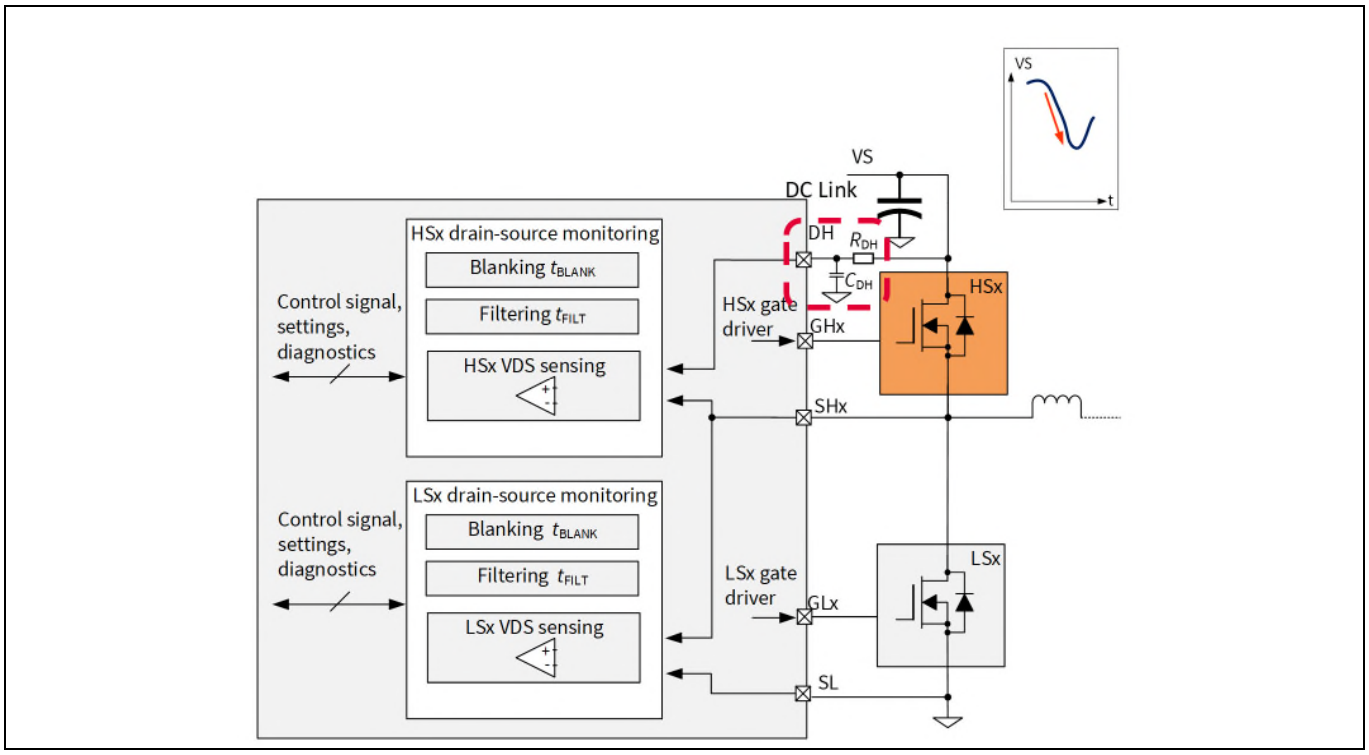

Figure 17 RC filter at the DH pin

The voltage shift between the DC link voltage and the DH pin (V_S - V_{DH}) must be limited during the fluctuations of the battery voltage. A fluctuation in voltage that is too high between V_S and V_{DH} can cause an incorrect detection of drain-source overvoltage of the high-side MOSFETs.

The drain-source comparator of the high-side MOSFETs monitors the voltage difference:

$V_{DH} - V_{SHx} = V_{DH} - V_S + V_S - V_{SHx}$

The term $V_{DH} - V_S$ represents the voltage shift caused by the RC filter during a variation of the V_S.

Figure 18 shows a simulation of the voltage shift between V_{DH} and V_S with a DH filter with a time constant of 1 µs during a V_S drop with a slew rate of -0.5 V/µs during 4 µs. The voltage shift exceeds 400 mV, and can trigger an incorrect detection of drain-source overvoltage on a high-side MOSFET, depending on the configured drain-source overvoltage threshold.

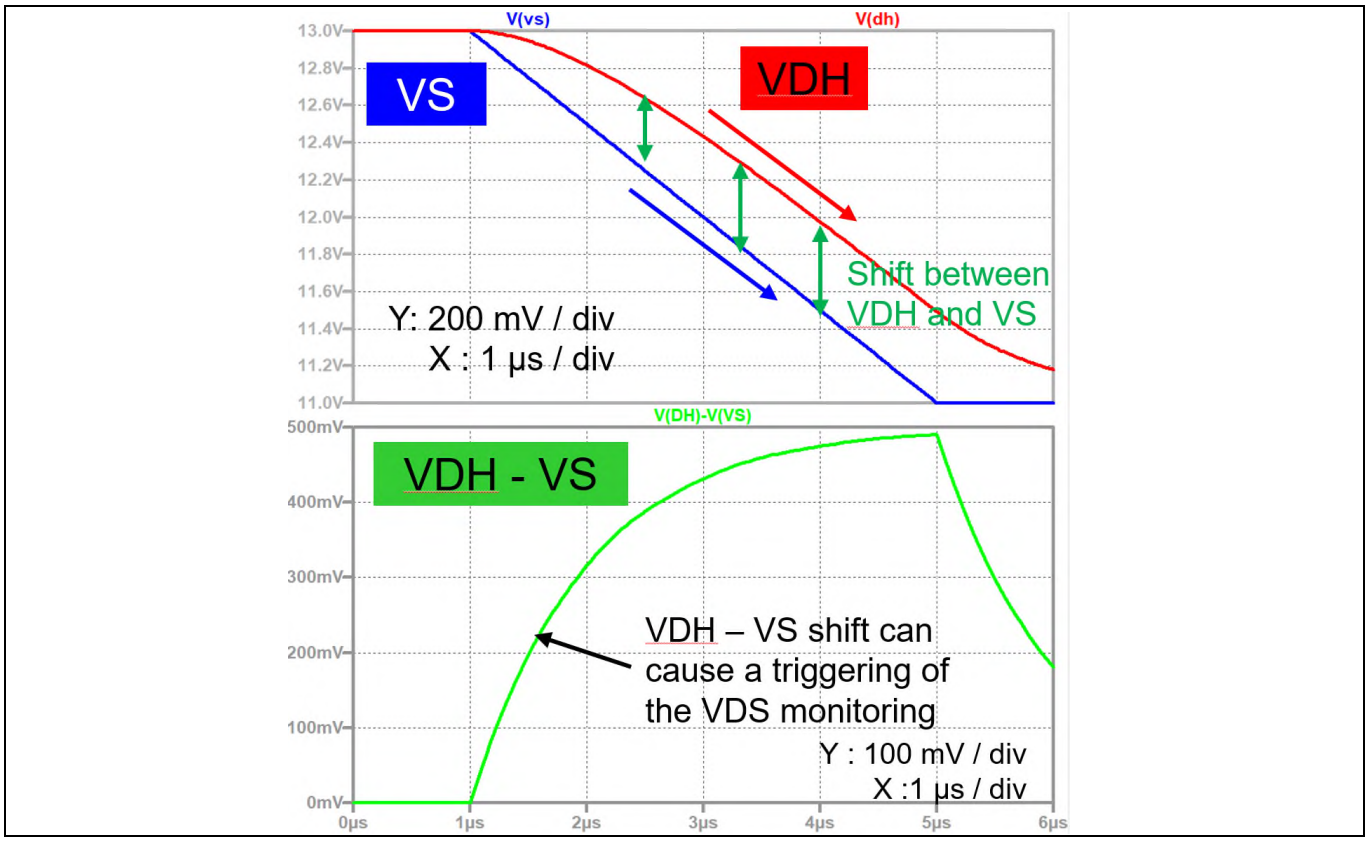

Figure 18 Simulation of the voltage shift between V_S and V_{DH} during a V_S drop with a slew rate of -0.5V/µs during 4 µs with a DH filter with a time constant of 1 µs

The voltage shift VDH- VS is attenuated by decreasing the RC time constant as shown in **Figure 19**.

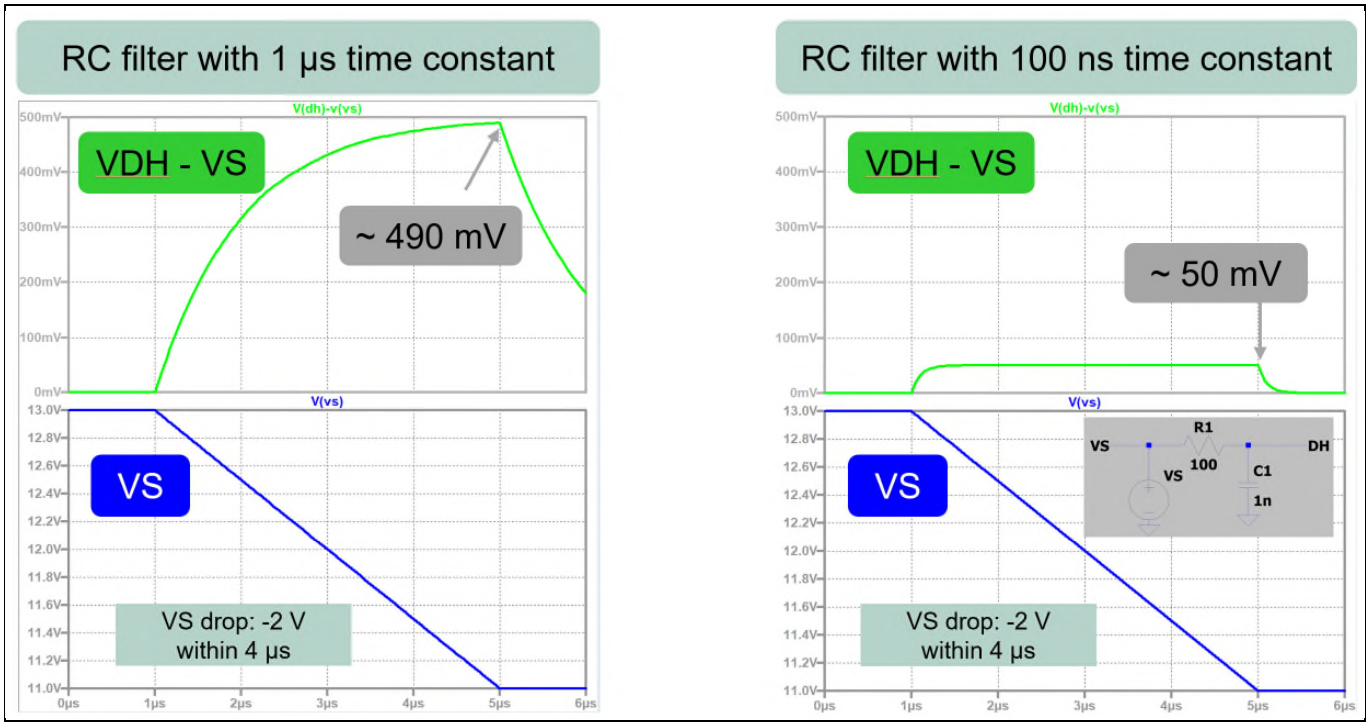

Figure 19 Comparison of the voltage shift between V_S and V_{DH} during a VS drop with DH filter with 1µs and 100ns time constants

It is recommended to use an RC time constant, which is significantly lower than the filter time of the drain-source monitoring (t_{FVDS}). If t_{FVDS} = 1…2 µs, it is recommended to keep the RC time constant in the range of 100 to 400 ns. For example:

R_{DH} = 100 to 330 Ω

C_{DH} = 1 nF

1.27 What is the gain drift?

The gain drift is the drift of the gain after calibration, resulting from the device ageing and from the temperature drift (T_j = -40°C to 150°C).
For example, the gain of the CSA is calibrated at 25°C with two-point calibration (that is, using two load currents).

1.28 How to handle unused pins when brake mode is enabled?

Recommendation for unused pins GHx, SHx and GLx:

GHx: must be left open

SHx: must be connected to GND

GLx: must be left open

Connecting SHx pins to GND when the brake mode is activated prevents an incorrect detection of a drain-source overvoltage on the unconnected LSx.

1.29 How do the gate drivers behave during the first PWM period?

For example, in a half bridge application, if we PWM on HS MOSFET, and the device is initialized and enabled: When the first PWM arrives, as is shown in **Figure 20**:

Initially, before the first rising edge comes, HS and LS MOSFETs are OFF
The HS MOSFET is turned after the first rising edge, and the LS MOSFET is still OFF
The HS MOSFET is turned off after the first falling edge
After tCCP, the LS MOSFET is turned ON

This frame is different from other frames in other PWM periods, as is shown in **Figure 21**.

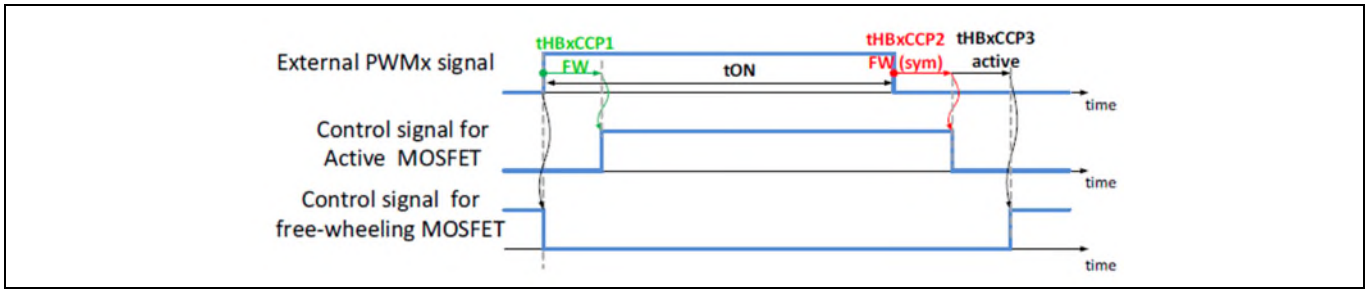

Figure 20 Gate driver control signal during the first PWM

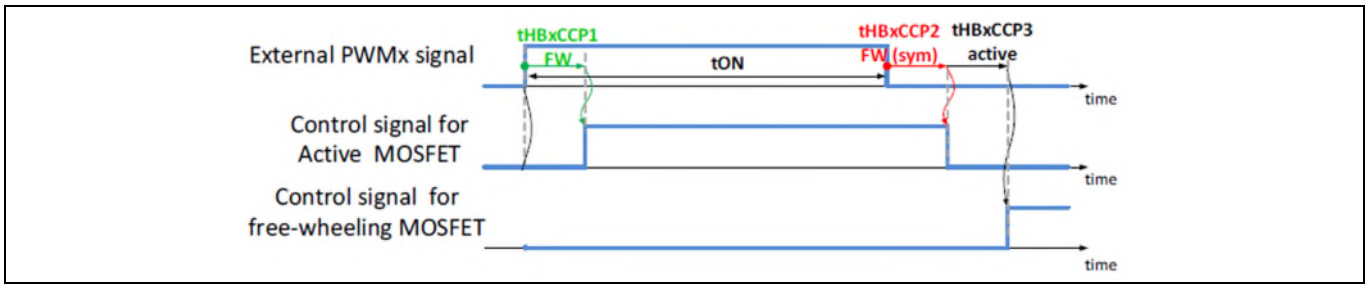

Figure 21 Gate driver control signal after the first PWM

2 Terminology

Table 2 Table of abbreviations

Abbreviation	Description
FW	Free wheeling
SH	Source of high side
HS	High side
LS	Low side
VS	Voltage supply
WD	Watch dog
DS	Drain-source
OV	Overvoltage
CSA	Current sense amplifier
GND	Ground
MSB	Most significant bit
SDI	Serial data input
T_j	Junction temperature

Revision history

Document version	Date of release	Description of changes
1.0	2019-09-23	First release
1.1	2020-08-24	Document extended to TLE92104 Chapter 1.7: Updated cross-references to figures Chapter 1.7.1: corrected bit setting
1.2	2021-06-21	Document extended Added chapters 2.10-26
1.3	2022-07-14	Document extended Added chapters 27-29 Earlier chapters updated

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Edition 2022-07-15

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
Z8F66967920

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