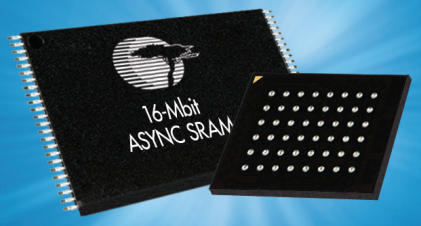
CYPRESS

# FAST SRAM WITH POWERSNOOZE™

## INTEGRATES HIGH SPEED AND LOW POWER




PRODUCT OVERVIEW

### COMBINES BEST FEATURES OF FAST AND LOW-POWER SRAM

Cypress's existing Asynchronous SRAM product portfolio includes two device families with distinct features. Using the latest process technology, Cypress now offers a new family of devices that combine the access time of Fast Asynchronous SRAM with a unique ultra low-power sleep mode (PowerSnooze™).

### SOFT-ERROR MITIGATION IN ASYNCHRONOUS SRAM

Cypress's latest generation asynchronous SRAM devices have a hardware ECC block that performs all ECC-related functions in line, without affecting the access time performance of the device. This is supplemented by a 16-bit interleaving scheme to prevent the occurrence of multi-bit errors. Together these features achieve FIT rates of less than 0.1 FIT/Mbit.

### CYPRESS'S LATEST INNOVATION: POWERSNOOZE™

Fast SRAM with PowerSnooze eliminates the tradeoff between performance and power consumption in Asynchronous SRAM applications. In this new family of devices, the best features of existing family of products are achieved through the provision of a novel ultra low-power sleep mode called PowerSnooze. PowerSnooze is an additional operating mode to standard Asynchronous SRAM operating modes (Active, Standby, and Data-Retention). Deep sleep pin (DS#) enables switching of device between the high performance active mode and the ultra low-power PowerSnooze mode. With deep sleep current as low as 22 µA on 16-Mbit devices, Fast SRAM with PowerSnooze combines the best features of fast and low-power SRAM in a single device.

### PERFORMANCE AND POWER TRADEOFF IN EXISTING ASYNCHRONOUS SRAM FAMILY OF PRODUCTS

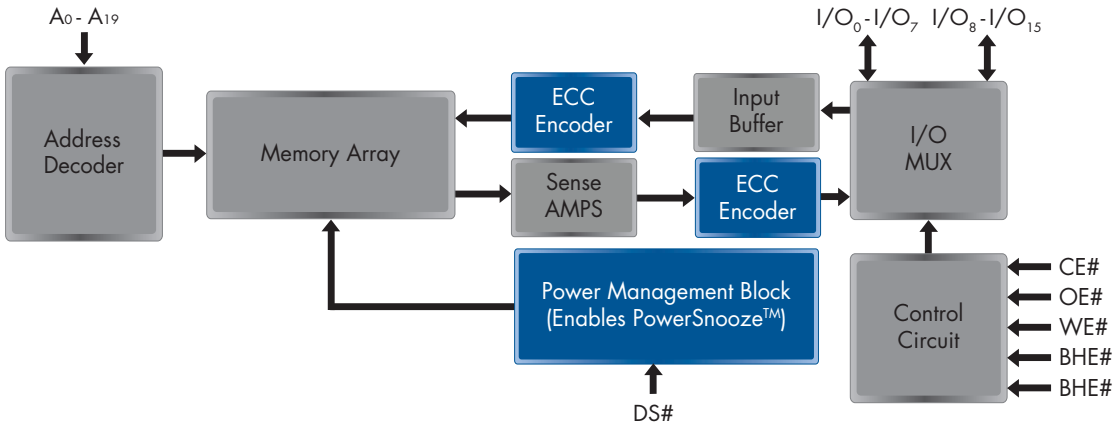
| Parameters | Cypress 16-Mbit Fast SRAM | Cypress 16-Mbit Low-Power SRAM |
|---|---|---|
| Access Time | 10 ns, 15 ns | 45 ns, 55 ns, 70 ns |
| Active Current | >100 mA | <50 mA |
| Standby Current | >20 mA | <25 uA |

### ADVANTAGES

- Eliminates tradeoff between performance & power consumption
- Industry leading access time: 10 ns (16-Mbit FAST)
- Deep sleep current: 22 uA (16-Mbit)
- Highest level of reliability: Soft-Error Rate < 0.1 FIT/Mbit
- On-chip Error Correcting Code (ECC) to detect and correct all single bit errors
- Bit-interleaving to avoid multi-bit upsets
- Multiple configurations: x16, and x32
- Multiple operating voltages: 1.8 V, 3 V, 5 V
- Available in industry standard package options
- Fit-form-function compatible with current generation Fast SRAM packages



CYPRESS PERFORM




Fast SRAM with PowerSnooze Block Diagram

## KEY FEATURES OF FAST SRAM WITH POWERSNOOZE

| | |
|---|---|
| Density | 16-Mbit |
| Process Technology | 65-nm |
| On-chip ECC | Yes, (38,32) Hamming Code for single-bit error correction |
| Soft Error Rate (SER) | <0.1 FIT/Mbit |
| Bus Width | x16, x32 |
| Voltage Options | 1.8 V, 3 V, 5 V |
| Access Time | 10 ns |
| Operating Current | 110 mA@ 85°C |
| Standby Current | 30 mA@ 85°C |
| Deep Sleep Current | 22 uA@ 85°C |
| Packages: | 48-pin TSOP I, 48-ball VFBGA, 54-pin TSOP II, 119-ball BGA |
| Temperature Grade: | Industrial, Automotive |

## 16-MBIT FAST ASYNCHRONOUS SRAM WITH POWERSNOOZE

| Part Number | Organization | Voltage | Speed | Package | Temperature Grade |
|---|---|---|---|---|---|
| CY7S1061G | 1 M x 16 | 1.8 V, 3 V, 5 V | 10 ns, 15 ns | 48-VFBGA, 48-TSOP I, 48-TSOP II | Industrial |
| CY7S1061GE | 1 M x 16 | 1.8 V, 3 V, 5 V | 10 ns, 15 ns | 48-TSOP I | Industrial |
| CY7S1062G | 512 K x 32 | 1.8 V, 3 V | 10 ns, 15 ns | 119-BGA | Industrial |

## APPLICATIONS

PLCs • Test Equipment • Industrial Automation • Multi-Functional Printers • Servers • Switches and Routers • Audio/Video Applications • Handheld Devices • Medical Devices • Gaming Machines • Military/Automotive Electronics

## GET STARTED NOW

For more information please visit us at www.cypress.com/go/AsyncSRAM

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