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FUJITSU

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FR Family FR80
32-BIT MICROCONTROLLER
MB91625/MB91635A/MB91640A/MB91645A/MB91660 Series

A/D Converter Conversion Time Setting

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Revision History

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1 Introduction

This application note explains important points on the functionality used in the A/D converter and settings for the A/D conversion time for the FR Family MB91625/MB91635A/MB91640A/MB91645A/ MB91660 Series 32-bit microcontrollers.

2 Internal Block Architecture of A/D Converter

The conversion for the A/D converter used in the MB91625/MB91635A/MB91640A/ MB91645A/ MB91660 Series utilizes a successive approximation conversion method with an RC-type sample and hold circuit. The basic A/D converter specifications for each series are identical. However, the number of units and channels for the A/D converter are different for each microcontroller in the series. See the hardware manual of each microcontroller for individual specifications.

This section covers the MB91635A Series, and Figure 2-1 shows the A/D converter block diagram. The A/D converter for the MB91635A has built-in two 10-bit A/D converters capable of assigning 31 channel analog inputs to each unit.

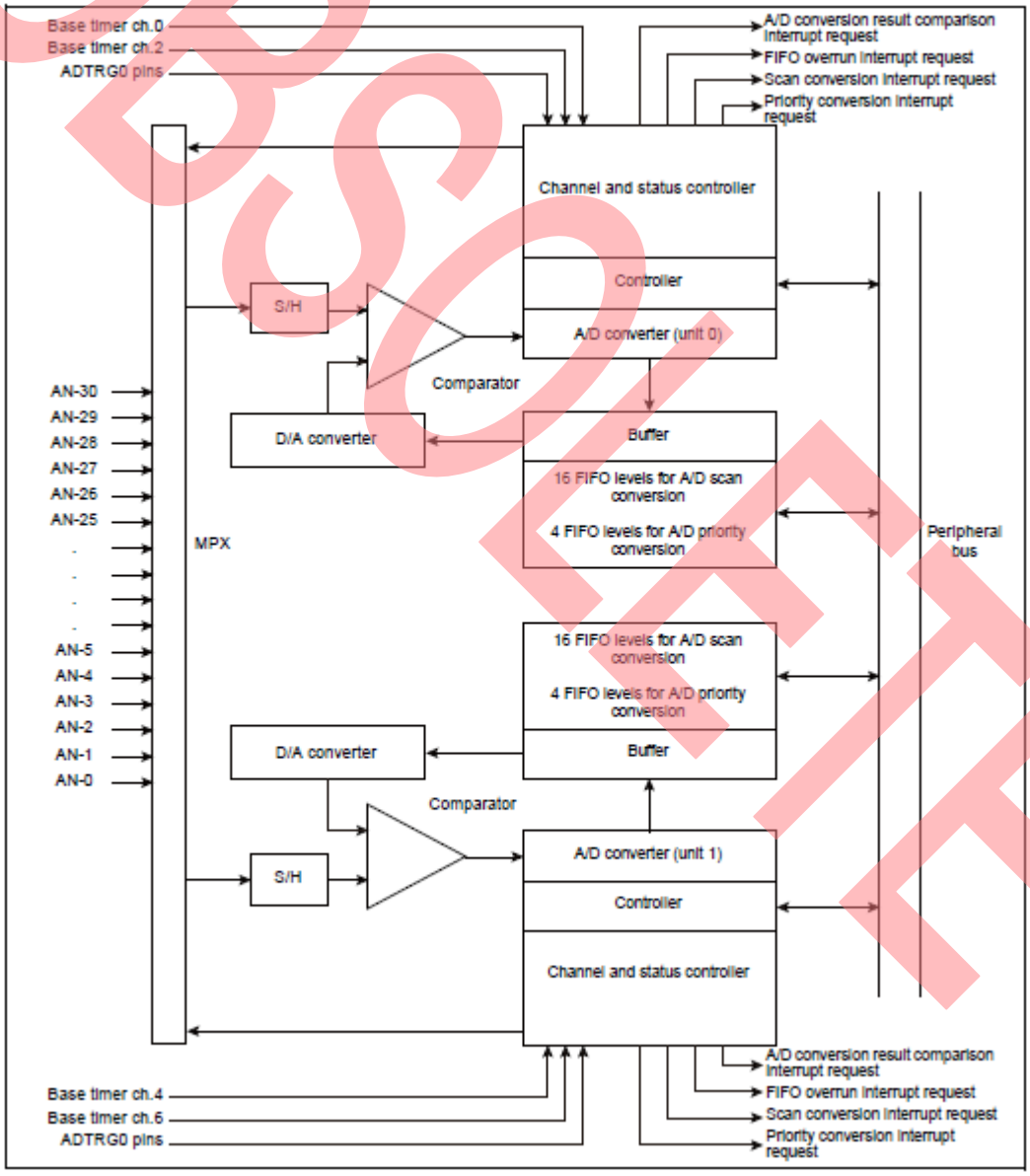

Figure 2-1 Block diagram of 10-bit A/D converter (MB91635A Series)

3 Register for Setting A/D Conversion Time

3.1 Sampling Time Setting Register (ADSTx0, ADSTx0)

The A/D conversion time is configured from the sampling and compare times. The sampling time setting register is to set the sampling time. After A/D conversion is started, the input voltage is sampled by the sample and hold (S/H) circuit. The sampling time setting register starts sampling and sets the input voltage storage time. The bit configuration for the sampling time setting register is shown in the chart below.

Sampling time setting registers 00, 01 (ADST00, ADST01)

bit	15	14	13	12	11	10	9	8
	STX01	STX00	ST05	ST04	ST03	ST02	ST01	ST00
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	0	0	0	0	0

Sampling time setting registers 10, 11 (ADST10, ADST11)

bit	7	6	5	4	3	2	1	0
	STX11	STX10	ST15	ST14	ST13	ST12	ST11	ST10
Attribute	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	0	0	0	0	0

R/W: Read/Write

Chart 3-1 Bit configuration for the sampling time setting register (ADSTx0, ADSTx0)

- [bit15, bit14] / [bit7, bit6] : STXx1, STXx0 (Sampling time N-times setting bit)

  The value set by STx5 to STx0 bit is multiplied N (x1, x4, x8, x16) times.

STXx1	STXx0	Description
0	0	Setting value x1
0	1	Setting value×4
1	0	Setting value×8
1	1	Setting value×16

- [bit13 to bit8] / [bit5 to bit0] : STx5 to STx0 (sampling time setting bit)

  Sets the value to set the sampling time.

The sampling time set by this register is calculated with the following formula.

Sampling time = Peripheral clock (PCLK) cycle × (ST+1) × STX

3.2 Compare Time Setting Register (ADCTx)

A/D conversion time is configured from the sampling and compare times. The compare time setting register is the register that sets this compare time. The size of the analog voltage sampled by the sample and holder (S/H) circuit and the size of the DA converter are compared by the comparator. The digital values for the DA converter are increased or decreased depending on the results of comparison. The final corresponding digital value gives the converted digital value and the conversion time is set in the compare time setting register. The bit configuration for the compare time setting register is shown in the chart below.

bit	7	6	5	4	3	2	1	0
	Undefined	Undefined	Undefined	Undefined	Undefined	CT2	CT1	CT0
Attribute	-	-	-	-	-	R/W	R/W	R/W
Initial value	X	X	X	X	X	1	1	1

R/W: Read/Write

-: Undefined

X: Undefined

Chart 3-2 Bit configuration for the compare time setting register (ADCTx)

- [bit2 to bit0] : CT2 to CT0 (compare time setting bit)

  Determines the value to set the compare time.

The compare time is calculated using the following formula.

Compare time = {(CT+1)×10+4}× Peripheral clock (PCLK) cycle

4 Analog Input and External Circuit

The following figure shows an analog input pin in an equivalent circuit.

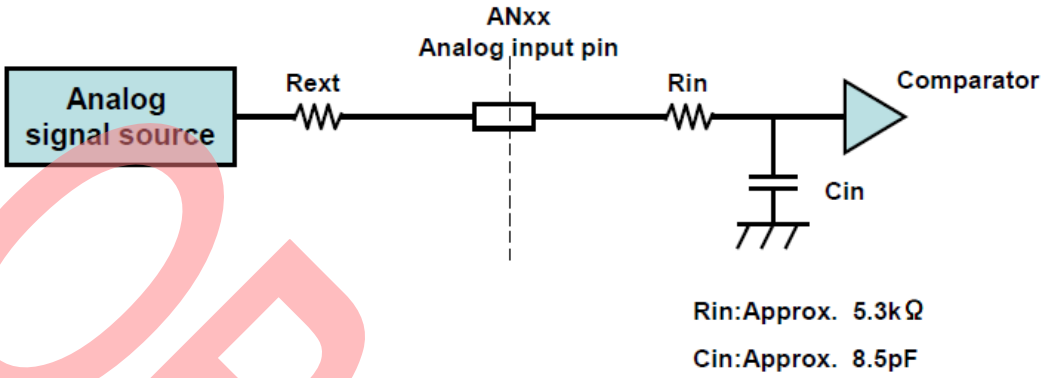

Figure 4-1 Analog input and external circuit

The functions of Rext, Rin, Cin of the equivalent circuit are defined as follows.

Rext: external by the user system impedance

Rin: analog switch ON resistor

Cin: capacitor for storing analog voltage

These values are required for sampling time setting and compare time setting. When the external impedance is large, sampling the capacitor takes time. Also, if operating at a low-rate during the comparing process, holding the sampling analog voltage may be impossible. Be sure to take these points into consideration before setting the conversion time of the A/D converter.

5 A/D Conversion Time (sampling time + compare time) Setting Precautions

5.1 Sampling time setting precautions

When setting the A/D sampling time, be sure to consider the C and R-values that are used in the sampling circuit. Also, the output impedance of the external circuit that is connected to the analog input affects the A/D converter sampling time. Be sure to take this into consideration before setting the sampling time.

The sampling time is calculated using the following formula.

$$Ts = (Rin + Rext) \times Cin \times 8 \quad \cdots\cdots A)$$

Ts: sampling time

Rin: A/D input resistance

Cin: A/D input capacitance

Rext: external circuit impedance

”8”: CR coefficient that suppresses error margin to within a range of 1LSB

(Ex.) External impedance (Rext)= sampling time (minimum value) at 3.7kΩ. If a value is assigned to each variable in formula A),

$$Ts \geq (5.3k\Omega + 3.7k\Omega) \times 8.5pF \times 8 = 612ns$$

Therefore, in this example, the A/D converter sampling time must be adjusted to 612ns or higher. Set the value that satisfies the minimum value of the sampling time for the sampling time setting register.

If the A/D converter sampling time is insufficient, this insufficient voltage will become the error margin. To guarantee the accuracy of the A/D converter, ensure there is a sufficient sampling time.

5.2 Compare time setting precautions

Loss of the electric charge in the capacitor that was charged by the A/D sampling circuit happens because of a slow leakage current during compare time. The error margin produced as a result of this phenomenon affects the accuracy of A/D data. The effects can be substantial if the A/D is operated at a low-rate. Therefore, pay close attention when setting the compare time.

Calculate the compare time by applying this phenomenon to the A/D converter for the MB91625/MB91635A/MB91640A/ MB91645A/MB91660 Series. Each type of A/D converter uses an intrinsic transistor in the internal sample and hold circuit. The intrinsic transistor has a leakage current of 5nA (at highest temperature and lowest power).

$i = 5[nA]$ ·····1)

The A/D input capacitance is

$C = 8.5[pF]$ ·····2)

The voltage drop (⊿V) after time (⊿t) when the current (i) flows from capacitance (C) is given in the following formula.

$⊿t = C \times ⊿V / i$ ·····3)

When 1LSB (3mV) fall time of the A/D converter is entered into formula 3),

$⊿t = 8.5[pF] \times 3[mV] / 5[nA]$

$= 5.1[\mu s]$

The maximum value of the A/D compare time is given in the results above. If the A/D compare time delays more than 5.1[µs], the A/D conversion error increases. Operating the A/D compare time at 5.1µs or less is recommended so that the A/D conversion accuracy does not decrease.

The A/D compare time is calculated using the formula below, found in paragraph 3-2.

Compare time = [(CT+1)×10 + 4] ×PCLK cycle ·····B)

(CT : compare time setting bit)

When the compare time (max. value) and CT (min. value) are entered into formula B), the PCLK cycle (max. value) can be calculated.

Compare time (max. value) = 5.1[µs]

CT (min. value) = 0

Enter these values into formula B).

5.1[µs] ≥ {(0+1) ×10 + 4} ×PCLK cycle (max. value)

PCLK cycle (max. value) ≤ 5.1[µs]/14 = 364[ns] (frequency notation of 2.75MHz)

Based on the above results, the PCLK cycle (max. value) equals 364[ns].

If the A/D compare is operated using a clock with more delay than the PCLK cycle (max. value), the A/D converter accuracy decreases. If the A/D converter is used, operating the PCLK cycle at a high-rate above 364[ns] is recommended so that the A/D converter accuracy does not decrease.

Be sure to take the above-mentioned points into consideration before setting the conversion time of the A/D converter.