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Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



FR60, CY91460N Series, 32-bit Microcontroller Datasheet

CY91F463NA is a line of the general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. CY91F463NA uses the FR60 CPU which is compatible with the FR CPUs.

CY91F463NA contains the LIN-USART and CAN controllers.

Note: CY91F463NC improved the features of CY91F463NA and updated the sector map for the flash memory. Please select CY91F463NC for the future development.

Features

FR60 CPU

- 32-bit RISC, load/store architecture, five-stage pipeline
- Maximum operating frequency: 80 MHz (oscillator frequency: 4 MHz; oscillator frequency multiplier: 20 (PLL clock multiplication method))
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation instructions, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi load store instructions: Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
Signed 32-bit multiplication: 5 cycles
Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving): 6 cycles (16 priority levels)
- Harvard architecture allowing program access and data access to be executed simultaneously
- Instructions compatible with the FR family

Internal Peripheral Resources

- Flash memory capacity : 288 Kbytes
- Internal RAM capacity: 8 Kbytes (Data RAM) + 2 Kbytes (Instruction/data RAM)
- General-purpose port: Maximum 48 ports
- DMAC (DMA Controller)
Maximum of 5 channels for able to operate simultaneously
2 transfer sources (internal peripheral/software)
Activation source can be selected by programs

Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)

Transfer mode (burst transfer/step transfer/block transfer)

Transfer data size selectable from 8/16/32-bit

Multi-byte transfer capable (by programs)

DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)

- A/D converter (sequential comparison)

10-bit resolution: 8 channels

Conversion time: 1 μ s (using at 5 V) , 3 μ s (using at 3.3 V)

- External interrupt inputs: 10 channels

- Bit search module (for REALOS)

Function to search from the MSB (most significant bit) for the position of the first "0", "1" or changed bit in a word

- LIN-USART (full duplex double buffer): 4 channels

Clock synchronous/asynchronous selectable

Sync-break detection

Internal dedicated baud rate generator

- I²C bus interface (Supports 400 kbps): 2 channels

Master/slave transmission and reception

Arbitration function, clock synchronization function

- CAN controller (C-CAN): 2 channels

Maximum transfer speed: 1 Mbps

32 transmission/reception message buffers

- 16-bit PPG timer: 8 channels

- 16-bit reload timer: 4 channels + 1 channel (exclusive A/D converter)

- 16-bit free-run timer: 4 channels

- Input capture: 4 channels

- Output compare: 4 channels
- 8/16-bit up/down counter: 2 channels (8-bit)/1channel (16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption mode: Sleep/stop mode function

Package: LQFP-64 (LQG064)

CMOS 0.18 μ m technology

3.3 V only power supplies or 5 V only power supplies

Operating temperature range:

– 40°C to + 85°C (using at 5 V)

– 40°C to + 105°C (using at 3.3 V)

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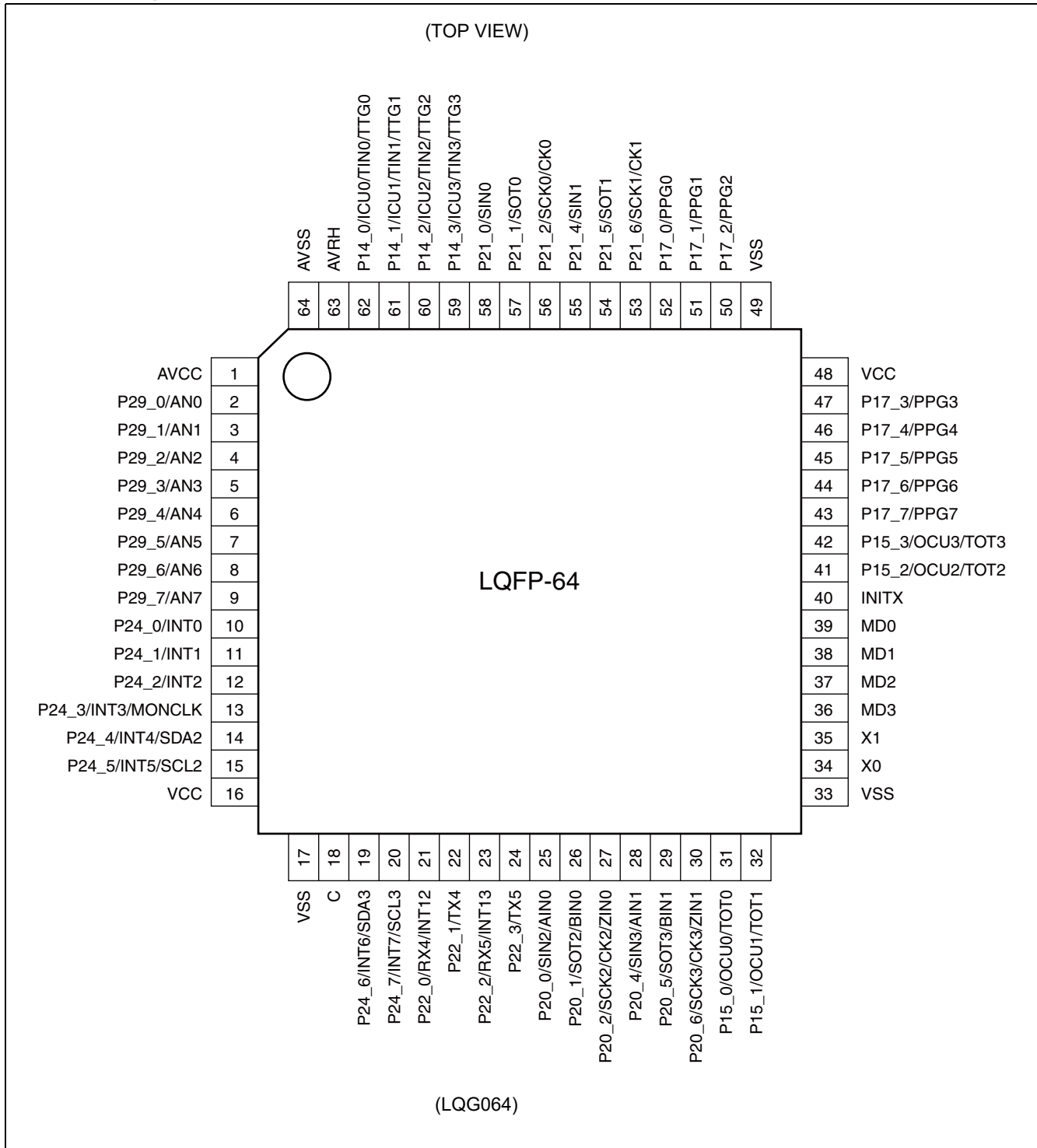
1. Product Lineup

Part Number Parameter	CY91V460A	CY91F463NA CY91F463NC
Max core frequency (CLKB)	80 MHz	
Max resource frequency (CLKP)	40 MHz	
Max external bus frequency (CLKT)	40 MHz	-
Max CAN frequency (CLKCAN)	20 MHz	
Technology	0.35 μm	0.18 μm
Watchdog Timer	Yes	No
Watchdog Timer (CR oscillator)	Yes (disengageable)	Yes
Bit search	Yes	
Reset input (INITX)	Yes	
Hardware standby input (HSTX)	Yes	No
Clock modulator	Yes	
Low-power mode	Yes	
DMAC	5 channels	
MAC (μDSP)	No	
MMU/MPU	MPU (16 channels) ^[1]	MPU (4 channels) ^[1]
Flash memory	Emulation SRAM 32-bit read data	288 Kbytes
Flash protection	-	Yes
Data RAM	64 Kbytes	8 Kbytes
Instruction/data RAM	64 Kbytes	2 Kbytes
Flash-cache (instruction cache)	16 Kbytes	4 Kbytes
Boot-ROM/BI-ROM	4 Kbytes fixed	4 Kbytes (BI-ROM)
Real-time clock	1 channels	
Free-run timer	8 channels	4 channels
ICU	8 channels	4 channels
OCU	8 channels	4 channels
16-bit reload timer	8 channels	4 channels + 1 channel
16-bit PPG	16 channels	8 channels

Part Number Parameter	CY91V460A	CY91F463NA CY91F463NC
16-bit PFM	1 channel	No
Sound Generator	1 channel	No
8/16-bit up/down counter	4 channels (8-bit) / 2 channels (16-bit)	2 channels (8-bit) / 1 channel (16-bit)
C_CAN	6 channels (128 message buffers)	2 channels (32 message buffers)
LIN-USART	4 channels + 4 channels (FIFO) + 8 channels	4 channels
I ² C (400 kbps)	4 channels	2 channels
FR external bus	Yes (32-bit address, 32-bit data)	No
External interrupt	16 channels	10 channels
NMI interrupts	Yes	No
Stepping motor controller (SMC)	6 channels	No
LCD controller (40 × 4)	1 channel	No
10-bit A/D converter	32 channels	8 channels
Alarm comparator	2 channels	No
Clock supervisor	Yes	No
Main clock oscillator	4 MHz	
Sub clock oscillator	32 kHz	-
CR oscillator	100 kHz	100 kHz / 2 MHz
PLL	× 20	
DSU4	Yes	No
EDSU	Yes (32 BP) ^[1]	Yes (8 BP) ^[1]
Power supply voltage	3 V / 5 V	
Regulator	Yes	
Power consumption	n.a.	< 700 mW
Temperature range (T _A)	0 °C to +70°C	- 40 °C to + 105°C
Package	BGA-660	LQFP-64

1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

2. Pin Assignment



3. Pin Description

Pin No.	Pin Name	I/O	I/O Circuit Type ^[1]	Function
2 to 9	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins for A/D converter
10 to 12	P24_0 to P24_2	I/O	A	General-purpose input/output ports
	INT0 to INT2			External interrupt input pins
13	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pins
	MONCLK			Clock monitor output pin
14	P24_4	I/O	C	General-purpose input/output port
	INT4			External interrupt input pin
	SDA2			I ² C bus data input/output pin
15	P24_5	I/O	C	General-purpose input/output port
	INT5			External interrupt input pin
	SCL2			I ² C bus clock input/output pin
19	P24_6	I/O	C	General-purpose input/output port
	INT6			External interrupt input pin
	SDA3			I ² C bus data input/output pin
20	P24_7	I/O	C	General-purpose input/output port
	INT7			External interrupt input pin
	SCL3			I ² C bus clock input/output pin
21	P22_0	I/O	A	General-purpose input/output port
	RX4			RX input pin of CAN4
	INT12			External interrupt input pin
22	P22_1	I/O	A	General-purpose input/output port
	TX4			TX output pin of CAN4
23	P22_2	I/O	A	General-purpose input/output port
	RX5			RX input pin of CAN5
	INT13			External interrupt input pin
24	P22_3	I/O	A	General-purpose input/output port
	TX5			TX output pin of CAN5
25	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin of LIN-USART2
	AIN0			Up/down counter input pin
26	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin of LIN-USART2
	BIN0			Up/down counter input pin
27	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin of LIN-USART2
	CK2			Free-run timer input pin
	ZIN0			Up/down counter input pin
28	P20_4	I/O	A	General-purpose input/output port
	SIN3			Data input pin of LIN-USART3
	AIN1			Up/down counter input pin

Pin No.	Pin Name	I/O	I/O Circuit Type ^[1]	Function
29	P20_5	I/O	A	General-purpose input/output port
	SOT3			Data output pin of LIN-USART3
	BIN1			Up/down counter input pin
30	P20_6	I/O	A	General-purpose input/output port
	SCK3			Clock input/output pin of LIN-USART3
	CK3			Free-run timer input pin
	ZIN1			Up/down counter input pin
31	P15_0	I/O	A	General-purpose input/output port
	OCU0			Output compare output pin
	TOT0			Reload timer output pin
32	P15_1	I/O	A	General-purpose input/output port
	OCU1			Output compare output pin
	TOT1			Reload timer output pin
34	X0	–	J	Clock (oscillation) input
35	X1	–	J	Clock (oscillation) output
36	MD3	I	I	Mode setting pin
37	MD2	I	G	Mode setting pin
38	MD1	I	G	Mode setting pin
39	MD0	I	G	Mode setting pin
40	INITX	I	H	External reset input
41	P15_2	I/O	A	General-purpose input/output port
	OCU2			Output compare output pin
	TOT2			Reload timer output pin
42	P15_3	I/O	A	General-purpose input/output port
	OCU3			Output compare output pin
	TOT3			Reload timer output pin
43 to 47, 50 to 52	P17_7 to P17_0	I/O	A	General-purpose input/output ports
	PPG7 to PPG0			PPG timer output pins
53	P21_6	I/O	A	General-purpose input/output port
	SCK1			Clock input/output pin of LIN-USART1
	CK1			Free-run timer input pin
54	P21_5	I/O	A	General-purpose input/output port
	SOT1			Data output pin of LIN-USART1
55	P21_4	I/O	A	General-purpose input/output port
	SIN1			Data input pin of LIN-USART1
56	P21_2	I/O	A	General-purpose input/output port
	SCK0			Clock input/output pin of LIN-USART0
	CK0			Free-run timer input pin
57	P21_1	I/O	A	General-purpose input/output port
	SOT0			Data output pin of LIN-USART0
58	P21_0	I/O	A	General-purpose input/output port
	SIN0			Data input pin of LIN-USART0

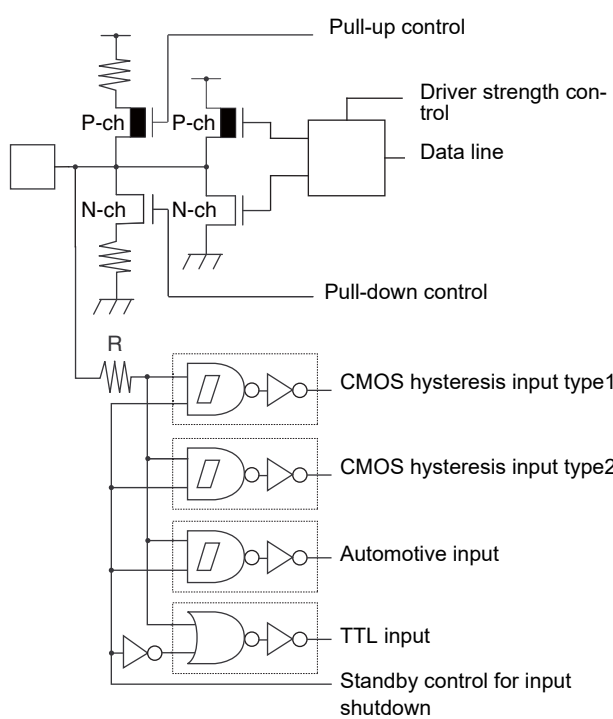
Pin No.	Pin Name	I/O	I/O Circuit Type ^[1]	Function
59	P14_3	I/O	A	General-purpose input/output port
	ICU3			Input capture input pin
	TIN3			External trigger input pin of reload timer
	TTG3			PPG timer input pin
60	P14_2	I/O	A	General-purpose input/output port
	ICU2			Input capture input pin
	TIN2			External trigger input pin of reload timer
	TTG2			PPG timer input pin
61	P14_1	I/O	A	General-purpose input/output port
	ICU1			Input capture input pin
	TIN1			External trigger input pin of reload timer
	TTG1			PPG timer input pin
62	P14_0	I/O	A	General-purpose input/output port
	ICU0			Input capture input pin
	TIN0			External trigger input pin of reload timer
	TTG0			PPG timer input pin

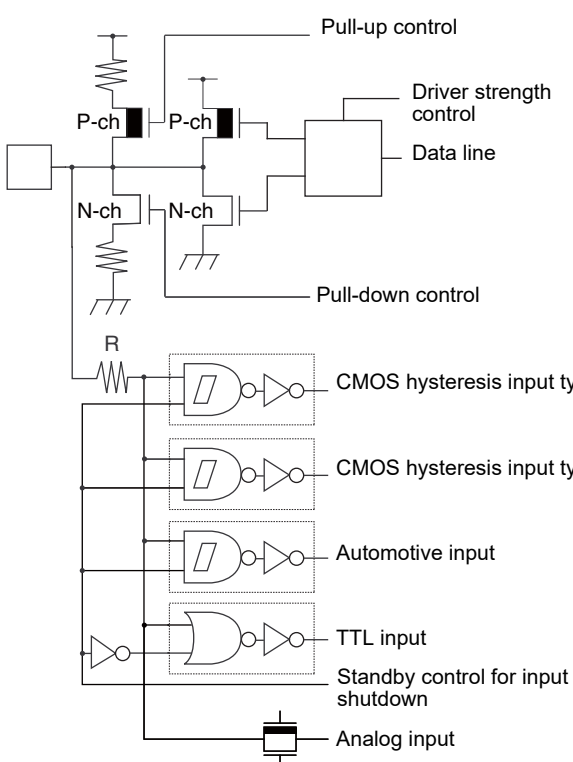
1. For I/O circuit type, refer to “[I/O Circuit Type](#)”.

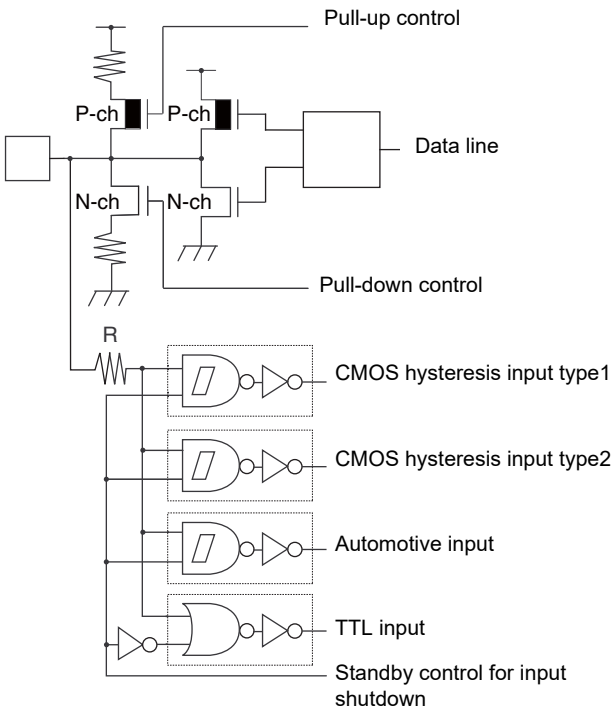
3.1 Power Supply/GND Pins

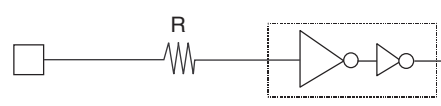
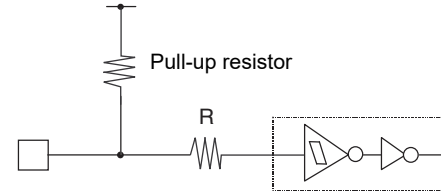
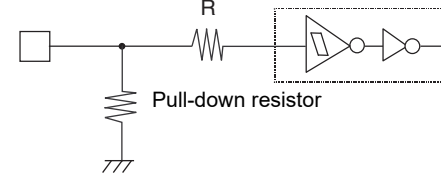
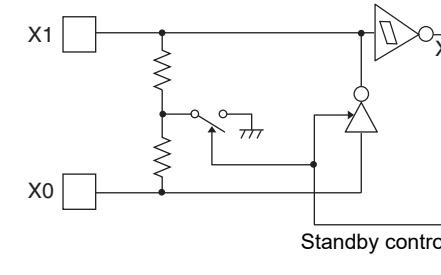
Pin No.	Pin Name	I/O	Function
17, 33, 49	VSS	-	GND pins
16, 48	VCC	-	3.3 V/5 V power supply pins
64	AVSS	-	Analog GND pin for A/D converter
1	AVCC	-	3.3 V/5 V power supply pin for A/D converter
63	AVRH	-	Reference power supply pin for A/D converter
18	C	-	Capacitor connection pin for internal regulator

4. I/O Circuit Type

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> ■ CMOS level output (programmable $I_{OL} = 5\text{mA}$, $I_{OH} = -5\text{mA}$, $I_{OL} = 2\text{mA}$, $I_{OH} = -2\text{mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown function ■ Programmable pull-up resistor: approx. $50\text{ k}\Omega$

Type	Circuit	Remarks
B	 <p>Pull-up control</p> <p>P-ch</p> <p>P-ch</p> <p>Driver strength control</p> <p>Data line</p> <p>N-ch</p> <p>N-ch</p> <p>Pull-down control</p> <p>R</p> <p>CMOS hysteresis input type1</p> <p>CMOS hysteresis input type2</p> <p>Automotive input</p> <p>TTL input</p> <p>Standby control for input shutdown</p> <p>Analog input</p>	<ul style="list-style-type: none"> ■ CMOS level output (programmable $I_{OL} = 5\text{ mA}$, $I_{OH} = -5\text{ mA}$, $I_{OL} = 2\text{ mA}$, $I_{OH} = -2\text{ mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown: approx. 50 kΩ ■ Analog input

Type	Circuit	Remarks
C	 <p>Pull-up control</p> <p>P-ch</p> <p>N-ch</p> <p>Pull-down control</p> <p>Data line</p> <p>R</p> <p>CMOS hysteresis input type1</p> <p>CMOS hysteresis input type2</p> <p>Automotive input</p> <p>TTL input</p> <p>Standby control for input shutdown</p>	<ul style="list-style-type: none"> ■ CMOS level output ($I_{OL} = 3 \text{ mA}$, $I_{OH} = -3 \text{ mA}$) ■ 2 different CMOS hysteresis inputs with input shutdown function ■ Automotive input with input shutdown function ■ TTL input with input shutdown function ■ Programmable pull-up resistor: approx.50 kΩ

Type	Circuit	Remarks
G		<ul style="list-style-type: none"> ■ MASK ROM and evaluation device: CMOS level input ■ Flash device: <ul style="list-style-type: none"> □ CMOS level input □ 12 V resistant (for MD [2:0])
H		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ Pull-up resistor value: approx. 50 kΩ
I		<ul style="list-style-type: none"> ■ CMOS hysteresis input ■ Pull-down resistor value: approx. 50 kΩ
J		Oscillation circuit

5. Precautions for Handling The Devices

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such over voltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

Note:

The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (a) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (b) Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, submarine repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with Cypress sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mounting type. In either case, quality assurance of heat resistance are applied for mounting under the Cypress's recommended conditions only at the soldering stage. For detailed information on mount conditions, contact the sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket. Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions. If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges. You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

(a) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

(b) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between + 5°C to + 30°C.

(c) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

(d) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

■ Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

(a) Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.

(b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.

(c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.

(d) Ground all fixtures and instruments, or protect with anti-static measures.

(e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, Flame

Note: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with Cypress sales representatives.

6. Handling Devices

■ Power supply pins

Because there are multiple VCC and VSS pins, respective pins at the same potential are interconnected to prevent malfunctions such as latch-up. However, you must connect the pins externally to the power supply and ground lines to reduce the electro-magnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Furthermore, the current supply source should be connected to the VCC and VSS pins of the device at a low impedance.

It is recommended to connect a ceramic bypass capacitor of approximately 0.1 μ F as a bypass capacitor between the V_{CC} and V_{SS} near this device.

■ Crystal oscillator circuit

Noise in proximity to the X0 and X1 pins can cause the device to malfunction. Printed circuit boards should be designed so that the X0 and X1 pins, crystal oscillator (or ceramic oscillator), and bypass capacitors connected to ground are located near the device and ground.

It is recommended that the printed circuit board artwork be designed such that the X0 and X1 pins are surrounded by ground plane for the stable operation.

Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

■ Mode pins (MD0 to MD3)

Connect them directly to VCC or VSS. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and VCC or VSS on the printed circuit board as much as possible and connect them at a low impedance. When used pulling down, design your circuit not to generate noises with a resistance 1 k Ω or less. Test your circuit and confirm that there is no problem.

■ Operation at power-on

At power-on, it is necessary to make the terminal INITX “L” level.

Maintain the “L” level input to the INITX pin for the duration of the stabilization wait time immediately after the power on to ensure the stabilization wait time as required by the oscillator circuit.

■ Note on oscillator input at power-on

At power-on, ensure that the clock is input until the oscillator stabilization wait time has elapsed.

■ Built-in regulator

As this series includes built-in step-down regulators, always connect a bypass capacitor of 4.7 μ F or more to the C pin for use by the regulator.

■ Notes on power on/off

Connect/disconnect the power supply pins when power on/off, or turn on/off in the following order.

Power on : VCC \rightarrow AVCC, AVRH

Power off : AVCC, AVRH \rightarrow VCC

■ Precautions for the STOP mode

Set 1 to the bit 0 (OSCD1) of STCR register. When shifting to the STOP mode, a regulator switches to the stand-by regulator (for low-consumption current). Due to the limited drive current, stop the (programming/erasing) access to the A/D converter and Flash before shifting to the STOP mode.

■ Serial communication

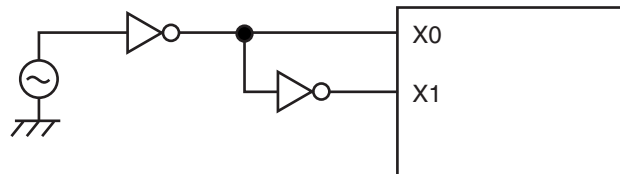
There is a possibility to receive wrong data due to the noise or other causes on the serial communication. Therefore, design a board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example, apply a checksum to detect an error. If an error is detected, retransmit the data.

■ Notes on using external clock

When using the external clock, as a general rule you should simultaneously supply X0 and X1 pins. And also, the clock signal to X0 should be supplied a clock signal with the reverse phase to X1 pins. However, in this case the stop mode (oscillation stop mode) must not be used.

Example of using external clock (normal)



Note: Stop mode (oscillation stop mode) cannot be used.

■ Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

7. Notes on Debugger

7.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

7.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

7.3 Operand Break

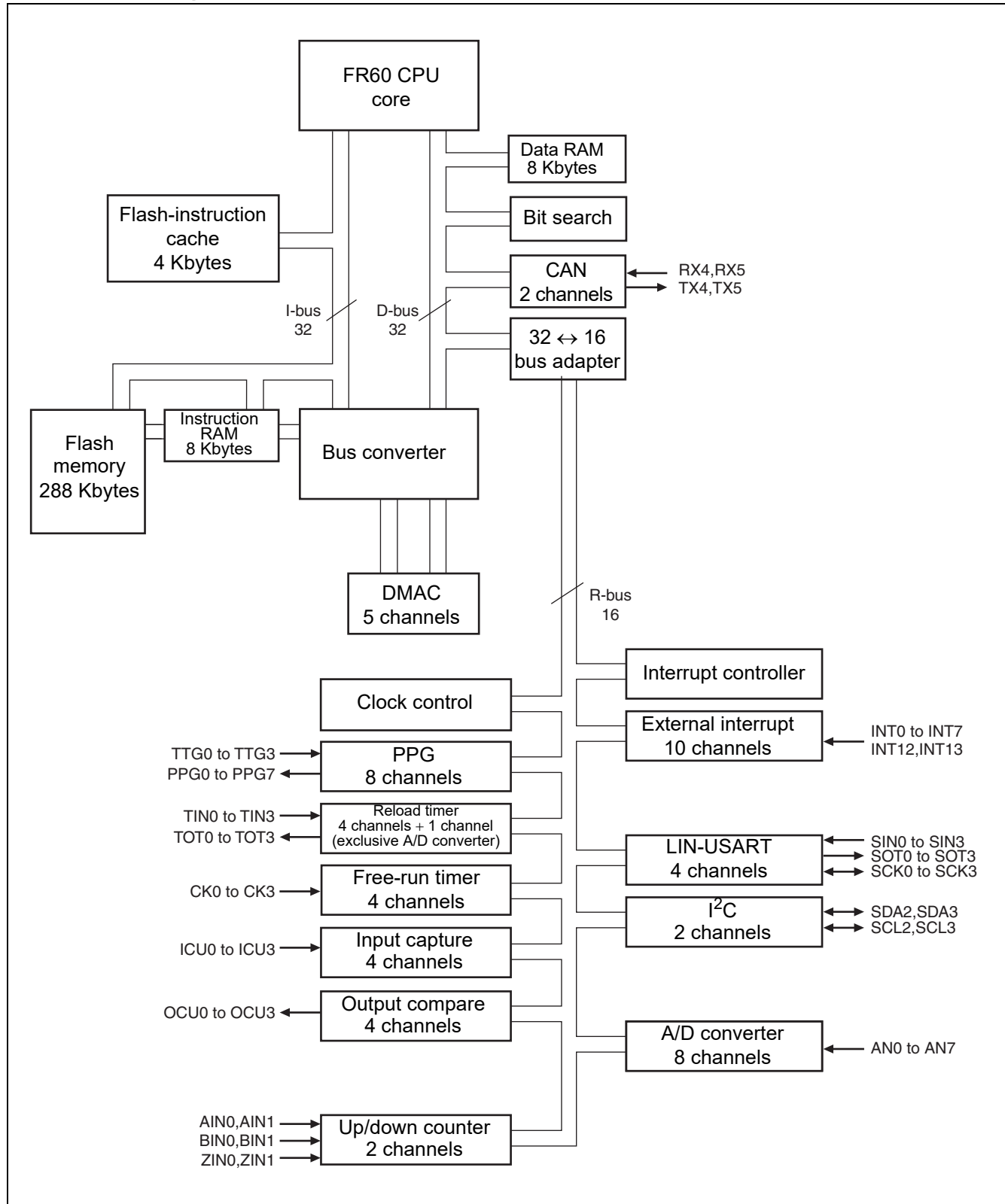
It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

7.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the following exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated. As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

- The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:
 - (a) a user interrupt or NMI is accepted; (b) single-step execution is performed; or (c) execution breaks due to a data event or from the emulator menu.
 - D0 and D1 flags are updated in advance.
 - An EIT handling routine (user interrupt/NMI or emulator) is executed.
 - Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).
- The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.
 - The PS register is updated in advance.
 - An EIT handling routine (user interrupt/NMI or emulator) is executed.
 - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1).

8. Block Diagram



9. CPU and Control Unit

Internal Architecture

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

9.1 Features

- Adoption of RISC architecture
Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
32-bit × 32-bit multiplication: 5 cycles
16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
Quick response speed (6 cycles)
Multiple-interrupt support
Level mask function (16 levels)
- Enhanced instructions for I/O operation
Memory-to-memory transfer instruction
Bit processing instruction
- Basic instruction word length: 16 bits
- Low-power consumption
SLEEP mode/STOP mode

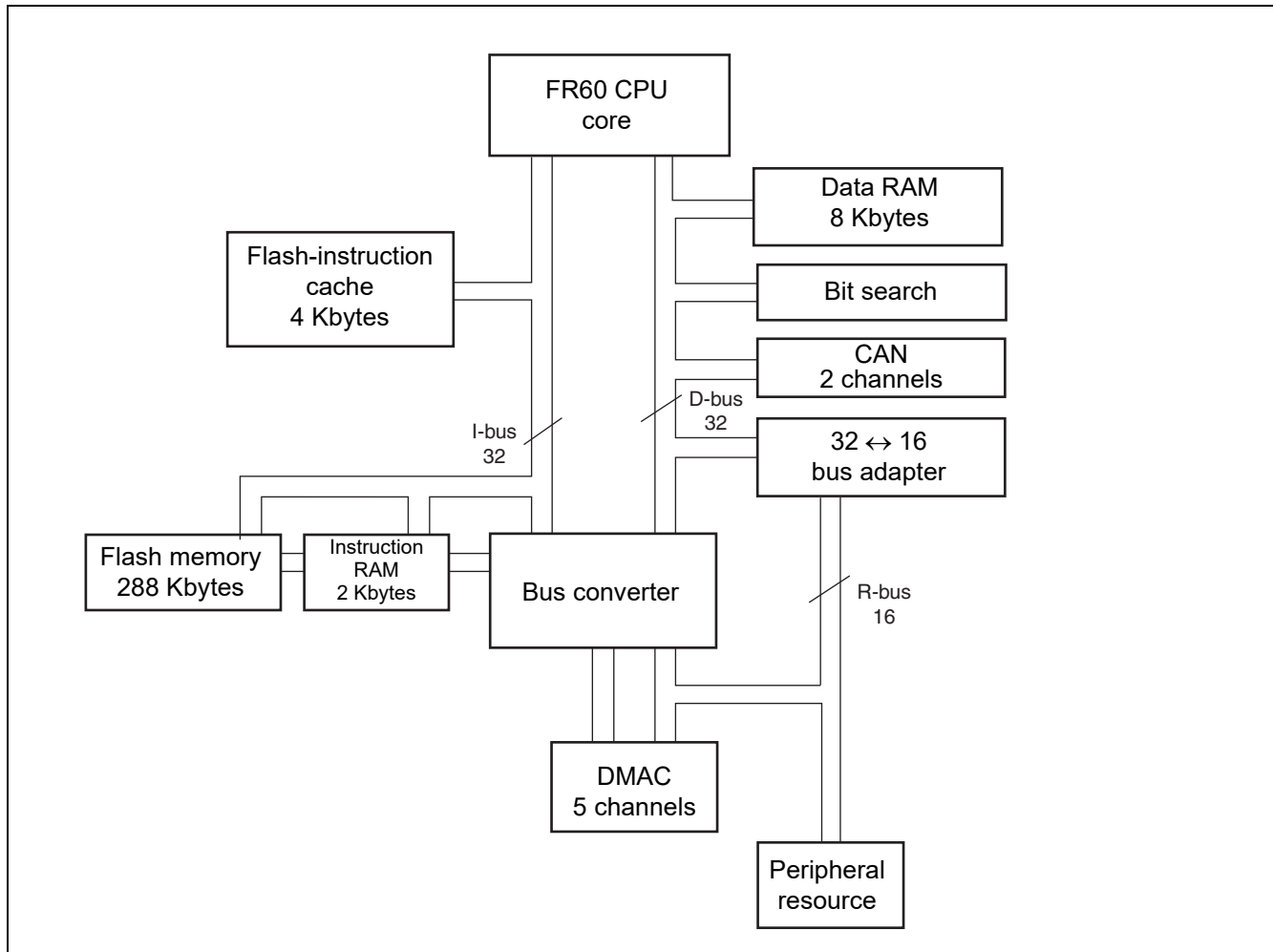
9.2 Internal Architecture

The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.

A 32-bit ↔ 16-bit bus adapter is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.

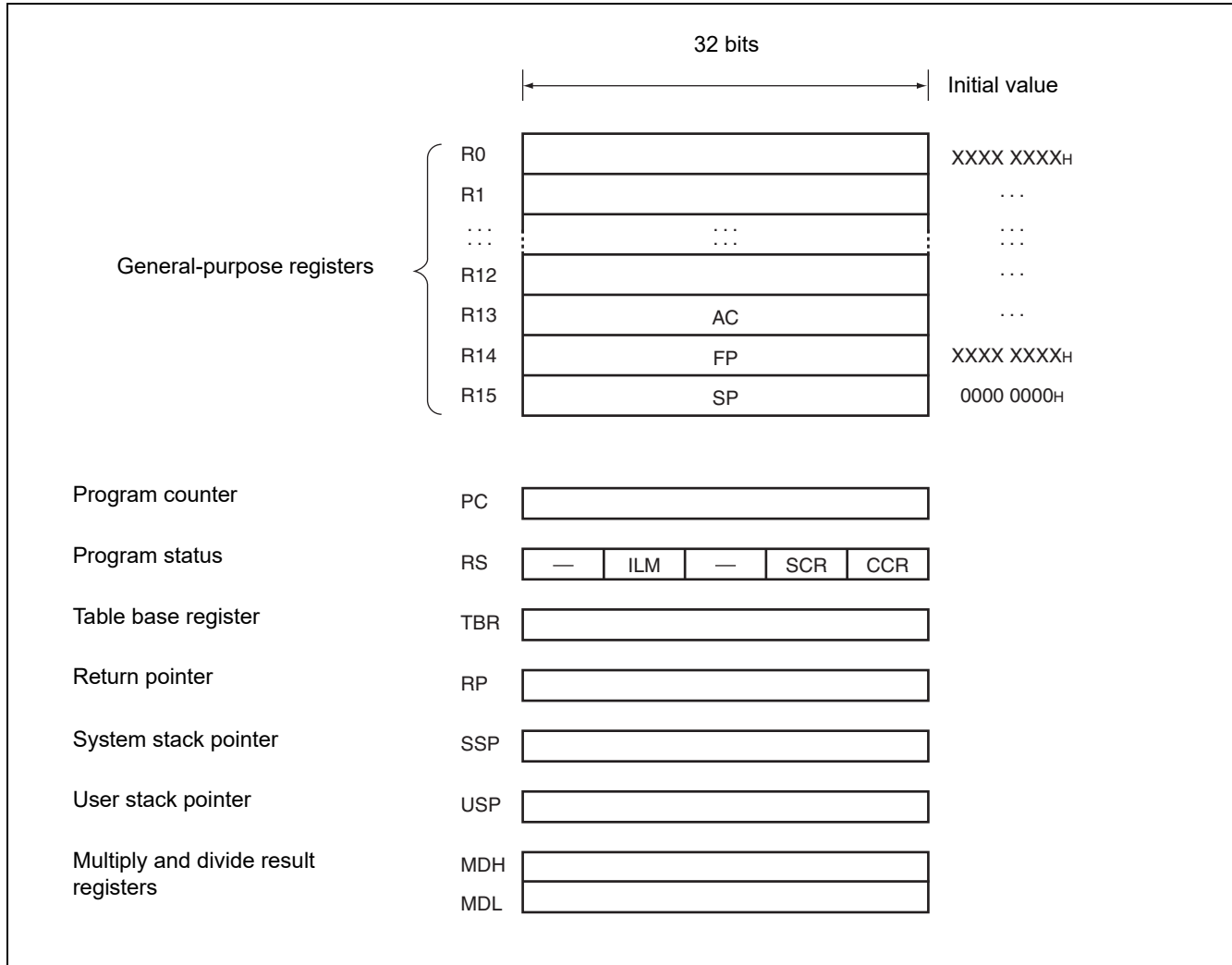
A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

The following figure shows the internal architecture structure.



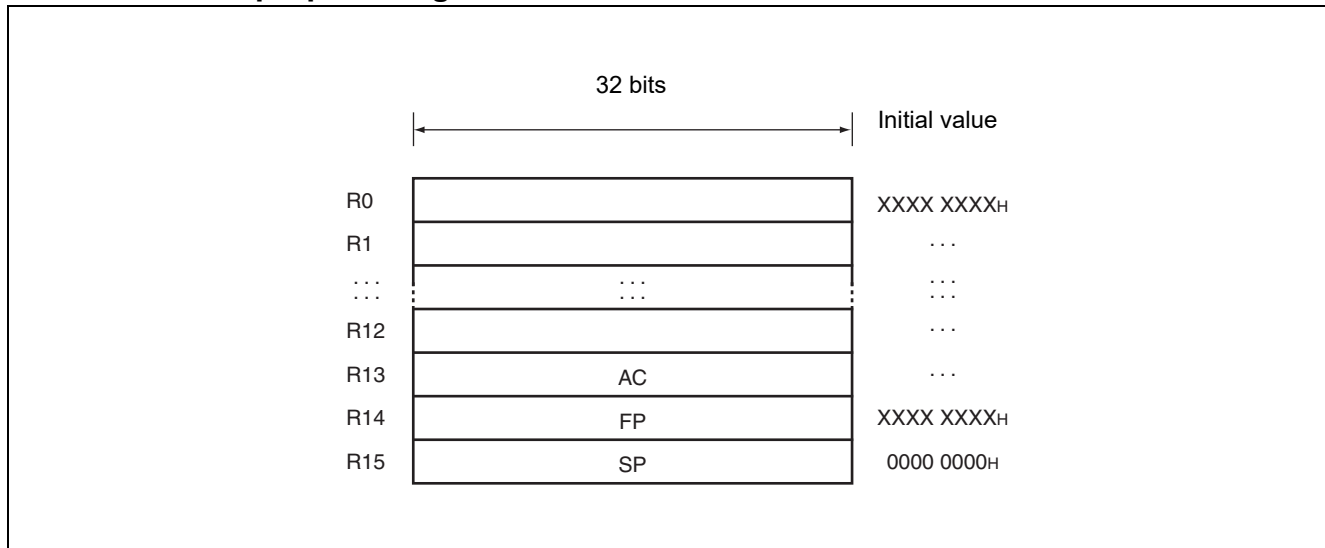
9.3 Programming Model

9.3.1 Basic Programming Model



9.4 Registers

9.4.1 General-purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Enhanced commands are provided for some of the 16 registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

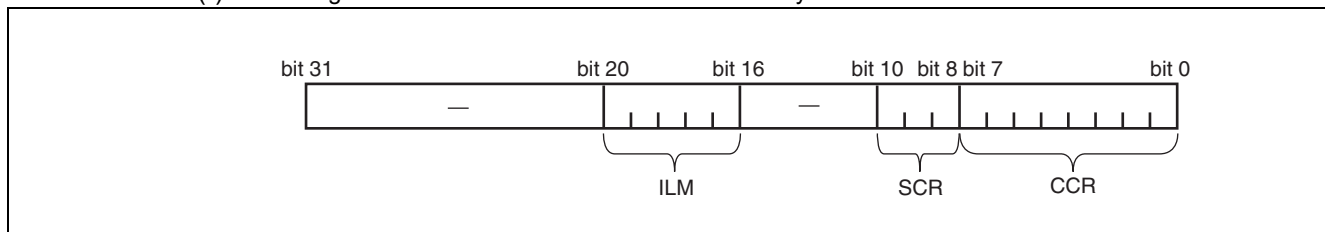
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

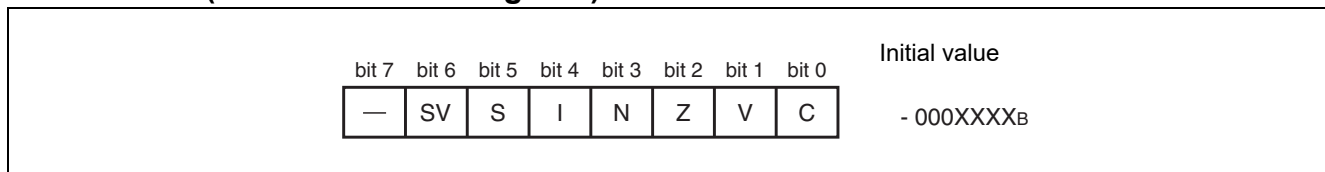
9.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The values are always read "0". Write access to these bits is invalid.



9.4.3 CCR (Condition Code Register)



SV: Supervisor

S: Stack flag

I: Interrupt enable flag

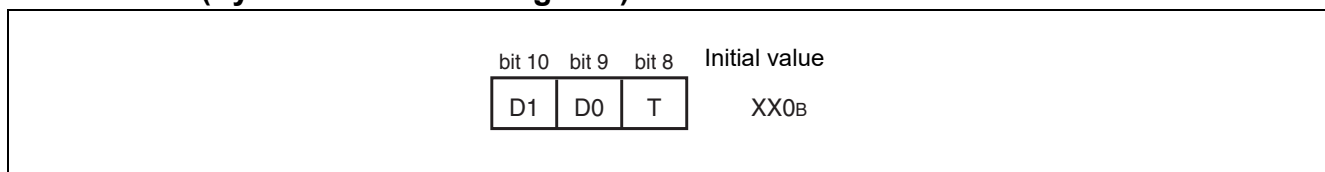
N: Negative enable flag

Z: Zero flag

V: Overflow flag

C: Carry flag

9.4.4 SCR (System Condition Register)



Flag for step multiplication (D1, D0)

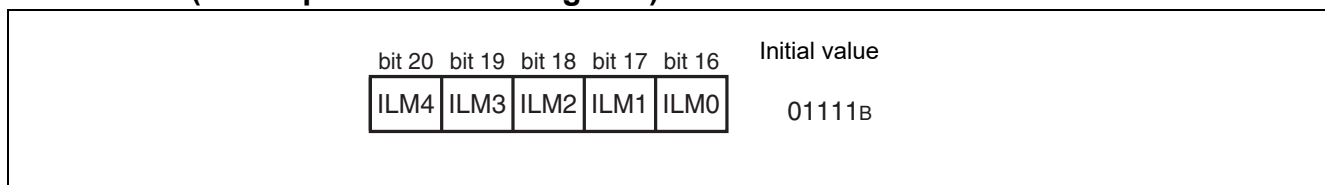
This flag stores interim data during execution of step multiplication.

Step trace trap flag (T)

This flag indicates whether the step trace trap is enabled or disabled.

The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

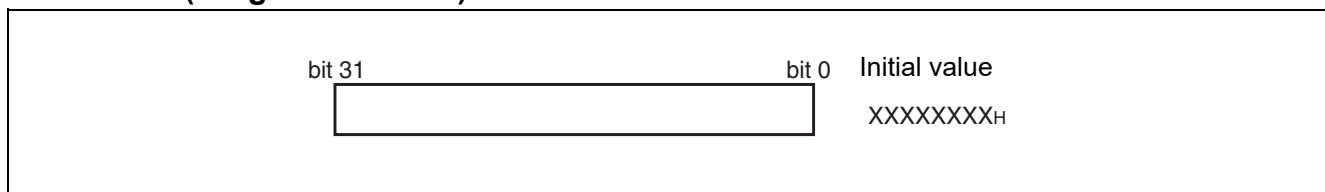
9.4.5 ILM (Interrupt Level Mask Register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value "01111_B" at reset.

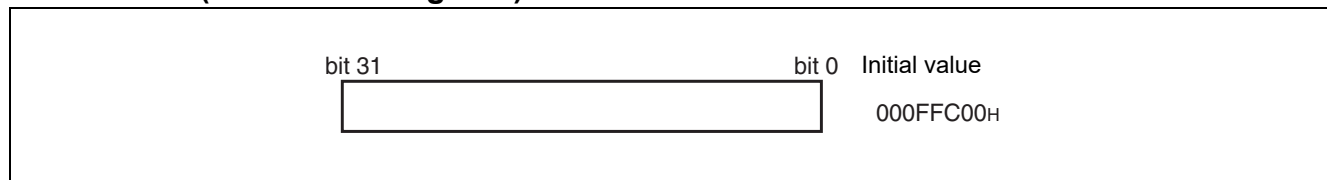
9.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

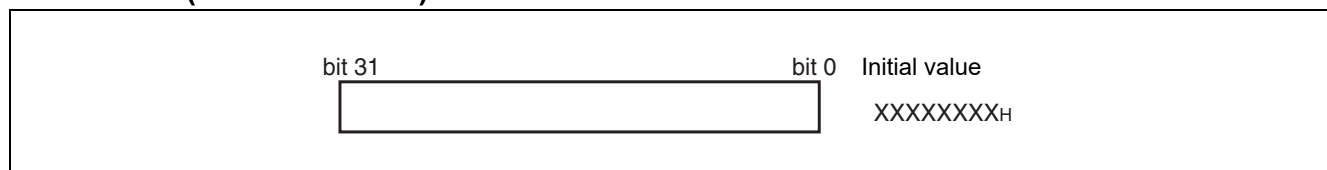
9.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00_H.

9.4.8 RP (Return Pointer)



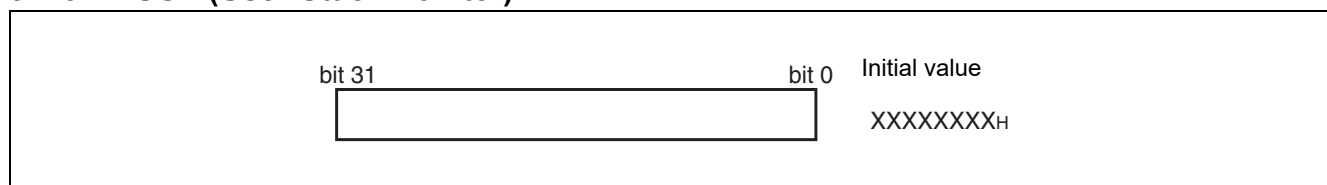
The return pointer stores the address to return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

9.4.9 USP (User Stack Pointer)



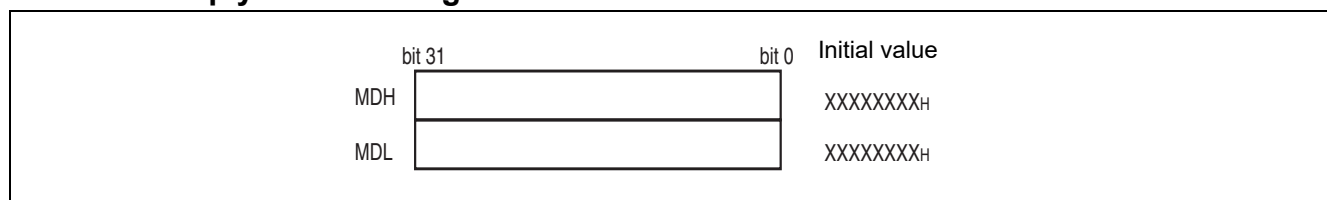
When the S flag is "1", the user stack pointer functions as the R15 register.

- The USP register can also be explicitly specified.

The initial value at reset is undefined.

- This register cannot be used with RETI instructions.

9.4.10 Multiply & Divide Registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

10. Mode Setting

In the FR family, the mode pins (MD2, MD1, MD0) and the mode register (MODR) are used to set the operating mode.

10.1 Mode Pins

The three pins MD2, MD1, MD0 are used to specify the mode vector fetch.

Settings other than shown in the table are prohibited.

Mode Pins ^[1]			Mode Name	Reset Vector Access Area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	Not allowed

1. Always use MD3 with "0".

10.2 Mode Register (MODR)

The data written to the mode register using mode vector fetch is called mode data.

After the mode register (MODR) is set, the device operates according to the operation mode set in this register.

The mode register is set by all reset sources. User programs cannot write data to the mode register.

Rewriting is allowed in the emulator mode. In this case, use an 8-bit length data transfer instruction.

Data cannot be written by the transfer instruction of the 16/32-bit length.

Be sure to set these bits to "00000111_B".

Operation is not guaranteed when any value other than "00000111_B" is set.

Note: The mode data needs to be allocated in 000FFFF8_H as byte data. The mode data (00000111_B) must be allocated in bit 31 to bit 24, as the FR family uses the big endian architecture.

11. Recommended Setting

11.1 Setting of PLL and Clock Gear

Table 1. Recommended Setting of PLL Division and Clock Gear

Clock Input [MHz]	PLL Multiplied Setting		Clock Gear Setting		PLL (vco) Output (X) [MHz]	Base Clock [MHz]
	DIVM	DIVN	DIVG	MULG		
4	2	20	16	20	160	80
4	2	19	16	20	152	76
4	2	18	16	20	144	72
4	2	17	16	16	136	68
4	2	16	16	16	128	64
4	2	15	16	16	120	60
4	2	14	16	16	112	56
4	2	13	16	12	104	52
4	2	12	16	12	96	48
4	2	11	16	12	88	44
4	4	10	16	24	160	40
4	4	9	16	24	144	36
4	4	8	16	24	128	32
4	4	7	16	24	112	28
4	6	6	16	24	144	24
4	8	5	16	28	160	20
4	10	4	16	32	160	16
4	12	3	16	32	144	12

11.2 Setting of Flash Memory Controller

11.2.1 Setting of Flash Access Timing

For executing programs with a Flash memory, follow the settings below according to the frequency of CPU clock (CLKB). This setting is the most suitable for a high-speed access to the Flash memory.

Table 2. Flash Memory Read Operating

CPU Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
To 24 MHz	0	0	0	0	1
To 48 MHz	0	0	1	0	2
To 80 MHz	1	1	3	0	4

Table 3. Flash Memory Write Operating

CPU Clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC
To 32 MHz	1	0	1	0	4
To 48 MHz	1	0	3	0	5
To 64 MHz	1	1	3	0	6
To 80 MHz	1	1	3	0	7

11.3 Setting of Clock Modulator

The setting values in the table are defined within the ranges of base clock frequency; 32 MHz to 80 MHz. The Flash memory access needs to be configured according to the Fmax. PLL and clock gear need to be configured according to the base clock.

Table 4. Setting of Clock Modulator

Modulation (k)	Internal Parameter (N)	CMPR [hex]	Base Clock [MHz]	Fmin [MHz]	Fmax [MHz]
1	3	026F	80	72.6	89.1
1	3	026F	76	69.1	84.5
1	5	02AE	76	65.3	90.8
2	3	046E	76	65.3	90.8
1	3	026F	72	65.5	79.9
1	5	02AE	72	62	85.8
1	7	02ED	72	58.8	92.7
2	3	046E	72	62	85.8
1	3	026F	68	62	75.3
1	5	02AE	68	58.7	80.9
1	7	02ED	68	55.7	87.3
1	9	032C	68	53	95
2	3	046E	68	58.7	80.9
2	5	04AC	68	53	95
3	3	066D	68	55.7	87.3
4	3	086C	68	53	95
1	3	026F	64	58.5	70.7
1	5	02AE	64	55.3	75.9
1	7	02ED	64	52.5	82
1	9	032C	64	49.9	89.1
2	3	046E	64	55.3	75.9
2	5	04AC	64	49.9	89.1
3	3	066D	64	52.5	82
4	3	086C	64	49.9	89.1
1	3	026F	60	54.9	66.1
1	5	02AE	60	51.9	71
1	7	02ED	60	49.3	76.7
1	9	032C	60	46.9	83.3
2	3	046E	60	51.9	71
2	5	04AC	60	46.9	83.3
3	3	066D	60	49.3	76.7
4	3	086C	60	46.9	83.3
5	3	0A6B	60	44.7	91.3
1	3	026F	56	51.4	61.6
1	5	02AE	56	48.6	66.1
1	7	02ED	56	46.1	71.4
1	9	032C	56	43.8	77.6

Modulation (k)	Internal Parameter (N)	CMPR [hex]	Base Clock [MHz]	Fmin [MHz]	Fmax [MHz]
1	11	036B	56	41.8	84.9
1	13	03AA	56	39.9	93.8
2	3	046E	56	48.6	66.1
2	5	04AC	56	43.8	77.6
2	7	04EA	56	39.9	93.8
3	3	066D	56	46.1	71.4
4	3	086C	56	43.8	77.6
5	3	0A6B	56	41.8	84.9
1	3	026F	52	47.8	57
1	5	02AE	52	45.2	61.2
1	7	02ED	52	42.9	66.1
1	9	032C	52	40.8	71.8
1	11	036B	52	38.8	78.6
1	13	03AA	52	37.1	86.8
2	3	046E	52	45.2	61.2
2	5	04AC	52	40.8	71.8
2	7	04EA	52	37.1	86.8
3	3	066D	52	42.9	66.1
3	5	06AA	52	37.1	86.8
4	3	086C	52	40.8	71.8
5	3	0A6B	52	38.8	78.6
6	3	0C6A	52	37.1	86.8
1	3	026F	48	44.2	52.5
1	5	02AE	48	41.8	56.4
1	7	02ED	48	39.6	60.9
1	9	032C	48	37.7	66.1
1	11	036B	48	35.9	72.3
1	13	03AA	48	34.3	79.9
1	15	03E9	48	32.8	89.1
2	3	046E	48	41.8	56.4
2	5	04AC	48	37.7	66.1
2	7	04EA	48	34.3	79.9
3	3	066D	48	39.6	60.9
3	5	06AA	48	34.3	79.9
4	3	086C	48	37.7	66.1
5	3	0A6B	48	35.9	72.3
6	3	0C6A	48	34.3	79.9
7	3	0E69	48	32.8	89.1
1	3	026F	44	40.6	48.1
1	5	02AE	44	38.4	51.6
1	7	02ED	44	36.4	55.7

Modulation (k)	Internal Parameter (N)	CMPR [hex]	Base Clock [MHz]	Fmin [MHz]	Fmax [MHz]
1	9	032C	44	34.6	60.4
1	11	036B	44	33	66.1
1	13	03AA	44	31.5	73
1	15	03E9	44	30.1	81.4
2	3	046E	44	38.4	51.6
2	5	04AC	44	34.6	60.4
2	7	04EA	44	31.5	73
3	3	066D	44	36.4	55.7
3	5	06AA	44	31.5	73
4	3	086C	44	34.6	60.4
4	5	08A8	44	28.9	92.1
5	3	0A6B	44	33	66.1
6	3	0C6A	44	31.5	73
7	3	0E69	44	30.1	81.4
1	3	026F	40	37	43.6
1	5	02AE	40	34.9	46.8
1	7	02ED	40	33.1	50.5
1	9	032C	40	31.5	54.8
1	11	036B	40	30	59.9
1	13	03AA	40	28.7	66.1
1	15	03E9	40	27.4	73.7
2	3	046E	40	34.9	46.8
2	5	04AC	40	31.5	54.8
2	7	04EA	40	28.7	66.1
2	9	0528	40	26.3	83.3
3	3	066D	40	33.1	50.5
3	5	06AA	40	28.7	66.1
3	7	06E7	40	25.3	95.8
4	3	086C	40	31.5	54.8
4	5	08A8	40	26.3	83.3
5	3	0A6B	40	30	59.9
6	3	0C6A	40	28.7	66.1
7	3	0E69	40	27.4	73.7
8	3	1068	40	26.3	83.3
1	3	026F	36	33.3	39.2
1	5	02AE	36	31.5	42
1	7	02ED	36	29.9	45.3
1	9	032C	36	28.4	49.2
1	11	036B	36	27.1	53.8
1	13	03AA	36	25.8	59.3
1	15	03E9	36	24.7	66.1

Modulation (k)	Internal Parameter (N)	CMPR [hex]	Base Clock [MHz]	Fmin [MHz]	Fmax [MHz]
2	3	046E	36	31.5	42
2	5	04AC	36	28.4	49.2
2	7	04EA	36	25.8	59.3
2	9	0528	36	23.7	74.7
3	3	066D	36	29.9	45.3
3	5	06AA	36	25.8	59.3
3	7	06E7	36	22.8	85.8
4	3	086C	36	28.4	49.2
4	5	08A8	36	23.7	74.7
5	3	0A6B	36	27.1	53.8
6	3	0C6A	36	25.8	59.3
7	3	0E69	36	24.7	66.1
8	3	1068	36	23.7	74.7
9	3	1267	36	22.8	85.8
1	3	026F	32	29.7	34.7
1	5	02AE	32	28	37.3
1	7	02ED	32	26.6	40.2
1	9	032C	32	25.3	43.6
1	11	036B	32	24.1	47.7
1	13	03AA	32	23	52.5
1	15	03E9	32	22	58.6
2	3	046E	32	28	37.3
2	5	04AC	32	25.3	43.6
2	7	04EA	32	23	52.5
2	9	0528	32	21.1	66.1
2	11	0566	32	19.5	89.1
3	3	066D	32	26.6	40.2
3	5	06AA	32	23	52.5
3	7	06E7	32	20.3	75.9
4	3	086C	32	25.3	43.6
4	5	08A8	32	21.1	66.1
5	3	0A6B	32	24.1	47.7
5	5	0AA6	32	19.5	89.1
6	3	0C6A	32	23	52.5
7	3	0E69	32	22	58.6
8	3	1068	32	21.1	66.1
9	3	1267	32	20.3	75.9
10	3	1466	32	19.5	89.1

12. Memory Space

12.1 Memory space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

■ Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

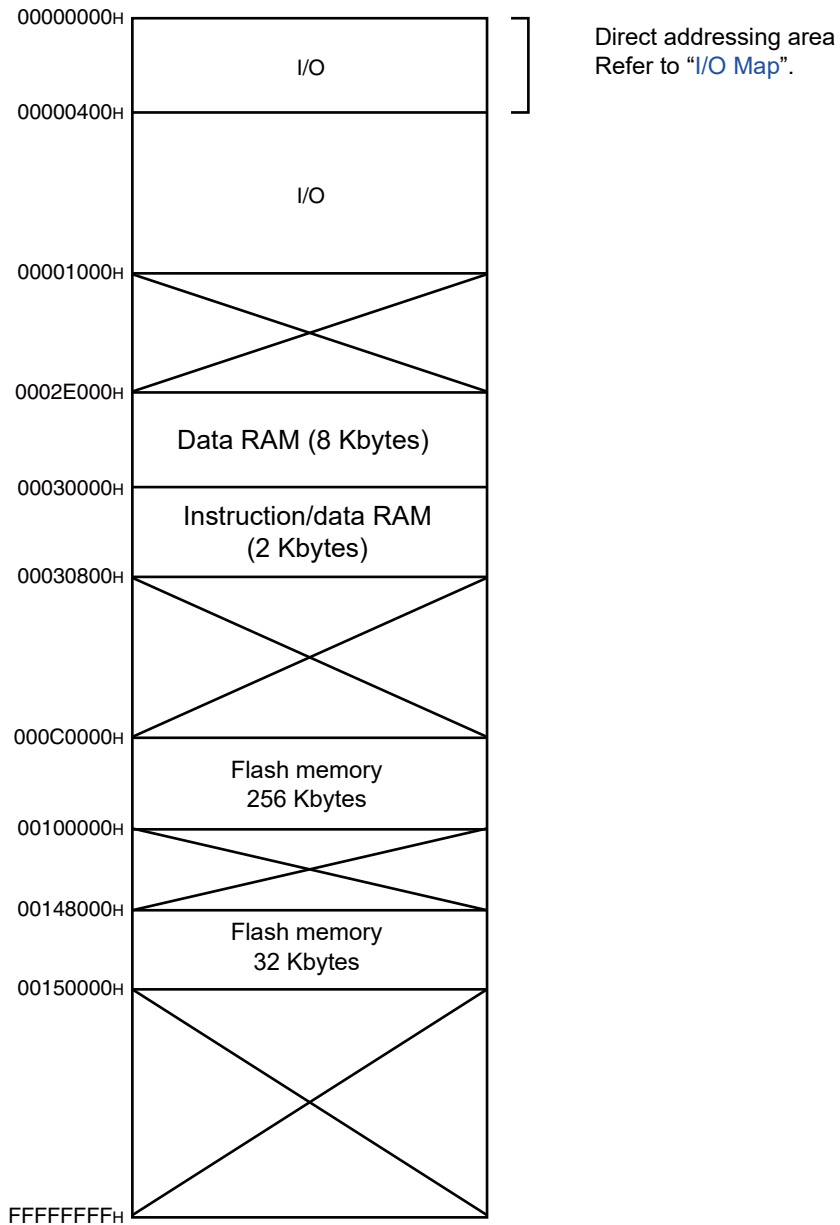
The size of directly addressable area depends on the length of the data to be accessed as shown below.

Byte data access: 000_H to $0FF_H$

Half word access: 000_H to $1FF_H$

Word data access: 000_H to $3FF_H$

12.2 Memory Map



12.3 Flash Memory Sector Configuration

CY91F463NC	
addr	
0014:FFFF _H	SA7(8 Kbytes)
0014:E000 _H	
0014:DFFF _H	SA6(8 Kbytes)
0014:C000 _H	
0014:BFFF _H	SA5(8 Kbytes)
0014:A000 _H	
0014:9FFF _H	SA4(8 Kbytes)
0014:8000 _H	
0014:7FFF _H	SA3(8 Kbytes)
0014:6000 _H	
0014:5FFF _H	SA2(8 Kbytes)
0014:4000 _H	
0014:3FFF _H	SA1(8 Kbytes)
0014:2000 _H	
0014:1FFF _H	SA0(8 Kbytes)
0014:0000 _H	
0013:FFFF _H	SA23(64 Kbytes)
0013:0000 _H	
0012:FFFF _H	SA22(64 Kbytes)
0012:0000 _H	
0011:FFFF _H	SA21(64 Kbytes)
0011:0000 _H	
0010:FFFF _H	SA20(64 Kbytes)
0010:0000 _H	
000F:FFFF _H	SA19(64 Kbytes)
000F:0000 _H	
000E:FFFF _H	SA18(64 Kbytes)
000E:0000 _H	
000D:FFFF _H	SA17(64 Kbytes)
000D:0000 _H	
000C:FFFF _H	SA16(64 Kbytes)
000C:0000 _H	
000B:FFFF _H	SA15(64 Kbytes)
000B:0000 _H	
000A:FFFF _H	SA14(64 Kbytes)
000A:0000 _H	
0009:FFFF _H	SA13(64 Kbytes)
0009:0000 _H	
0008:FFFF _H	SA12(64 Kbytes)
0008:0000 _H	
0007:FFFF _H	SA11(64 Kbytes)
0007:0000 _H	
0006:FFFF _H	SA10(64 Kbytes)
0006:0000 _H	
0005:FFFF _H	SA9(64 Kbytes)
0005:0000 _H	
0004:FFFF _H	SA8(64 Kbytes)
0004:0000 _H	
	addr+0 addr+1 addr+2 addr+3
	dat[31:16] dat[15:0]
	dat[31:0]

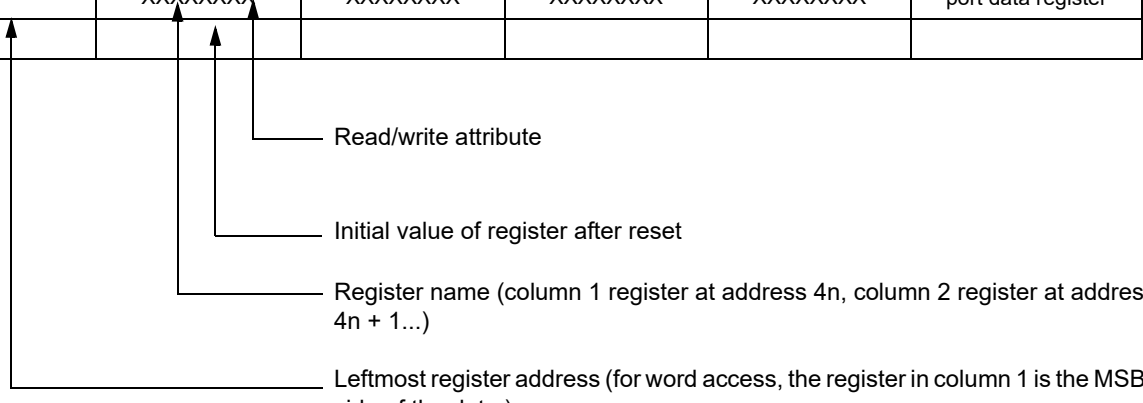
16-bit write mode
32-bit read mode

The shaded area is unusable.

Note: CY91F463NC has a different sector map for the flash memory to that of CY91F463NA. The sector map showed above is suited for CY91F463NC, not for CY91F463NA.

13. I/O Map

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000 _H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note: Initial values of register bits are represented as follows:

“ 1 ”: Initial value “ 1 ”

“ 0 ”: Initial value “ 0 ”

“ X ”: Initial value “ undefined ”

“ - ”: No physical register at this location

Access is prohibited to areas where the data access attributes are undefined.

Address	Register				Block
	+0	+1	+2	+3	
000000 _H to 000008 _H	Reserved				R-bus Port Data Register
00000C _H	Reserved		PDR14 [R/W] ---- XXXX	PDR15 [R/W] ---- XXXX	
000010 _H	Reserved	PDR17 [R/W] XXXXXXXX	Reserved		
000014 _H	PDR20 [R/W] -XXX-XXX	PDR21 [R/W] -XXX-XXX	PDR22 [R/W] ---- XXXX	Reserved	
000018 _H	PDR24 [R/W] XXXXXXXX	Reserved			
00001C _H	Reserved	PDR29 [R/W] XXXXXXXX	Reserved		
000020 _H	Reserved				
000024 _H to 00002C _H	Reserved				Reserved
000030 _H	EIRR0 [R/W] 00000000	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt 0 to 7
000034 _H	EIRR1 [R/W] 00000000	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt 12, 13
000038 _H	DICR [R/W] ----- 0	HRCL [R/W] 0 -- 11111	Reserved		DLYI/I-unit
00003C _H	Reserved				Reserved
000040 _H	SCR00 [R/W, W] 00000000	SMR00 [R/W, W] 00000000	SSR00 [R/W, R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART0
000044 _H	ESCR00 [R/W] 00000X00	ECCR00 [R/W, R, W] 000000XX	Reserved		
000048 _H	SCR01 [R/W, W] 00000000	SMR01 [R/W, W] 00000000	SSR01 [R/W, R] 00001000	RDR01/TDR01 [R/W] 00000000	LIN-USART1
00004C _H	ESCR01 [R/W] 00000X00	ECCR01 [R/W, R, W] 000000XX	Reserved		
000050 _H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART2
000054 _H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] 000000XX	Reserved		
000058 _H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART3
00005C _H	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] 000000XX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
000060 _H to 00007C _H	Reserved				Reserved
000080 _H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	BGR101 [R/W] 00000000	BGR001 [R/W] 00000000	Baud rate Generator LIN-USART0 to 3
000084 _H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088 _H , 00008C _H	Reserved				
000090 _H to 0000FC _H	Reserved				Reserved
000100 _H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104 _H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108 _H	Reserved				Reserved
000110 _H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXXXX XXXXXXXXXX		PPG 0
000114 _H	PDUT00 [W] XXXXXXXXXX XXXXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118 _H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXXXX XXXXXXXXXX		PPG 1
00011C _H	PDUT01 [W] XXXXXXXXXX XXXXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120 _H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXXXX XXXXXXXXXX		PPG 2
000124 _H	PDUT02 [W] XXXXXXXXXX XXXXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128 _H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXXXX XXXXXXXXXX		PPG 3
00012C _H	PDUT03 [W] XXXXXXXXXX XXXXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130 _H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXXXX XXXXXXXXXX		PPG 4
000134 _H	PDUT04 [W] XXXXXXXXXX XXXXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138 _H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXXXX XXXXXXXXXX		PPG 5
00013C _H	PDUT05 [W] XXXXXXXXXX XXXXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140 _H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXXXX XXXXXXXXXX		PPG 6
000144 _H	PDUT06 [W] XXXXXXXXXX XXXXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148 _H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXXXX XXXXXXXXXX		PPG 7
00014C _H	PDUT07 [W] XXXXXXXXXX XXXXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000150 _H to 00017C _H	Reserved				Reserved
000180 _H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184 _H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188 _H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018C _H	OCS01 [R/W] --- 0 -- 00 0000 -- 00		OCS23 [R/W] --- 0 -- 00 0000 -- 00		Output Compare 0 to 3
000190 _H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194 _H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198 _H , 00019C _H	Reserved				Reserved
0001A0 _H	Reserved			ADERL [R/W] 00000000	A/D Converter
0001A4 _H	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8 _H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] --- 00000	ADECH [R/W] --- 00000	
0001AC _H	Reserved				Reserved
0001B0 _H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG0, PPG1)
0001B4 _H	Reserved		TMCSRH0 [R/W] --- 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8 _H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG2, PPG3)
0001BC _H	Reserved		TMCSRH1 [R/W] --- 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0 _H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG4, PPG5)
0001C4 _H	Reserved		TMCSRH2 [R/W] --- 00000	TMCSRL2 [R/W] 0 - 000000	
0001C8 _H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG6, PPG7)
0001CC _H	Reserved		TMCSRH3 [R/W] --- 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0 _H to 0001E7 _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
0001E8 _H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (A/D converter)
0001EC _H	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0 _H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free-run Timer 0 (ICU0, ICU1)
0001F4 _H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free-run Timer 1 (ICU2, ICU3)
0001F8 _H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free-run Timer 2 (OCU0, OCU1)
0001FC _H	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free-run Timer 3 (OCU2, OCU3)
000200 _H	DMACA0 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204 _H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208 _H	DMACA1 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020C _H	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210 _H	DMACA2 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214 _H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218 _H	DMACA3 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021C _H	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220 _H	DMACA4 [R/W] * 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224 _H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228 _H to 00023C _H	Reserved				
000240 _H	DMACR [R/W] 0- - - 0000	Reserved			
000244 _H to 0002FC _H	Reserved				Reserved
000300 _H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0, 1
000304 _H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308 _H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	

Address	Register				Block
	+0	+1	+2	+3	
00030C _H to 000364 _H	Reserved				Reserved
000368 _H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] ----- 00	ITBAL2 [R/W] 00000000	I ² C 2
00036C _H	ITMKH2 [R/W] 00 ---- 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370 _H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	Reserved	
000374 _H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] ----- 00	ITBAL3 [R/W] 00000000	I ² C 3
000378 _H	ITMKH3 [R/W] 00 ---- 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 0000000	
00037C _H	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] - 0011111	Reserved	
000380 _H to 00038C _H	Reserved				Reserved
000390 _H	ROMS [R] 11111111 01001111		Reserved		ROM Select Register
000394 _H to 0003EC _H	Reserved				Reserved
0003F0 _H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4 _H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8 _H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FC _H	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400 _H to 00043C _H	Reserved				Reserved
000440 _H	ICR00 [R/W] --- 11111	ICR01 [R/W] --- 11111	ICR02 [R/W] --- 11111	ICR03 [R/W] --- 11111	Interrupt Control Unit
000444 _H	ICR04[R/W] --- 11111	ICR05 [R/W] --- 11111	ICR06 [R/W] --- 11111	ICR07 [R/W] --- 11111	
000448 _H	ICR08 [R/W] --- 11111	ICR09 [R/W] --- 11111	ICR10[R/W] --- 11111	ICR11 [R/W] --- 11111	
00044C _H	ICR12 [R/W] --- 11111	ICR13[R/W] --- 11111	ICR14[R/W] --- 11111	ICR15[R/W] --- 11111	
000450 _H	ICR16[R/W] --- 11111	ICR17[R/W] --- 11111	ICR18 [R/W] --- 11111	ICR19 [R/W] --- 11111	

Address	Register				Block
	+0	+1	+2	+3	
000454 _H	ICR20 [R/W] --- 11111	ICR21 [R/W] --- 11111	ICR22 [R/W] --- 11111	ICR23 [R/W] --- 11111	Interrupt Control Unit
000458 _H	ICR24[R/W] --- 11111	ICR25[R/W] --- 11111	ICR26[R/W] --- 11111	ICR27[R/W] --- 11111	
00045C _H	ICR28[R/W] --- 11111	ICR29 [R/W] --- 11111	ICR30[R/W] --- 11111	ICR31[R/W] --- 11111	
000460 _H	ICR32[R/W] --- 11111	ICR33[R/W] --- 11111	ICR34[R/W] --- 11111	ICR35[R/W] --- 11111	
000464 _H	ICR36[R/W] --- 11111	ICR37[R/W] --- 11111	ICR38 [R/W] --- 11111	ICR39 [R/W] --- 11111	
000468 _H	ICR40[R/W] --- 11111	ICR41[R/W] --- 11111	ICR42 [R/W] --- 11111	ICR43 [R/W] --- 11111	
00046C _H	ICR44[R/W] --- 11111	ICR45[R/W] --- 11111	ICR46[R/W] --- 11111	ICR47[R/W] --- 11111	
000470 _H	ICR48 [R/W] --- 11111	ICR49 [R/W] --- 11111	ICR50 [R/W] --- 11111	ICR51 [R/W] --- 11111	
000474 _H	ICR52[R/W] --- 11111	ICR53[R/W] --- 11111	ICR54[R/W] --- 11111	ICR55[R/W] --- 11111	
000478 _H	ICR56 [R/W] --- 11111	ICR57[R/W] --- 11111	ICR58 [R/W] --- 11111	ICR59 [R/W] --- 11111	
00047C _H	ICR60[R/W] --- 11111	ICR61 [R/W] --- 11111	ICR62 [R/W] --- 11111	ICR63 [R/W] --- 11111	Clock Control Unit
000480 _H	RSRR [R/W] 10000000	STCR [R/W] 001100-1	TBCR [R/W] 00XXXXX00	CTBR [W] XXXXXXXXXX	
000484 _H	CLKR [R/W] ----- 000	WPR [W] XXXXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	PLL Clock Gear Unit
000488 _H	Reserved				
00048C _H	PLLDIVM [R/W] ---- 0000	PLLDIVN [R/W] -- 000000	PLLDIVG [R/W] ---- 0000	PLLMULG [R/W] 00000000	Real Time Clock (Watch Timer)
000490 _H	PLLCTRL [R/W] ---- 0000	Reserved			
000494 _H	Reserved				Reserved
000498 _H	PORTEN [R/W] ----- 00	Reserved			Port Input Enable Control
00049C _H	Reserved				Reserved
0004A0 _H	Reserved	WTCER [R/W] ----- 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4 _H	Reserved	WTBR [R/W] --- XXXXX XXXXXXXX XXXXXXXX			
0004A8 _H	WTHR [R/W] --- 00000	WTMR [R/W] -- 000000	WTSR [R/W] -- 000000	Reserved	
0004AC _H	Reserved		CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock Monitor
0004B0 _H , 0004B4 _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
0004B8 _H	CMPR [R/W] -- 000010 11111101		Reserved	CMCR [R/W] - 001 -- 00	Clock Modulator
0004BC _H	CMT1 [R/W] 00000000 1 --- 0000		CMT2 [R/W] -- 000000 -- 000000		
0004C0 _H	CANPRE [R/W] 00000000	CANCKD [R/W] -- 00 ----	Reserved		CAN Clock Control
0004C4 _H	Reserved	LVDET [R/W] 00000 - 00	HWWE [R/W] ----- 00	HWWD [R/W, W] 00011000	Low-voltage Detection
0004C8 _H	OSCRH [R/W] 000 -- 001	OSCRL [R/W] ----- 000	Reserved		Main-Oscillation Stabilization Timer
0004CC _H	Reserved				
0004D0 _H to 0007F8 _H	Reserved				Reserved
0007FC _H	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800 _H to 000CFC _H	Reserved				Reserved
000D00 _H to 000D08 _H	Reserved				R-bus Port Data Direct Read Register
000D0C _H	Reserved		PDRD14 [R] ---- XXXX	PDRD15 [R] ---- XXXX	
000D10 _H	Reserved	PDRD17 [R] XXXXXXXX	Reserved		
000D14 _H	PDRD20 [R] - XXX- XXX	PDRD21 [R] - XXX- XXX	PDRD22 [R] ---- XXXX	Reserved	
000D18 _H	PDRD24 [R] XXXXXXXX	Reserved			
000D1C _H	Reserved	PDRD29 [R] XXXXXXXX	Reserved		
000D20 _H	Reserved				
000D24 _H to 000D3C _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000D40 _H to 000D48 _H	Reserved				R-bus Port Direction Register
000D4C _H	Reserved		DDR14 [R/W] ---- 0000	DDR15 [R/W] ---- 0000	
000D50 _H	Reserved	DDR17 [R/W] 00000000	Reserved		
000D54 _H	DDR20 [R/W] -000- 000	DDR21 [R/W] -000- 000	DDR22 [R/W] ---- 0000	Reserved	
000D58 _H	DDR24 [R/W] 00000000	Reserved			
000D5C _H	Reserved	DDR29 [R/W] 00000000	Reserved		
000D60 _H	Reserved				
000D64 _H to 000D7C _H	Reserved				Reserved
000D80 _H to 000D88 _H	Reserved				R-bus Port Function Register
000D8C _H	Reserved		PFR14 [R/W] ---- 0000	PFR15 [R/W] ---- 0000	
000D90 _H	Reserved	PFR17 [R/W] 00000000	Reserved		
000D94 _H	PFR20 [R/W] -000- 000	PFR21 [R/W] -000- 000	PFR22 [R/W] ---- 0000	Reserved	
000D98 _H	PFR24 [R/W] 00000000	Reserved			
000D9C _H	Reserved	PFR29 [R/W] 00000000	Reserved		
000DA0 _H	Reserved				
000DA4 _H to 000DBC _H	Reserved				Reserved
000DC0 _H to 000DC8 _H	Reserved				R-bus Extension Port Function Register
000DCC _H	Reserved		EPFR14 [R/W] ---- 0000	EPFR15 [R/W] ---- 0000	
000DD0 _H	Reserved				R-bus Extension Port Function Register
000DD4 _H	EPFR20 [R/W] - 000- 000	EPFR21 [R/W] - 0- - - 0- -	Reserved		
000DD8 _H	Reserved				
000DDC _H	Reserved				
000DE0 _H	Reserved				
000DE4 _H to 000DFC _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000E00 _H to 000E08 _H	Reserved				R-bus Port Output Drive Select Register
000E0C _H	Reserved		PODR14 [R/W] ---- 0000	PODR15 [R/W] ---- 0000	
000E10 _H	Reserved	PODR17 [R/W] 00000000	Reserved		
000E14 _H	PODR20 [R/W] - 000- 000	PODR21 [R/W] - 000- 000	PODR22 [R/W] ---- 0000	Reserved	
000E18 _H	PODR24 [R/W] 00000000	Reserved			
000E1C _H	Reserved	PODR29 [R/W] 00000000	Reserved		
000E20 _H	Reserved				
000E24 _H to 000E3C _H	Reserved				Reserved
000E40 _H to 000E48 _H	Reserved				R-bus Pin Input Level Select Register
000E4C _H	Reserved		PILR14 [R/W] ---- 0000	PILR15 [R/W] ---- 0000	
000E50 _H	Reserved	PILR17 [R/W] 00000000	Reserved		
000E54 _H	PILR20 [R/W] - 000- 000	PILR21 [R/W] -000- 000	PILR22 [R/W] ---- 0000	Reserved	
000E58 _H	PILR24 [R/W] 00000000	Reserved			
000E5C _H	Reserved	PILR29 [R/W] 00000000	Reserved		
000E60 _H	Reserved				
000E64 _H to 000E7C _H	Reserved				Reserved
000E80 _H to 000E88 _H	Reserved				R-bus Port Extra Input Level Select Register
000E8C _H	Reserved		EPILR14 [R/W] ---- 0000	EPILR15 [R/W] ---- 0000	
000E90 _H	Reserved	EPILR17 [R/W] 00000000	Reserved		
000E94 _H	EPILR20 [R/W] - 000- 000	EPILR21 [R/W] - 000- 000	EPILR22 [R/W] ---- 0000	Reserved	
000E98 _H	EPILR24 [R/W] 00000000	Reserved			
000E9C _H , 000EA0 _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000EA4 _H to 000EBC _H	Reserved				Reserved
000EC0 _H to 000EC8 _H	Reserved				R-bus Port Pull-up/down Enable Register
000ECC _H	Reserved		PPER14 [R/W] ---- 0000	PPER15 [R/W] ---- 0000	
000ED0 _H	Reserved	PPER17 [R/W] 00000000	Reserved		
000ED4 _H	PPER20 [R/W] -000- 000	PPER21 [R/W] -000- 000	PPER22 [R/W] ---- 0000	Reserved	
000ED8 _H	PPER24 [R/W] 00000000	Reserved			
000EDC _H	Reserved	PPER29 [R/W] 00000000	Reserved		
000EE0 _H	Reserved				
000EE4 _H to 000EFC _H	Reserved				Reserved
000F00 _H to 000F08 _H	Reserved				R-bus Port Pull-up/down Control- Register
000F0C _H	Reserved		PPCR14 [R/W] ---- 1111	PPCR15 [R/W] ---- 1111	R-bus Port Pull-up/down Control Register
000F10 _H	Reserved	PPCR17 [R/W] 11111111	Reserved		
000F14 _H	PPCR20 [R/W] -111-111	PPCR21 [R/W] -111-111	PPCR22 [R/W] ---- 1111	Reserved	
000F18 _H	PPCR24 [R/W] 11111111	Reserved			
000F1C _H	Reserved	PPCR29 [R/W] 11111111	Reserved		
000F20 _H	Reserved				
000F24 _H to 000F3C _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000 _H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004 _H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008 _H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100C _H	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010 _H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014 _H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018 _H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101C _H	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020 _H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024 _H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028 _H to 006FFC _H	Reserved				Reserved
007000 _H	FMCS [R/W] 01101000	FMCR [R/W] --- -0000	FCHCR [R/W] -----00 10000011		Flash Memory/ I-Cache Control Register
007004 _H	FMWT [R/W] 11111111 01011101		FMWT2 [R/W] - 101 ----	FMPS [R/W] ----- 000	
007008 _H	FMAC [R] ----- -- 00000 000000000 00000000				
00700C _H	FCHA0 [R/W] ----- - 0000000 000000000 00000000				I-Cache Non-cacheable area setting Register
007010 _H	FCHA1 [R/W] ----- - 0000000 000000000 00000000				
007014 _H to 00AFFC _H	Reserved				Reserved
00B000 _H to 00BFFC _H	BI-ROM size is 4 Kbytes : 00B000 _H to 00BFFF _H				BI-ROM 4 Kbytes
00C000 _H to 00C3FC _H	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
00C400 _H	CTRLR4 [R/W] 00000000 00000001		STATR4 [R/W] 00000000 00000000		CAN 4 Control Register
00C404 _H	ERRCNT4 [R] 00000000 00000000		BTR4 [R/W] 00100011 00000001		
00C408 _H	INTR4 [R] 00000000 00000000		TESTR4 [R/W] 00000000 X0000000		
00C40C _H	BRPE4 [R/W] 00000000 00000000		Reserved		
00C410 _H	IF1CREQ4 [R/W] 00000000 00000001		IF1CMSK4 [R/W] 00000000 00000000		CAN 4 IF1 Register
00C414 _H	IF1MSK24 [R/W] 11111111 11111111		IF1MSK14 [R/W] 11111111 11111111		
00C418 _H	IF1ARB24 [R/W] 00000000 00000000		IF1ARB14 [R/W] 00000000 00000000		
00C41C _H	IF1MCTR4 [R/W] 00000000 00000000		Reserved		
00C420 _H	IF1DTA14 [R/W] 00000000 00000000		IF1DTA24 [R/W] 00000000 00000000		
00C424 _H	IF1DTB14 [R/W] 00000000 00000000		IF1DTB24 [R/W] 00000000 00000000		
00C428 _H , 00C42C _H	Reserved				
00C430 _H	IF1DTA24 [R/W] 00000000 00000000		IF1DTA14 [R/W] 00000000 00000000		CAN 4 IF1 Register
00C434 _H	IF1DTB24 [R/W] 00000000 00000000		IF1DTB14 [R/W] 00000000 00000000		
00C438 _H , 00C43C _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C440 _H	IF2CREQ4 [R/W] 00000000 00000001		IF2CMSK4 [R/W] 00000000 00000000		CAN 4 IF2 Register
00C444 _H	IF2MSK24 [R/W] 11111111 11111111		IF2MSK14 [R/W] 11111111 11111111		
00C448 _H	IF2ARB24 [R/W] 00000000 00000000		IF2ARB14 [R/W] 00000000 00000000		
00C44C _H	IF2MCTR4 [R/W] 00000000 00000000		Reserved		
00C450 _H	IF2DTA14 [R/W] 00000000 00000000		IF2DTA24 [R/W] 00000000 00000000		
00C454 _H	IF2DTB14 [R/W] 00000000 00000000		IF2DTB24 [R/W] 00000000 00000000		
00C458 _H , 00C45C _H	Reserved				
00C460 _H	IF2DTA24 [R/W] 00000000 00000000		IF2DTA14 [R/W] 00000000 00000000		
00C464 _H	IF2DTB24 [R/W] 00000000 00000000		IF2DTB14 [R/W] 00000000 00000000		
00C468 _H to 00C47C _H	Reserved				
00C480 _H	TREQR24 [R] 00000000 00000000		TREQR14 [R] 00000000 00000000		CAN 4 Status Flags
00C484 _H	TREQR44 [R] 00000000 00000000		TREQR34 [R] 00000000 00000000		
00C488 _H	TREQR64 [R] 00000000 00000000		TREQR54 [R] 00000000 00000000		
00C48C _H	TREQR84 [R] 00000000 00000000		TREQR74 [R] 00000000 00000000		
00C490 _H	NEWDT24 [R] 00000000 00000000		NEWDT14 [R] 00000000 00000000		
00C494 _H	NEWDT44 [R] 00000000 00000000		NEWDT34 [R] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
00C498 _H	NEWDT64 [R] 00000000 00000000		NEWDT54 [R] 00000000 00000000		CAN 4 Status Flags
00C49C _H	NEWDT84 [R] 00000000 00000000		NEWDT74 [R] 00000000 00000000		
00C4A0 _H	INTPND24 [R] 00000000 00000000		INTPND14 [R] 00000000 00000000		
00C4A4 _H	INTPND44 [R] 00000000 00000000		INTPND34 [R] 00000000 00000000		
00C4A8 _H	INTPND64 [R] 00000000 00000000		INTPND54 [R] 00000000 00000000		
00C4AC _H	INTPND84 [R] 00000000 00000000		INTPND74 [R] 00000000 00000000		
00C4B0 _H	MSGVAL24 [R] 00000000 00000000		MSGVAL14 [R] 00000000 00000000		
00C4B4 _H	MSGVAL44 [R] 00000000 00000000		MSGVAL34 [R] 00000000 00000000		
00C4B8 _H	MSGVAL64 [R] 00000000 00000000		MSGVAL54 [R] 00000000 00000000		
00C4BC _H	MSGVAL84 [R] 00000000 00000000		MSGVAL74 [R] 00000000 00000000		
00C4C0 _H to 00C4FC _H	Reserved				
00C500 _H	CTRLR5 [R/W] 00000000 00000001		STATR5 [R/W] 00000000 00000000		CAN 5 Control Register
00C504 _H	ERRCNT5 [R] 00000000 00000000		BTR5 [R/W] 00100011 00000001		
00C508 _H	INTR5 [R] 00000000 00000000		TESTR5 [R/W] 00000000 X0000000		
00C50C _H	BRPE5 [R/W] 00000000 00000000		Reserved		
00C510 _H	IF1CREQ5 [R/W] 00000000 00000001		IF1CMSK5 [R/W] 00000000 00000000		CAN 5 IF1 Register
00C514 _H	IF1MSK25 [R/W] 11111111 11111111		IF1MSK15 [R/W] 11111111 11111111		
00C518 _H	IF1ARB25 [R/W] 00000000 00000000		IF1ARB15 [R/W] 00000000 00000000		
00C51C _H	IF1MCTR5 [R/W] 00000000 00000000		Reserved		
00C520 _H	IF1DTA15 [R/W] 00000000 00000000		IF1DTA25 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
00C524 _H	IF1DTB15 [R/W] 00000000 00000000		IF1DTB25 [R/W] 00000000 00000000		CAN 5 IF1 Register
00C528 _H , 00C52C _H	Reserved				
00C530 _H	IF1DTA25 [R/W] 00000000 00000000		IF1DTA15 [R/W] 00000000 00000000		
00C534 _H	IF1DTB25 [R/W] 00000000 00000000		IF1DTB15 [R/W] 00000000 00000000		
00C538 _H , 00C53C _H	Reserved				
00C540 _H	IF2CREQ5 [R/W] 00000000 00000001		IF2CMSK5 [R/W] 00000000 00000000		CAN 5 IF2 Register
00C544 _H	IF2MSK25 [R/W] 11111111 11111111		IF2MSK15 [R/W] 11111111 11111111		
00C548 _H	IF2ARB25 [R/W] 00000000 00000000		IF2ARB15 [R/W] 00000000 00000000		
00C54C _H	IF2MCTR5 [R/W] 00000000 00000000		Reserved		
00C550 _H	IF2DTA15 [R/W] 00000000 00000000		IF2DTA25 [R/W] 00000000 00000000		
00C554 _H	IF2DTB15 [R/W] 00000000 00000000		IF2DTB25 [R/W] 00000000 00000000		
00C558 _H , 00C55C _H	Reserved				
00C560 _H	IF2DTA25 [R/W] 00000000 00000000		IF2DTA15 [R/W] 00000000 00000000		
00C564 _H	IF2DTB25 [R/W] 00000000 00000000		IF2DTB15 [R/W] 00000000 00000000		
00C568 _H to 00C57C _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00C580 _H	TREQR25 [R] 00000000 00000000		TREQR15 [R] 00000000 00000000		CAN 5 Status Flags
00C584 _H	TREQR45 [R] 00000000 00000000		TREQR35 [R] 00000000 00000000		
00C588 _H	TREQR65 [R] 00000000 00000000		TREQR55 [R] 00000000 00000000		
00C58C _H	TREQR85 [R] 00000000 00000000		TREQR75 [R] 00000000 00000000		
00C590 _H	NEWDT25 [R] 00000000 00000000		NEWDT15 [R] 00000000 00000000		
00C594 _H	NEWDT45 [R] 00000000 00000000		NEWDT35 [R] 00000000 00000000		
00C598 _H	NEWDT65 [R] 00000000 00000000		NEWDT55 [R] 00000000 00000000		
00C59C _H	NEWDT85 [R] 00000000 00000000		NEWDT75 [R] 00000000 00000000		
00C5A0 _H	INTPND25 [R] 00000000 00000000		INTPND15 [R] 00000000 00000000		
00C5A4 _H	INTPND45 [R] 00000000 00000000		INTPND35 [R] 00000000 00000000		
00C5A8 _H	INTPND65 [R] 00000000 00000000		INTPND55 [R] 00000000 00000000		
00C5AC _H	INTPND85 [R] 00000000 00000000		INTPND75 [R] 00000000 00000000		
00C5B0 _H	MSGVAL25 [R] 00000000 00000000		MSGVAL15 [R] 00000000 00000000		
00C5B4 _H	MSGVAL45 [R] 00000000 00000000		MSGVAL35 [R] 00000000 00000000		
00C5B8 _H	MSGVAL65 [R] 00000000 00000000		MSGVAL55 [R] 00000000 00000000		
00C5BC _H	MSGVAL85 [R] 00000000 00000000		MSGVAL75 [R] 00000000 00000000		
00C5C0 _H to 00EFC _H	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
00F00 _H	BCTRL [R/W] ----- 11111100 00000000				EDSU / MPU
00F04 _H	BSTAT [R/W] ----- 000 00000000 10 -- 0000				
00F08 _H	BIAC [R] 00000000 00000000 00000000 00000000				
00F0C _H	BOAC [R] 00000000 00000000 00000000 00000000				
00F10 _H	BIRQ [R/W] 00000000 00000000 00000000 00000000				
00F14 _H to 00F01C _H	Reserved				
00F20 _H	BCR0 [R/W] ----- 00000000 00000000 00000000				
00F24 _H	BCR1 [R/W] ----- 00000000 00000000 00000000				
00F28 _H	BCR2 [R/W] ----- 00000000 00000000 00000000				
00F2C _H	BCR3 [R/W] ----- 00000000 00000000 00000000				
00F30 _H to 00F03C _H	Reserved				
00F40 _H to 00F07C _H	Reserved				Reserved
00F80 _H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F84 _H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F88 _H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F8C _H	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F90 _H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F94 _H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F98 _H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F9C _H	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A0 _H	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
00F0A4 _H	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F0A8 _H	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC _H	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0 _H	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4 _H	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8 _H	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC _H	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0 _H to 00F0FC _H	Reserved				
00F100 _H to 02DFFC _H	Reserved				Reserved
02E000 _H to 02FFFC _H	CY91F463NA/F463NC Data RAM size is 8 Kbytes: 02E000 _H to 02FFFF _H (data access is 0 wait cycle)				D-RAM 8 Kbytes
030000 _H to 0307FC _H	CY91F463NA/F463NC Instruction/data RAM size is 2 Kbytes: 030000 _H to 0307FF _H (instruction access is 0 wait cycle, data access is 1 wait cycle)				I/D-RAM 2 Kbytes
030800 _H to 0BFFFC _H	Reserved				Reserved
0C0000 _H to 0DFFFC _H	ROMS04 area (128 Kbytes)				Flash memory 256 Kbytes
0E0000 _H to 0FFFF4 _H	ROMS05 area (128 Kbytes)				
0FFFF8 _H	FMV [R] XXXXXXXX _H				Reset/Mode Vector
0FFFFC _H	FRV [R] XXXXXXXX _H				
100000 _H to 147FFC _H	Reserved				Reserved
148000 _H to 14FFFC _H	ROMS07 area (32 Kbytes)				Flash memory 32 Kbytes
148000 _H to 4FFFC _H	Reserved				Reserved

1. The lower 16 bits (DTC15 to DTC0) of DMACA0 to DMACA4 cannot be accessed in bytes.

14. Interrupt Source Table

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		Resource number ^[1]
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Default vector address	
Reset	0	00	-	-	3FC _H	000FFFFC _H	-
Mode vector	1	01	-	-	3F8 _H	000FFFF8 _H	-
System reserved	2	02	-	-	3F4 _H	000FFFF4 _H	-
System reserved	3	03	-	-	3F0 _H	000FFFF0 _H	-
System reserved	4	04	-	-	3EC _H	000FFFE _C	-
CPU supervisor mode (INT #5 instruction) ^[2]	5	05	-	-	3E8 _H	000FFFE8 _H	-
Memory protection exception ^[2]	6	06	-	-	3E4 _H	000FFFE4 _H	-
System reserved	7	07	-	-	3E0 _H	000FFFE0 _H	-
System reserved	8	08	-	-	3DC _H	000FFFD _C	-
System reserved	9	09	-	-	3D8 _H	000FFFD8 _H	-
System reserved	10	0A	-	-	3D4 _H	000FFFD4 _H	-
System reserved	11	0B	-	-	3D0 _H	000FFFD0 _H	-
System reserved	12	0C	-	-	3CC _H	000FFFC _C	-
System reserved	13	0D	-	-	3C8 _H	000FFFC8 _H	-
Undefined instruction exception	14	0E	-	-	3C4 _H	000FFFC4 _H	-
NMI request	15	0F	F _H fixed		3C0 _H	000FFFC0 _H	-
External interrupt 0	16	10	ICR00	440 _H	3BC _H	000FFFB _C	0, 16
External interrupt 1	17	11			3B8 _H	000FFFB8 _H	1, 17
External interrupt 2	18	12	ICR01	441 _H	3B4 _H	000FFFB4 _H	2, 18
External interrupt 3	19	13			3B0 _H	000FFFB0 _H	3, 19
External interrupt 4	20	14	ICR02	442 _H	3AC _H	000FFFA _C	20
External interrupt 5	21	15			3A8 _H	000FFFA8 _H	21
External interrupt 6	22	16	ICR03	443 _H	3A4 _H	000FFFA4 _H	22
External interrupt 7	23	17			3A0 _H	000FFFA0 _H	23
System reserved	24	18	ICR04	444 _H	39C _H	000FFF9 _C	-
System reserved	25	19			398 _H	000FFF98 _H	-
System reserved	26	1A	ICR05	445 _H	394 _H	000FFF94 _H	-
System reserved	27	1B			390 _H	000FFF90 _H	-
External interrupt 12	28	1C	ICR06	446 _H	38C _H	000FFF8 _C	-
External interrupt 13	29	1D			388 _H	000FFF88 _H	-
System reserved	30	1E	ICR07	447 _H	384 _H	000FFF84 _H	-
System reserved	31	1F			380 _H	000FFF80 _H	-
Reload timer 0	32	20	ICR08	448 _H	37C _H	000FFF7 _C	4, 32
Reload timer 1	33	21			378 _H	000FFF78 _H	5, 33
Reload timer 2	34	22	ICR09	449 _H	374 _H	000FFF74 _H	34
Reload timer 3	35	23			370 _H	000FFF70 _H	35
System reserved	36	24	ICR10	44A _H	36C _H	000FFF6 _C	36
System reserved	37	25			368 _H	000FFF68 _H	37

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		Resource number ^[1]
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Default vector address	
System reserved	38	26	ICR11	44B _H	364 _H	000FFF64 _H	38
Reload timer 7	39	27			360 _H	000FFF60 _H	39
Free-run timer 0	40	28	ICR12	44C _H	35C _H	000FFF5C _H	40
Free-run timer 1	41	29			358 _H	000FFF58 _H	41
Free-run timer 2	42	2A	ICR13	44D _H	354 _H	000FFF54 _H	42
Free-run timer 3	43	2B			350 _H	000FFF50 _H	43
System reserved	44	2C	ICR14	44E _H	34C _H	000FFF4C _H	44
System reserved	45	2D			348 _H	000FFF48 _H	45
System reserved	46	2E	ICR15	44F _H	344 _H	000FFF44 _H	46
System reserved	47	2F			340 _H	000FFF40 _H	47
System reserved	48	30	ICR16	450 _H	33C _H	000FFF3C _H	-
System reserved	49	31			338 _H	000FFF38 _H	-
System reserved	50	32	ICR17	451 _H	334 _H	000FFF34 _H	-
System reserved	51	33			330 _H	000FFF30 _H	-
CAN 4	52	34	ICR18	452 _H	32C _H	000FFF2C _H	-
CAN 5	53	35			328 _H	000FFF28 _H	-
LIN-USART0 RX	54	36	ICR19	453 _H	324 _H	000FFF24 _H	6, 48
LIN-USART0 TX	55	37			320 _H	000FFF20 _H	7, 49
LIN-USART1 RX	56	38	ICR20	454 _H	31C _H	000FFF1C _H	8, 50
LIN-USART1 TX	57	39			318 _H	000FFF18 _H	9, 51
LIN-USART2 RX	58	3A	ICR21	455 _H	314 _H	000FFF14 _H	52
LIN-USART2 TX	59	3B			310 _H	000FFF10 _H	53
LIN-USART3 RX	60	3C	ICR22	456 _H	30C _H	000FFF0C _H	54
LIN-USART3 TX	61	3D			308 _H	000FFF08 _H	55
System reserved	62	3E	ICR23 ^[3]	457 _H	304 _H	000FFF04 _H	-
Delayed interrupt	63	3F			300 _H	000FFF00 _H	-
System reserved ^[4]	64	40	(ICR24)	(458 _H)	2FC _H	000FFEFC _H	-
System reserved ^[4]	65	41			2F8 _H	000FFE8 _H	-
System reserved	66	42	ICR25	459 _H	2F4 _H	000FFE4 _H	10, 56
System reserved	67	43			2F0 _H	000FFE0 _H	11, 57
System reserved	68	44	ICR26	45A _H	2EC _H	000FEEC _H	12, 58
System reserved	69	45			2E8 _H	000FEE8 _H	13, 59
System reserved	70	46	ICR27	45B _H	2E4 _H	000FEE4 _H	60
System reserved	71	47			2E0 _H	000FEE0 _H	61
System reserved	72	48	ICR28	45C _H	2DC _H	000FEDC _H	62
System reserved	73	49			2D8 _H	000FED8 _H	63
I ² C 2	74	4A	ICR29	45D _H	2D4 _H	000FED4 _H	-
I ² C 3	75	4B			2D0 _H	000FED0 _H	-

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		Resource number ^[1]
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Default vector address	
System reserved	76	4C	ICR30	45E _H	2CC _H	000FFECC _H	64
System reserved	77	4D			2C8 _H	000FFEC8 _H	65
System reserved	78	4E	ICR31	45F _H	2C4 _H	000FFEC4 _H	66
System reserved	79	4F			2C0 _H	000FFEC0 _H	67
System reserved	80	50	ICR32	460 _H	2BC _H	000FFECB _H	68
System reserved	81	51			2B8 _H	000FFEB8 _H	69
System reserved	82	52	ICR33	461 _H	2B4 _H	000FFEB4 _H	70
System reserved	83	53			2B0 _H	000FFEB0 _H	71
System reserved	84	54	ICR34	462 _H	2AC _H	000FFEAC _H	72
System reserved	85	55			2A8 _H	000FFEA8 _H	73
System reserved	86	56	ICR35	463 _H	2A4 _H	000FFEA4 _H	74
System reserved	87	57			2A0 _H	000FFEA0 _H	75
System reserved	88	58	ICR36	464 _H	29C _H	000FFE9C _H	76
System reserved	89	59			298 _H	000FFE98 _H	77
System reserved	90	5A	ICR37	465 _H	294 _H	000FFE94 _H	78
System reserved	91	5B			290 _H	000FFE90 _H	79
Input capture 0	92	5C	ICR38	466 _H	28C _H	000FFE8C _H	80
Input capture 1	93	5D			288 _H	000FFE88 _H	81
Input capture 2	94	5E	ICR39	467 _H	284 _H	000FFE84 _H	82
Input capture 3	95	5F			280 _H	000FFE80 _H	83
System reserved	96	60	ICR40	468 _H	27C _H	000FFE7C _H	84
System reserved	97	61			278 _H	000FFE78 _H	85
System reserved	98	62	ICR41	469 _H	274 _H	000FFE74 _H	86
System reserved	99	63			270 _H	000FFE70 _H	87
Output compare 0	100	64	ICR42	46A _H	26C _H	000FFE6C _H	88
Output compare 1	101	65			268 _H	000FFE68 _H	89
Output compare 2	102	66	ICR43	46B _H	264 _H	000FFE64 _H	90
Output compare 3	103	67			260 _H	000FFE60 _H	91
System reserved	104	68	ICR44	46C _H	25C _H	000FFE5C _H	92
System reserved	105	69			258 _H	000FFE58 _H	93
System reserved	106	6A	ICR45	46D _H	254 _H	000FFE54 _H	94
System reserved	107	6B			250 _H	000FFE50 _H	95
System reserved	108	6C	ICR46	46E _H	24C _H	000FFE4C _H	-
Phase Frequency modulator	109	6D			248 _H	000FFE48 _H	-
System reserved	110	6E	ICR47 ^[4]	46F _H	244 _H	000FFE44 _H	-
System reserved	111	6F			240 _H	000FFE40 _H	-
PPG0	112	70	ICR48	470 _H	23C _H	000FFE3C _H	15, 96
PPG1	113	71			238 _H	000FFE38 _H	97

Interrupt source	Interrupt number		Interrupt level		Interrupt vector		Resource number ¹⁾
	Decimal	Hexa-decimal	Setting register	Register address	Offset	Default vector address	
PPG2	114	72	ICR49	471 _H	234 _H	000FFE34 _H	98
PPG3	115	73			230 _H	000FFE30 _H	99
PPG4	116	74	ICR50	472 _H	22C _H	000FFE2C _H	100
PPG5	117	75			228 _H	000FFE28 _H	101
PPG6	118	76	ICR51	473 _H	224 _H	000FFE24 _H	102
PPG7	119	77			220 _H	000FFE20 _H	103
System reserved	120	78	ICR52	474 _H	21C _H	000FFE1C _H	104
System reserved	121	79			218 _H	000FFE18 _H	105
System reserved	122	7A	ICR53	475 _H	214 _H	000FFE14 _H	106
System reserved	123	7B			210 _H	000FFE10 _H	107
System reserved	124	7C	ICR54	476 _H	20C _H	000FFE0C _H	108
System reserved	125	7D			208 _H	000FFE08 _H	109
System reserved	126	7E	ICR55	477 _H	204 _H	000FFE04 _H	110
System reserved	127	7F			200 _H	000FFE00 _H	111
Up/down counter 0	128	80	ICR56	478 _H	1FC _H	000FFDFC _H	-
Up/down counter 1	129	81			1F8 _H	000FFDF8 _H	-
System reserved	130	82	ICR57	479 _H	1F4 _H	000FFDF4 _H	-
System reserved	131	83			1F0 _H	000FFDF0 _H	-
Real time clock	132	84	ICR58	47A _H	1EC _H	000FFDEC _H	-
Calibration unit	133	85			1E8 _H	000FFDE8 _H	-
A/D converter 0	134	86	ICR59	47B _H	1E4 _H	000FFDE4 _H	14, 112
System reserved	135	87			1E0 _H	000FFDE0 _H	-
System reserved	136	88	ICR60	47C _H	1DC _H	000FFDDC _H	-
System reserved	137	89			1D8 _H	000FFDD8 _H	-
Low voltage detection	138	8A	ICR61	47D _H	1D4 _H	000FFDD4 _H	-
System reserved	139	8B			1D0 _H	000FFDD0 _H	-
Time-base overflow	140	8C	ICR62	47E _H	1CC _H	000FFDCC _H	-
PLL clock gear	141	8D			1C8 _H	000FFDC8 _H	-
DMA controller	142	8E	ICR63	47F _H	1C4 _H	000FFDC4 _H	-
Main OSC stability wait	143	8F			1C0 _H	000FFDC0 _H	-
System reserved	144	90	-	-	1BC _H	000FFDBC _H	-
Used by the INT instruction	145 to 255	91 to FF	-	-	1B8 _H to 000 _H	000FFDB8 _H to 000FFC00 _H	-

1. The peripheral resources to which RN (Resource Number) is assigned are capable of being DMA transfer activation sources. In addition, RN respectively corresponds to an IS (Input Source) of the DMAC channel control register A (DMACA0 to DMACA4), and the IS (Input Source) can be obtained by representing RN in a binary number and adding "1" to the head of it.

2. Memory Protection Unit (MPU) support

3. ICR23 can be switched to ICR47 by setting REALOS compatibility bit (address 0C03_H ISO[0]).

4. Used by REALOS

15. Electrical Characteristics

15.1 Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^[1]	V_{CC}	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	
Analog power supply voltage ^[1]	AV_{CC}	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	[2]
Analog power supply voltage ^[1]	$AVRH$	$V_{SS} - 0.5$	$V_{SS} + 6.0$	V	[2]
Input voltage ^[1]	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	[3]
Analog pin input voltage ^[1]	V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Output voltage ^[1]	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	[3]
Maximum clamp current	I_{CLAMP}	- 2.0	+2.0	mA	[4]
Total maximum clamp current	$\Sigma I_{CLAMP} $	-	20	mA	[4]
"L" level maximum output current	I_{OL}	-	10	mA	[5]
"L" level average output current	I_{OLAV}	-	4	mA	[6]
"L" level total maximum output current	ΣI_{OL}	-	100	mA	
"L" level total average output current	ΣI_{OLAV}	-	50	mA	[7]
"H" level maximum output current	I_{OH}	-	- 10	mA	[5]
"H" level average output current	I_{OHAV}	-	- 4	mA	[6]
"H" level total maximum output current	ΣI_{OH}	-	- 100	mA	
"H" level total average output current	ΣI_{OHAV}	-	- 20	mA	[7]
Power consumption	P_D	-	700	mW	
Operation temperature	T_A	-40	+105	°C	When using $V_{CC} = 3.3$ V
		-40	+85	°C	When using $V_{CC} = 5.0$ V
Storage temperature	T_{stg}	- 55	+ 125	°C	

1. The parameter is based on $V_{SS} = AV_{SS} = 0.0$ V.

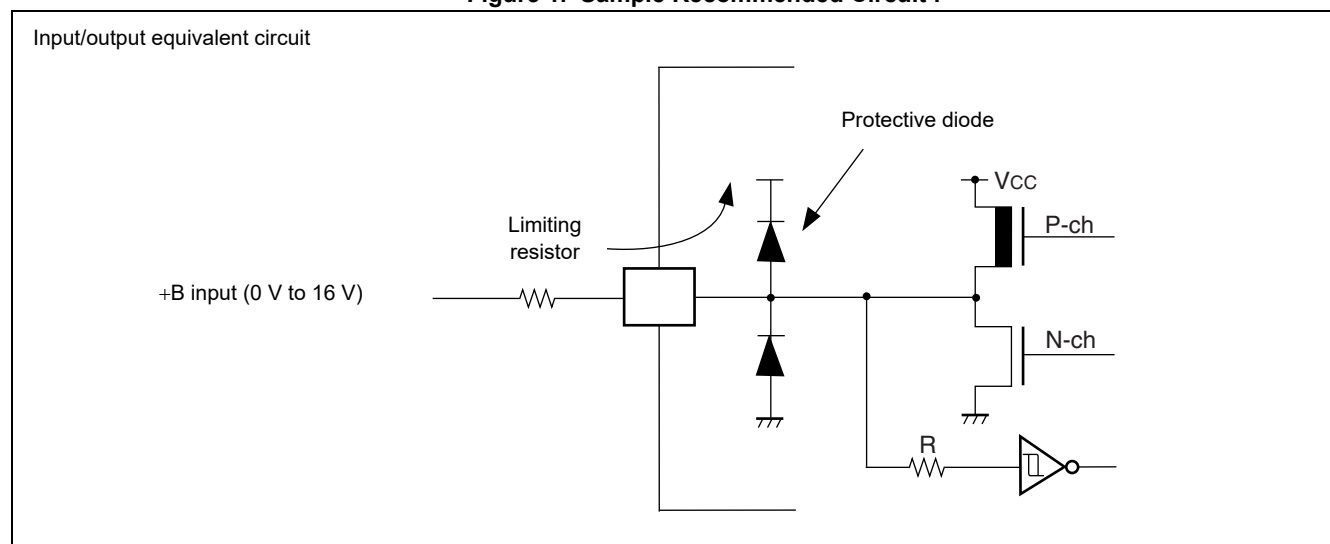
2. AV_{CC} and $AVRH$ must not exceed $V_{CC} + 0.3$ V, for example, at power on. AV_{CC} must not exceed V_{CC} .

3. V_I and V_O must not exceed $V_{CC} + 0.3$ V. However, when the maximum value of the current to the input or the current from the input is limited by using outside parts, I_{CLAMP} ratings are applied in place of V_I ratings.

4.

- Corresponding pins: Pin name P29_0 to P29_7, P24_0 to P24_7, P22_0 to P22_3, P20_0 to P20_2, P20_4 to P20_6, P15_0 to P15_3, P17_0 to P17_7, P21_0 to P21_2, P21_4 to P21_6, P14_0 to P14_3
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The + B signal is an input signal exceeding V_{CC} voltage. The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
 - Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
 - Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
 - Note that if the + B signal is input at power-on, since the power is supplied through the pin, the power supply voltage may become the voltage at which a power-on reset does not work.
 - Do not leave + B input pins open.
Note that analog input/output pins can input the + B signal only at using as a port.
5. Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
6. Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
7. Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

Figure 1. Sample Recommended Circuit :



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2 Recommended Operating Conditions

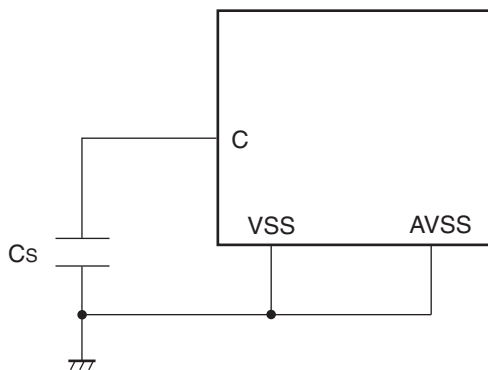
($V_{SS} = AV_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	3.0	3.6	V	When using $V_{CC} = 3.3\text{ V}$
		4.5	5.5	V	When using $V_{CC} = 5.0\text{ V}$
	AV_{CC}	3.0	3.6	V	When using $V_{CC} = 3.3\text{ V}$
		4.5	5.5	V	When using $V_{CC} = 5.0\text{ V}$
Smoothing capacitor	C_S	4.7 (accuracy within $\pm 50\%$)		μF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	$^{\circ}\text{C}$	When using $V_{CC} = 3.3\text{ V}$
		-40	+85	$^{\circ}\text{C}$	When using $V_{CC} = 5.0\text{ V}$

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



15.3 DC Characteristics

($V_{CC} = 3.0\text{ V to }3.6\text{ V / }4.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C / }-40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IHS}	Port pin	When CMOS hysteresis input type1 are selected	$0.7 \times V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IHC}	Port pin	When CMOS hysteresis input type2 are selected	$0.8 \times V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IHA}	Port pin	When Automotive inputs are selected	$0.8 \times V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IHT}	Port pin	When TTL input levels are selected	2.0	-	$V_{CC} + 0.3$	V	
	V_{IH1}	MD2 to MD0	CMOS level input	$0.7 \times V_{CC}$	-	$V_{CC} + 0.3$	V	
	V_{IH2}	MD3, INITX	CMOS hysteresis input	$0.7 \times V_{CC}$	-	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{ILS}	Port pin	When CMOS hysteresis input type1 are selected	$V_{SS} - 0.3$	-	$0.3 \times V_{CC}$	V	
	V_{ILC}	Port pin	When CMOS hysteresis input type2 are selected	$V_{SS} - 0.3$	-	$0.2 \times V_{CC}$	V	
	V_{ILA}	Port pin	When Automotive inputs are selected	$V_{SS} - 0.3$	-	$0.5 \times V_{CC}$	V	
	V_{ILT}	Port pin	When TTL input levels are selected	$V_{SS} - 0.3$	-	0.8	V	
	V_{IL1}	MD2 to MD0	CMOS level input	$V_{SS} - 0.3$	-	$0.3 \times V_{CC}$	V	
	V_{IL2}	MD3, INITX	CMOS hysteresis input	$V_{SS} - 0.3$	-	$0.3 \times V_{CC}$	V	
“H” level output voltage	V_{OH1}	Port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -2.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -1.0\text{ mA}$	$V_{CC} - 0.5$	-	-	V	[1]
	V_{OH2}	I ² C common port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -3.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	-	-	V	
	V_{OH3}	Port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -5.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -3.0\text{ mA}$	$V_{CC} - 0.5$	-	-	V	[1]

($V_{CC} = 3.0\text{ V to } 3.6\text{ V / } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C / } -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	V_{OL1}	Port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -2.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -1.0\text{ mA}$	-	-	0.4	V	[1]
	V_{OL2}	I ² C common port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -3.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -3.0\text{ mA}$	-	-	0.4	V	
	V_{OL3}	Port pin	$V_{CC} = 5.0\text{ V}$, $I_{OH} = -5.0\text{ mA}$ / $V_{CC} = 3.3\text{ V}$, $I_{OH} = -3.0\text{ mA}$	-	-	0.4	V	[1]
Input leak current	I_{IL}	-	$V_{CC} = AV_{CC} = 5.0\text{ V}$, $V_{SS} < V_I < V_{CC}$	-5	-	+5	μA	
Pull-up resistance value	R_{UP}	Port pin	-	25	50	100	$\text{k}\Omega$	
Pull-down resistance value	R_{DOWN}	Port pin	-	25	50	100	$\text{k}\Omega$	

($V_{CC} = 3.0\text{ V to } 3.6\text{ V / } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C / } -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC3}	VCC	$V_{CC} = 3.3\text{ V CPU core: } 80\text{ MHz}$,	-	75	102	mA	$T_A = -40^\circ\text{C to } +105^\circ\text{C}$
	I_{CC5}	VCC	$V_{CC} = 5.0\text{ V CPU core: } 80\text{ MHz}$,	-	75	102	mA	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$
	I_{CCS3}	VCC	$V_{CC} = 3.3\text{ V sleep mode}$	-	15	45	mA	
	I_{CCS5}	VCC	$V_{CC} = 5.0\text{ V sleep mode}$	-	15	45	mA	
	I_{CTS3}	VCC	$V_{CC} = 3.3\text{ V stop mode at using RTC)}^{[3]}$	-	100	550	μA	$T_A = +25^\circ\text{C}$ When the CR oscillator is operating and low voltage detection is enabled.
	I_{CTS5}	VCC	$V_{CC} = 5.0\text{ V stop mode at using RTC)}^{[3]}$	-	200	650	μA	$T_A = +25^\circ\text{C}$ When the CR oscillator is operating and low voltage detection is enabled.
	I_{CCH3}	VCC	$V_{CC} = 3.3\text{ V stop mode oscillation stop)}^{[4]}$	-	100	500	μA	$T_A = +25^\circ\text{C}$ When the CR oscillator is stopping and low voltage detection is enabled.
	I_{CCH5}	VCC	$V_{CC} = 5.0\text{ V stop mode oscillation stop)}^{[4]}$	-	150	600	μA	$T_A = +25^\circ\text{C}$ When the CR oscillator is stopping and low voltage detection is enabled.
	I_{CCF}	VCC	Flash programming (Write/Erase)	-	25	50	mA	^[2]
Input capacitance	C_{IN}	Except VCC, AVCC, VSS, AVSS	-	-	5	15	pF	

1. The drive power varies depending on the power supply voltage (3.3 V, 5.0 V).

2. The power supply current when writing or erasing by executing the automatic algorithm.

3. When the main clock oscillator is stopped and CR oscillator is operating (using the CR oscillator clock in the RTC) and the low voltage detection is enabled.

4. When the main clock oscillator is stopped, the CR oscillator is stopped and the low voltage detection is enabled.

15.4 AC Characteristics

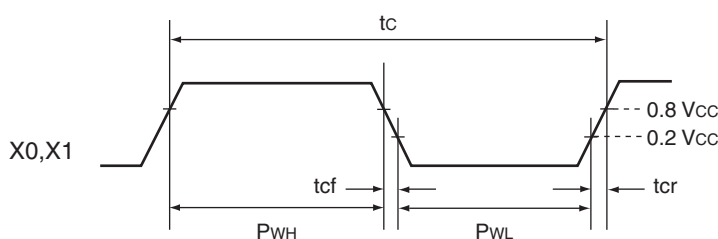
15.4.1 Clock Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V} / 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +125^\circ\text{C} / -40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Sym- bol	Pin Name	Condi- tion	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F _C	X0, X1	-	3.5	4	16	MHz	When using the oscillator circuit
				3.5	-	32	MHz	When using an external clock
Clock cycle time	t _C	X0, X1		62.5	-	285.7	ns	When using the oscillator circuit
				31.25	-	285.7	ns	When using an external clock
Internal operation clock frequency	F _{CP}	-		-	-	80	MHz	CPU clock, when using PLL ^[1]
	F _{CPP}	-		-	-	40	MHz	Peripheral clock
Internal operation clock cycle time	t _{CP}	-		12.5	-	-	ns	CPU clock, when using PLL
	t _{CPP}	-		25	-	-	ns	Peripheral clock
Input clock pulse width	P _{WH} , P _{WL}	X0		30	-	-	ns	
Input clock rise/fall time	tcf, tcr	X0		-	-	5	ns	

1. When using the clock modulator, set such that the maximum value of the modulated frequency is 96 MHz or less.

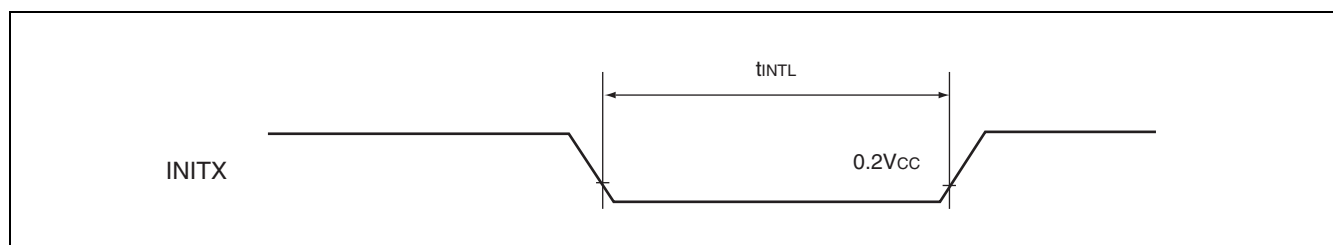
Figure 2. Clock Timing



15.4.2 Reset Input

($V_{CC} = 3.0\text{ V to } 3.6\text{ V/ } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C/-}40^\circ\text{C to } +85^\circ\text{C}$)

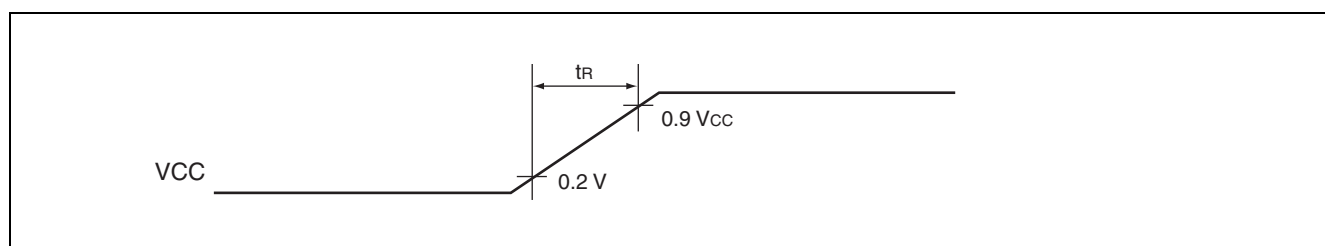
Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on or stop mode)	t_{INTL}	INITX	-	Oscillation stabilization time of oscillator + 2.6	-	ms
INITX input time (other than the above)				20	-	μs



15.4.3 Specification for Power-on

($V_{CC} = 3.0\text{ V to } 3.6\text{ V/ } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C/-}40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Power supply rising time	t_R	VCC	-	0.1	100	ms
Power supply start time	-	-	-	0.2	-	V
Power supply end time	-	-	-	-	$0.9 \times V_{CC}$	V



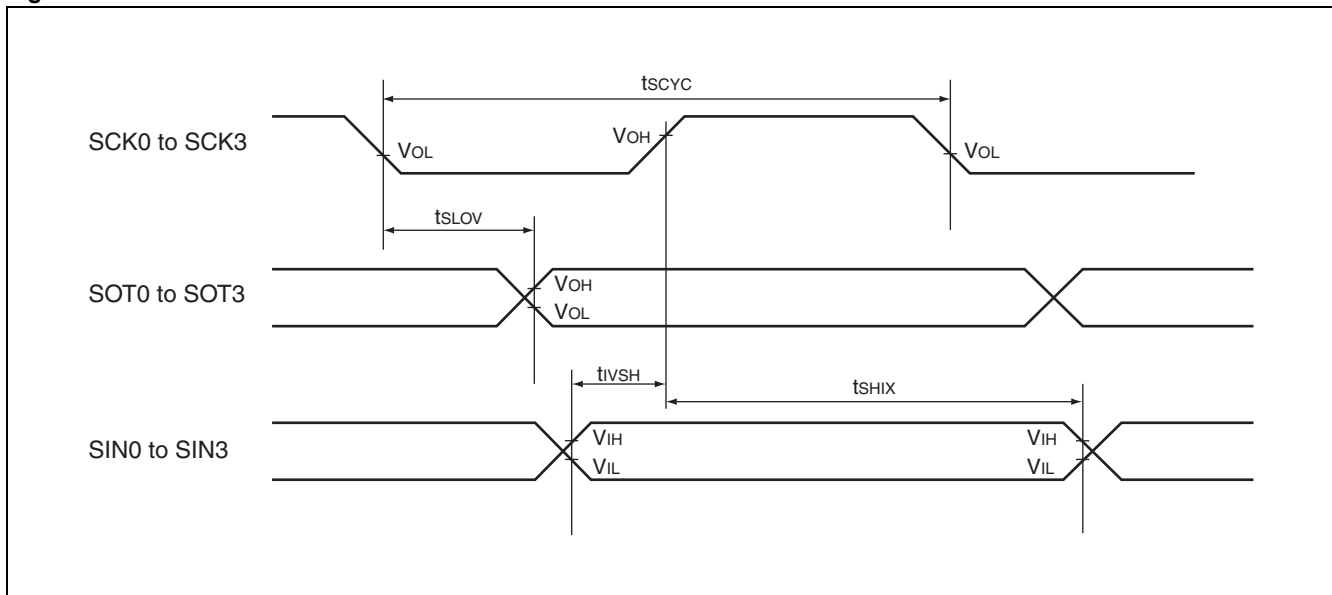
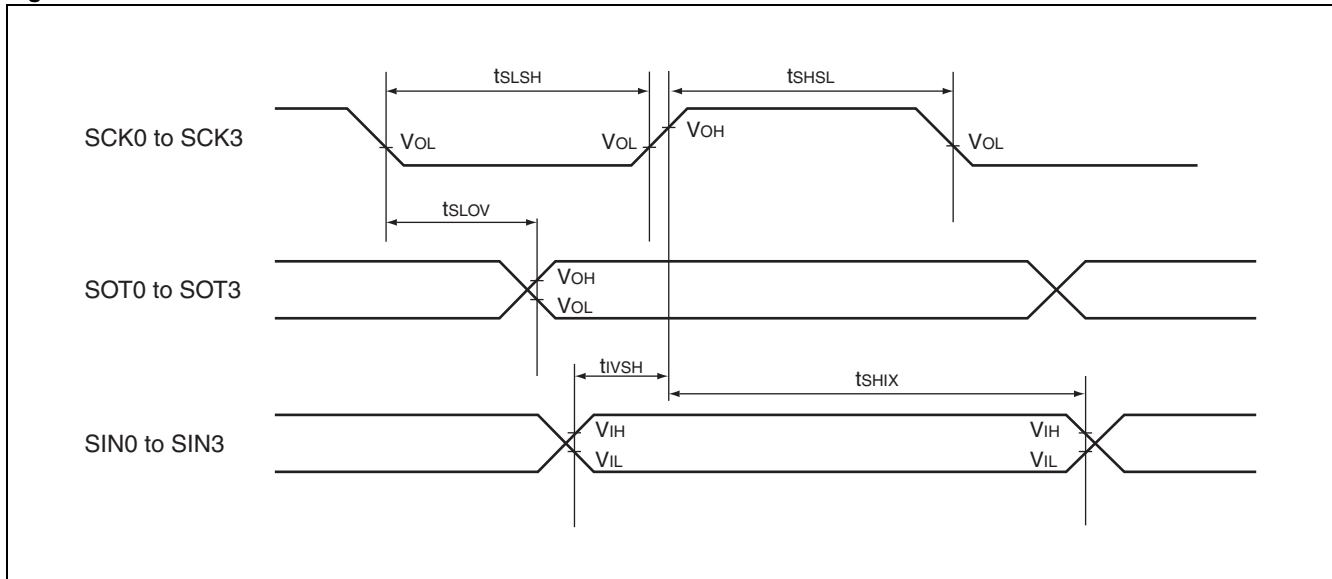
15.4.4 LIN-USART Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V/ }4.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to }+105^\circ\text{C/-}40^\circ\text{C to }+85^\circ\text{C}$)

Parameter	Symbol	Pin Name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK0 to SCK3	Internal shift clock mode	$8 \times t_{CLKP}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		- 80	+ 80	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		100	-	ns
SCK $\uparrow \rightarrow$ valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCK0 to SCK3	External shift clock mode	$4 \times t_{CLKP}$	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK3		$4 \times t_{CLKP}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK3, SOT0 to SOT3		-	150	ns
Valid SIN \rightarrow SCK \uparrow	t_{IVSH}	SCK0 to SCK3, SIN0 to SIN3		60	-	ns
SCK $\uparrow \rightarrow$ Valid SIN hold time	t_{SHIX}	SCK0 to SCK3, SIN0 to SIN3		60	-	ns

Notes:

- Above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

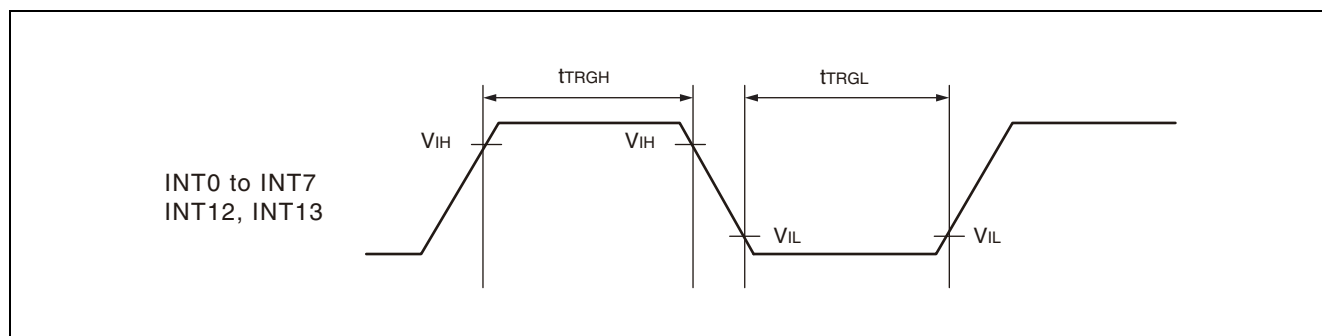
Figure 3. Internal Shift Clock Mode

Figure 4. External Shift Clock Mode


15.4.5 Trigger Input Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V/ } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C/-}40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
External interrupt input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7 INT12, INT13	$4 \times t_{CLKP}$	-	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.

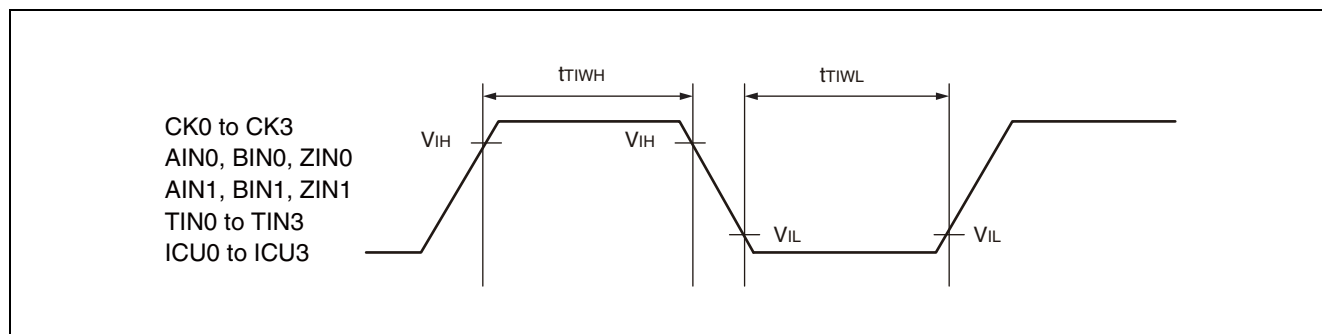


15.4.6 Timer Related Resource Input Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V/ } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40^\circ\text{C to } +105^\circ\text{C/-}40^\circ\text{C to } +85^\circ\text{C}$)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
Free-run timer input clock pulse width	t_{TIWH} t_{TIWL}	CK0 to CK3	$4 \times t_{CLKP}$	-	ns
Up/down counter input pulse width		AIN0, AIN1 BIN0, BIN1 ZIN0, ZIN1	$4 \times t_{CLKP}$	-	ns
Reload timer input pulse width		TIN0 to TIN3	$4 \times t_{CLKP}$	-	ns
Input capture input pulse width		ICU0 to ICU3	$4 \times t_{CLKP}$	-	ns

Note: t_{CLKP} is the cycle time of the peripheral clock.



15.4.7 I²C Timing

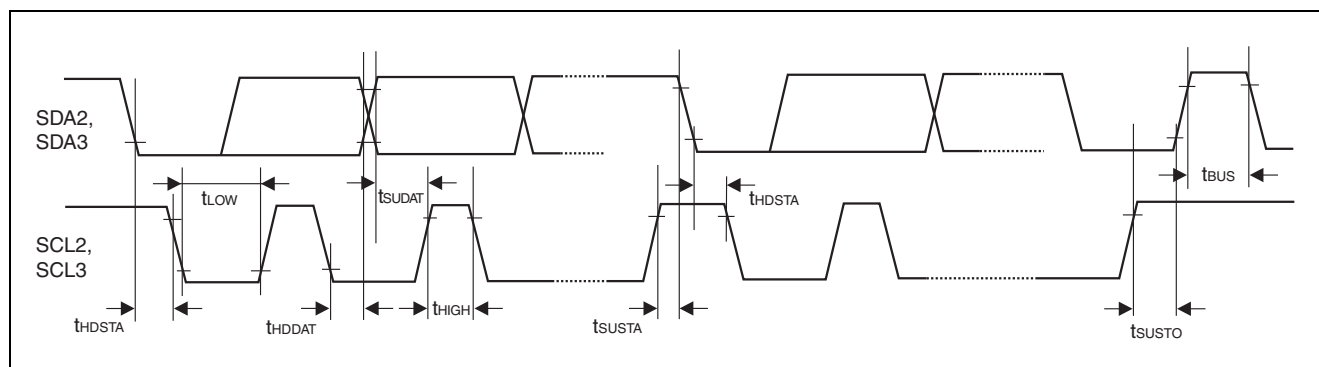
($V_{CC} = 3.0\text{ V to }3.6\text{ V/ }4.5\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C/-40 }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Condition	Standard Mode		Fast Mode ^[1]		Unit
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SDA2, SDA3, SCL2, SCL3	$R = 1\text{ k}\Omega$, $C = 50\text{ pF}$ ^[2]	0	100	0	400	kHz
"L" width of the SCL clock	t_{LOW}			4.7	—	1.3	—	μs
"H" width of the SCL clock	t_{HIGH}			4.0	—	0.6	—	μs
Bus free time between STOP and START conditions	t_{BUS}			4.7	—	1.3	—	μs
SCL $\uparrow \rightarrow$ SDA output delay time	t_{DLDAT}			—	$5 \times t_{CLKP}$	—	$5 \times t_{CLKP}$	ns
Setup time for a repeated START condition SCL $\uparrow \rightarrow$ SDA \downarrow	t_{SUSTA}			4.7	—	0.6	—	μs
Hold time for a repeated START condition SDA $\downarrow \rightarrow$ SCL \downarrow	t_{HDSTA}			4.0	—	0.6	—	μs
Setup time for STOP condition SCL $\uparrow \rightarrow$ SDA \uparrow	t_{SUSTO}			4.0	—	0.6	—	μs
SDA data input hold time SCL $\downarrow \rightarrow$ SDA $\downarrow \uparrow$	t_{HDDAT}			$2 \times t_{CLKP}$	—	$2 \times t_{CLKP}$	—	μs
SDA data input setup time SDA $\downarrow \uparrow \rightarrow$ SCL \uparrow	t_{SUDAT}			250	—	100	—	ns

1. For use at over 100 kHz, set the peripheral clock to at least 6 MHz.

2. R and C are the pull-up resistance and load capacitance of the SCL and SDA lines.

Note: t_{CLKP} is the cycle time of the peripheral clock.



15.5 Electrical Characteristics for A/D Converter

($V_{CC} = 3.0\text{ V to } 3.6\text{ V / } 4.5\text{ V to } 5.5\text{ V}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to } +105\text{ }^{\circ}\text{C / } -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error ^[1]	–	–	–	–	± 3	LSB	
Linearity error ^[1]	–	–	–	–	± 2.5	LSB	
Differential linearity error ^[1]	–	–	–	–	± 1.9	LSB	
Zero transition voltage ^[1]	V_{OT}	AN0 to AN7	$AV_{SS}-1.5\text{ LSB}$	$AV_{SS}-0.5\text{ LSB}$	$AV_{SS}-2.5\text{ LSB}$	V	
Full scale transition voltage ^[1]	V_{FST}	AN0 to AN7	$AVRH-3.5\text{ LSB}$	$AVRH-1.5\text{ LSB}$	$AVRH-0.5\text{ LSB}$	V	
Conversion time	–	–	1 ^[2]	–	–	μs	Using at 5 V
			3 ^[2]	–	–	μs	Using at 3.3 V
Analog port input current	I_{AIN}	AN0 to AN7	–	–	10	μA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	–	$AVRH$	V	
Reference voltage	–	$AVRH$	AV_{SS}	–	AV_{CC}	V	
Analog power supply current (analog + digital)	I_A	$AVCC$	–	2.4	4.7	mA	Including reference supply
Reference voltage supply current	I_R	$AVRH$	–	0.65	1.0	mA	
Analog input equivalent capacitance	C_{in}	AN0 to AN7	–	–	8.5	pF	
Analog input equivalent resistance	R_{in}	AN0 to AN7	–	–	2.6	k Ω	$AV_{CC} \geq 4.5\text{ V}$
			–	–	12.1	k Ω	$AV_{CC} \geq 3.0\text{ V}$
Output impedance of analog signal source	R_{ext}	–	–	–	4.2	k Ω	

1. Measured in the CPU sleep state

2. Set no shorter than this time period in the peripheral clock and conversion setting register

15.6 Notes on the A/D Converter

The diagram below shows the equivalent circuit of the sampling circuit in the A/D converter.

Apply the output impedance in the external circuit for the analog output under the following conditions.

- The recommended output impedance for the external circuit is 4.2 kΩ or less.
- If an external capacitor is used, remember to consider the capacitive voltage divider effect due to the external capacitor and the internal capacitor in the chip. Accordingly, an external capacitance several thousand times that of the internal capacitance is recommended.
- The analog voltage sampling period may be too short if the output impedance of the external circuit is high. In this case, select R_{ext} and T_{smp} to satisfy the following condition.

$$R_{ext} = T_{smp} / (7 \times C_{in}) - R_{in}$$

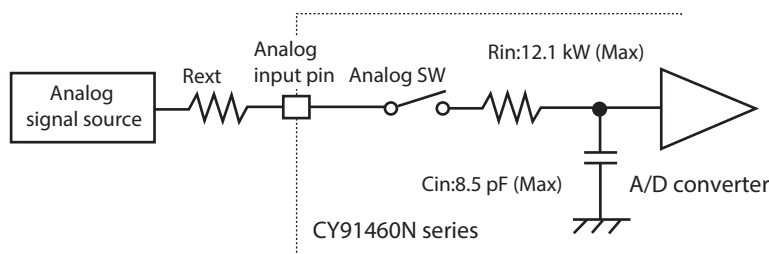
R_{ext} : Output impedance of the analog signal source

T_{smp} : Sampling time

C_{in} : Equivalent capacitance of analog input

R_{in} : Equivalent resistance of analog input

Input impedance



15.7 Definition of A/D Converter Terms

■ Resolution

Analog variation that is recognizable by an A/D converter.

■ Linearity error

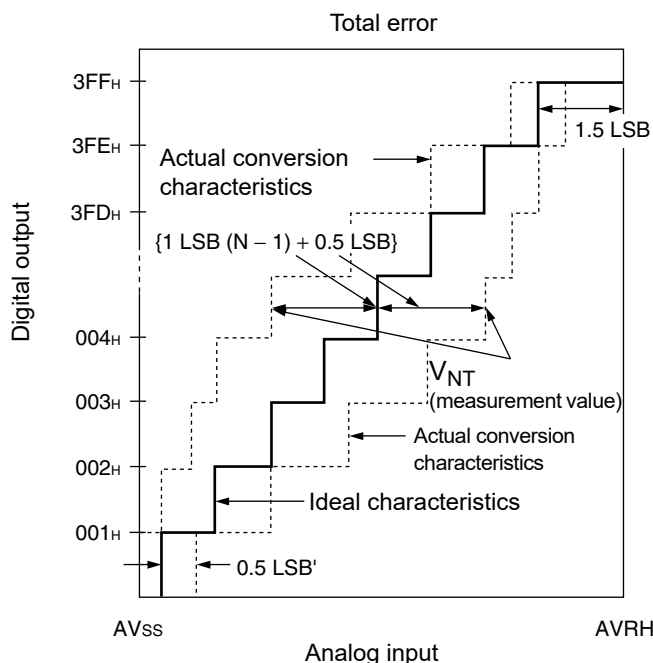
Deviation between actual conversion characteristics and a straight line connecting zero transition point (00 0000 0000 ↔ 00 0000 0001) and full scale transition point (11 1111 1110 ↔ 11 1111 1111).

■ Differential linearity error

Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error/full scale transition error/linearity error.



$$1\text{LSB'} (\text{ideal value}) = \frac{\text{AVRH} - \text{AV}_{\text{SS}}}{1024} [\text{V}]$$

$$\text{Total error of digital output } N = \frac{V_{\text{NT}} - \{1 \text{ LSB'} \times (N - 1) + 0.5 \text{ LSB'}\}}{1 \text{ LSB'}}$$

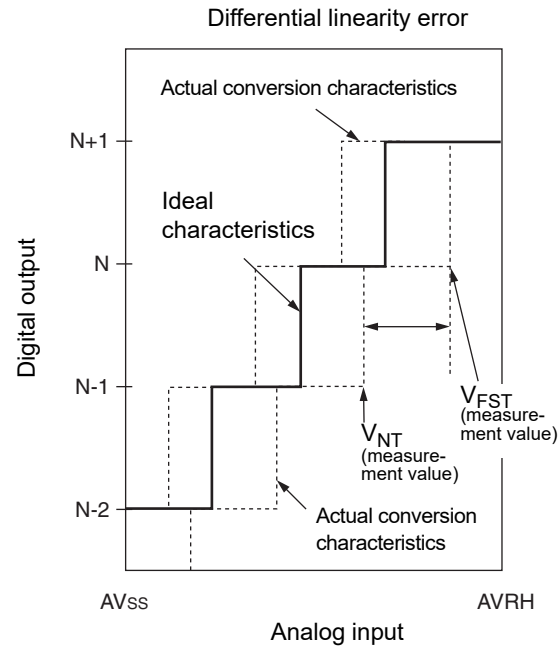
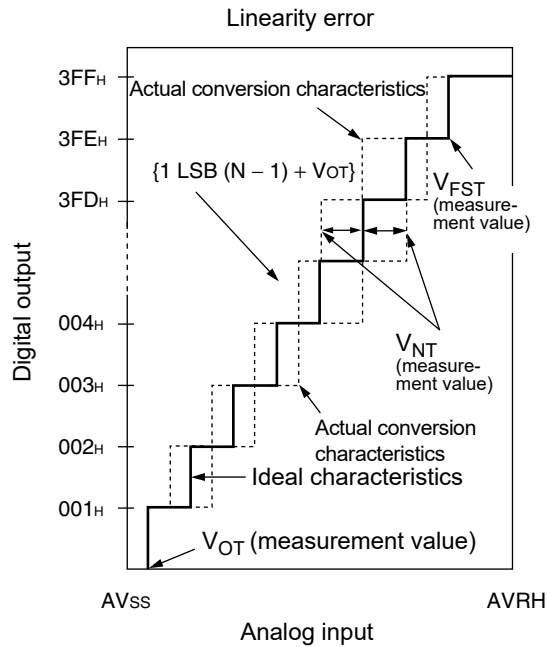
N: A/D converter digital output value

$V_{\text{OT'}}$ (ideal value) = $\text{AV}_{\text{SS}} + 0.5 \text{ LSB'}$ [V]

$V_{\text{FST'}}$ (ideal value) = $\text{AVRH} - 1.5 \text{ LSB'}$ [V]

V_{NT} : A voltage at which digital output transits from $(N + 1)$ to N

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{OT}\}}{1\text{LSB}} [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 [\text{LSB}]$$

$$1\text{LSB} = \frac{V_{FST} - V_{OT}}{1022} [\text{V}]$$

N: A/D converter digital output value

V_{OT} : A voltage at which digital output transits from 000_H to 001_H.

V_{FST} : A voltage at which digital output transits from 3FE_H to 3FF_H.

15.8 Flash Memory Program/Erase Characteristics

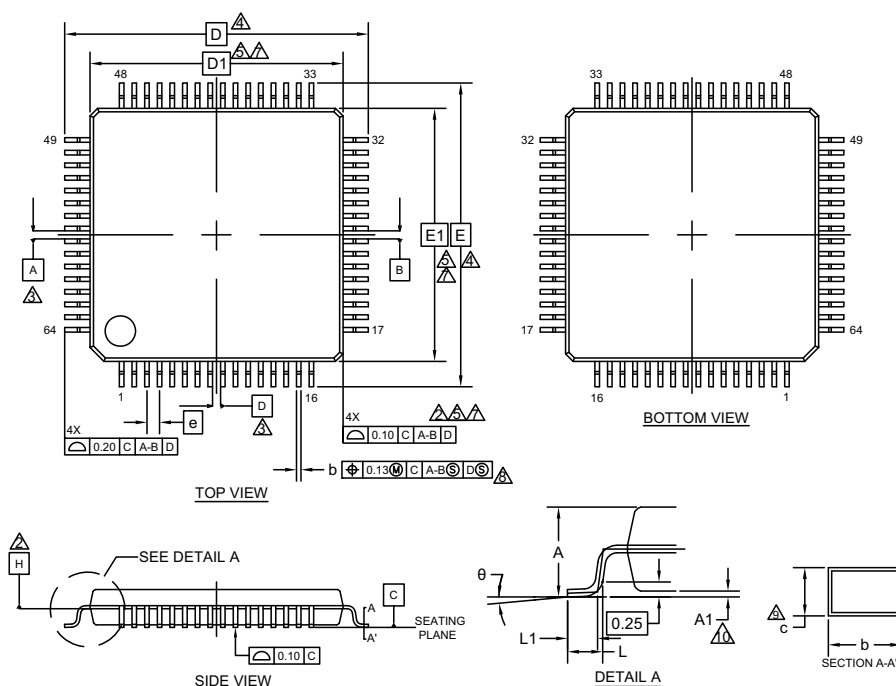
Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	$T_A = +25\text{ }^{\circ}\text{C}$ $V_{CC} = 5.0\text{ V}$	–	0.9	3.6	s	Excludes programming prior to erasure
Chip erase time		–	9	–	s	Excludes programming prior to erasure
Word (16-bit width) programming time		–	23	370	μs	Except for the overhead time of the system level
Program/Erase cycle	–	10000	–	–	cycle	
Flash memory data retention time	Average $T_A = +85\text{ }^{\circ}\text{C}$	20	–	–	year	[1]

1. The value is translated high-temperature measurement results of the technology reliability evaluation into average value at + 85 °C.

16. Ordering Information

Part Number	Package	Remarks
CY91F463NAPMC-GS-UJE1	64-pin plastic LQFP (LQG064)	Lead-free package
CY91F463NCPMC-GS-UJE1	64-pin plastic LQFP (LQG064)	Lead-free package

17. Package Dimension



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.27	0.32	0.37
c	0.09	—	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
- △ DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- △ DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- △ TO BE DETERMINED AT SEATING PLANE C.
- △ DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- △ DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- △ REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- △ DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- △ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- △ A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13881 **

PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

18. Main Changes in This Edition

Spanion Publication Number: **DS07-16607-4E**

Page	Section	Change Results
–	–	Changed the part number. MB91F463NB → MB91F463NC
11	I/O Circuit Type Type J	Corrected “invertor for clock input (Xout)” to “hysteresis type”.
35	Memory Space	Added the sector configuration for MB91F463NC in “3. flash memory sector configuration”.
81	Ordering Information	Changed the part number. MB91F463NBPMC → MB91F463NCPMC-GSE1

NOTE: Please see “Document History” for later revised information.

Page	Section	Change Results
Rev.*B		
-	Marketing Part Numbers changed from an MB prefix to a CY prefix	
2, 6, 77, 78	Features 2. Pin Assignment 16. Ordering Information 17. Package Dimensions	Package description modified to JEDEC description. FPT-64P-M23 → LQG064
77	16. Ordering Information	Revised Marketing Part Numbers as follows: Before) - MB91F463NCPMC-GSE1 After) - CY91F463NCPMC-GS-UJE1 Added Marketing Part Numbers as follows: - CY91F463NAPMC-GS-UJE1

Document History

Document Title: CY91F463NA/F463NC/V460A, FR60, CY91460N Series, 32-bit Microcontroller Datasheet Document Number: 002-04604				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	AKIH	06/29/2009	Migrated to Cypress and assigned document number 002-04604. No change to document contents or format.
*A	5208752	AKIH	04/07/2016	Updated to Cypress template
*B	6168325	WAFA	05/15/2018	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. Features 2. Pin Assignment 16. Ordering Information 17. Package Dimensions For details, please see 18. Main Changes in This Edition.
*C	6550103	ATSE	04/19/2019	Revised the following item; 15.7 Definition of A/D Converter Terms Differential linearity error of digital output N Before) $\{V(N+1)T - VNT\}/1LSB$ After) $\{V(N+1)T - VNT\}/1LSB - 1$

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