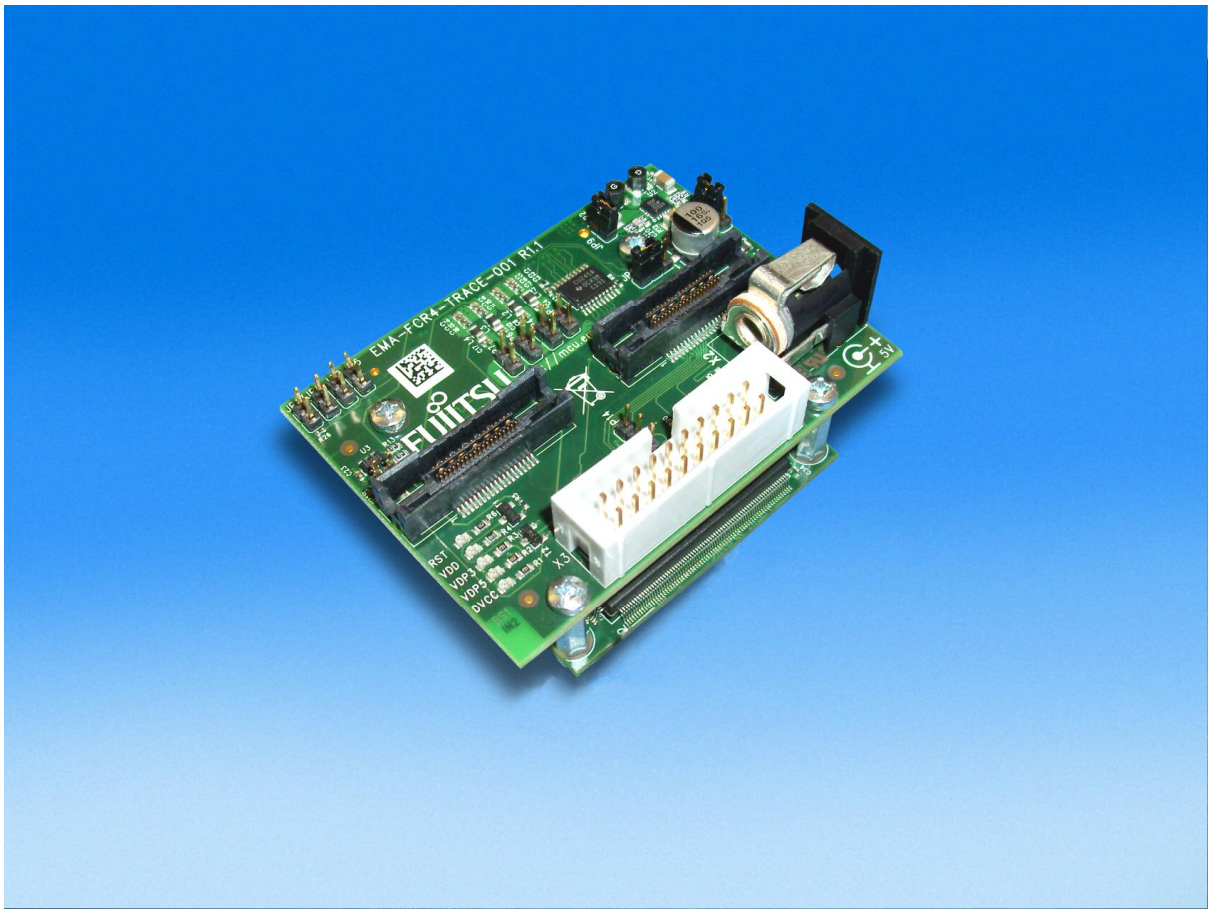
Fujitsu Semiconductor Europe
User Guide

FSEUMCU- UG-9E0013-10

FCR4 FAMILY
FCR4-CLUSTER SERIES
EMULATION BOARD
EMA-MB9DF125-001

USER GUIDE



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Revision History

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Contents

1 Overview

INTRODUCTION TO EMA-MB9DF125 ASSEMBLY

1.1 Abstract

The EMA-MB9DF125 Assembly (‘*Emulator Assembly’* for further reference) consists of two boards stacked-up and pre-mounted.

On top of the CPU emulation board equipped with Fujitsu’s ARM® Cortex™ FCR4 MB9DF125 Atlas-L MCU in a 240 pin trace package (EMA-MB9DF125-001), a trace and power adapter supporting the connection of trace and JTAG debug signals to standard-receptacles for debug-tools is mounted (EMA-FCR4-TRACE-001). Those boards will be hereinafter referred to as ‘*Emulator Board’* and ‘*Trace Board’*.

The Trace Board also provides 3.3V and 1.2V power supply from an external wall-plug adapter to operate the whole stack-up in standalone mode (for usage without a target circuit board, i.e. to allow the designer to start software development immediately prior to having a final target system available) but does not allow powering of a target system.

The centric placed receptacle for the target-board on the bottom side of the Emulator Board is associated with a footer having the footprint of the customer's CPU device for direct interconnection of target board pins; there is also an Extender available which will increase the distance between the Emulation Board and customer’s target board if necessary.

1.2 Features of Trace Board

- 5V regulated external DC power supply input
- On-board 3V3 and 1V2 voltage regulators
- Selectable power supply sources for standalone and target powered operation
- Power supply supervisor and Power-LEDs for all power supply chains, Reset LED
- JTAG Debug connector, In-Circuit Flash programming supported
- Debug from Target available using bus-switch
- Trace Probe connector

1.3 Trace Board Description

The Trace Boards supports Debug and Trace using ARM® Coresight technology for Fujitsu's FCR4 Emulator Boards. Standalone operation of supported Emulator Boards for software development tasks is supported using built-in power supply circuits.

1.3.1 Trace Board top view

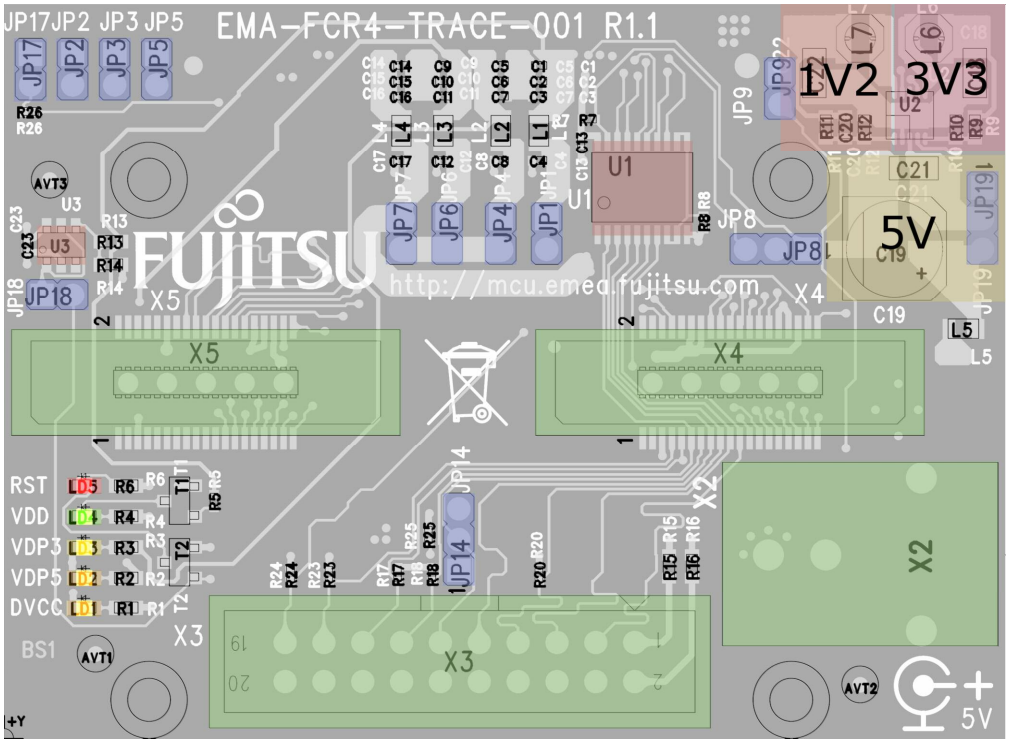


Figure 1-1: Trace Board top view

1.3.2 Power supply circuit

The power supply circuit features a Texas Instruments TPS62420DRC synchronous dual step-down DC-DC converter providing independent 1,2V and 3.3V output voltage rails from a regulated DC input voltage rated +5V.

> The power supply circuit is not intended for powering the target system

Various jumpers allow to adoption to customer's individual requirements and use cases (see next chapter)

1.3.3 Power monitor and reset

A Texas Instruments TPS3106K33DBV supervisory circuit is used to monitor MCU_VDD (1.2V) and 3.3V power supply chains to provide circuit initialization and timing supervision.

A Reset signal is asserted to CPU pin RSTX) on power up and when MCU_VDD drops below a threshold voltage. Reset signal assertion from power supply supervision (PWR_RST) is disabled by leaving jumper JP18 open (set by default) whereas Reset assertion from the target (RSTX) is enabled by default with jumper JP9 bridged. Furthermore Reset is controlled from the JTAG interface connector. LED D5 reflects Reset occurrences.

> Reset from the JTAG and Trace connectors will always trigger the MCU to reset (RSTX) whereas JTAG_NTRST depends on the JTAG interface selected for usage by jumper JP8 (debug from Trace Board or debug from target) in case the target board provides an additional JTAG interface connector .

1.3.4 Debug and trace facilities

The Trace Board supports Debug and Trace using ARM® Coresight technology and standard 20-pin dual row, 2.54mm pitch JTAG interface connector (Samtec HTST-110-01-L-DV, X3) ; utilising 2 MICTOR 38-pin connectors (TYCO 5767054-1, X4 and X5), 4-bit, 8-bit, 16-bit, and 32-bit trace data width is supported.

The JTAG signal lines from the target are shared with the Trace Board JTAG connector using a bus switch (U1) which can be enabled by closing jumper JP8 pin1 and pin 2 (mutually exclusive with the similar bus switch U4 on the Emulator board described next page)

> When using debug functionality from target, trace operation is disabled.

1.4 Features of Emulator Board

- Supports Fujitsu's FCR4 MB9DF125 - Series with 176 pin QFP-176 Package
- 176 pin receptacle corresponding with target-board footer having QFP-176 footprint
- Footer supports emulator header as well as MCU device in QFP-176 package
- 4 MHz main crystal, 32 kHz crystal for sub clock operation
- Bus switch to link target board JTAG interface to MCU

1.5 Emulator Board Description

Using Fujitsu's ARM® Cortex™ MB9DF125 Atlas-L MCU in 240 pin trace package for emulation, the Emulator board is capable of emulating Atlas-L 176 pin series package MCU inside customer's target environment while simultaneously providing trace and debug features using the stacked trace adapter board.

1.5.1 Emulator Board Top View

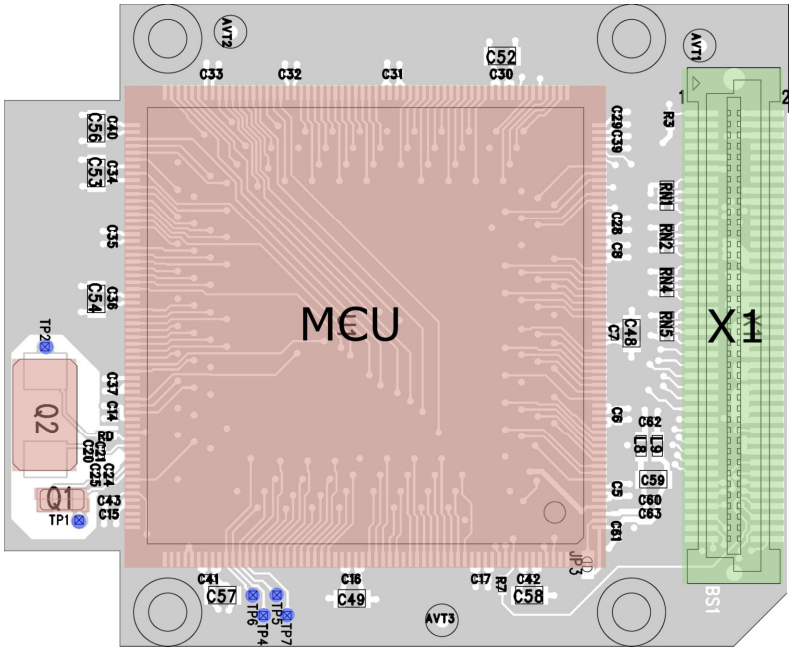


Figure 1-2: Emulator Board top view

1.5.2 Emulator Board Bottom View

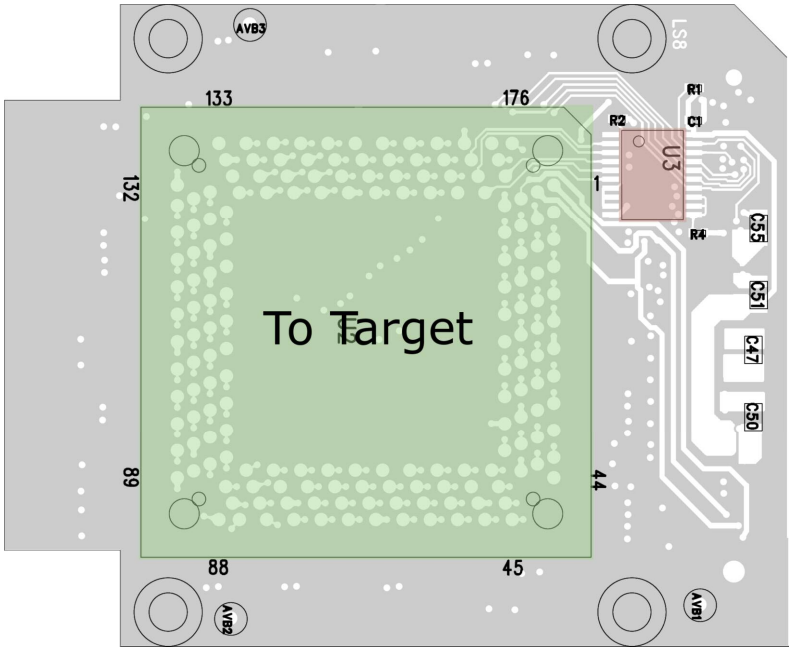


Figure 1-3: Emulator Board bottom view

1.5.3 MCU clocks

The board is supplied with a 4 MHz crystal as main oscillation source. Using the internal PLL of the MCU, internal clock rates up to 128 MHz can be achieved. In addition, an 32.768 kHz Crystal supports sub-clock and Real Time Clock Timer module.

1.5.4 B2B connector

B2B connector X1 connects the Emulator Board with the Trace Board to form the Emulation assembly.

1.5.5 Target header

The centric placed receptacle for the target-board on the bottom side of the Emulator Board is associated with a footer (NQPACK176SD) fitting the footprint of the customer's MCU device (Fujitsu's Cortex™ R4 MB9DF125 - Series with FPT-176P-M07 package)

Footer NQPACK176SD needs to be soldered to the target board for either being populated with the MCU device or direct interconnection of target board pins and Emulator Board; layout guidelines for target board design are described in chapter 6.

An Extender (YQ-SOCKET176SDF-2) allows increase the distance between the Emulation Board and customer's target board if necessary (see chapter 6 'Layout Guidelines for Target Board')

2 Installation

THIS CHAPTER DESCIBES THE INSTALLATION OF THE BOARD

2.1 First Installation

Carefully remove the board assembly from the shipping package. First, check if there are any damages before powering up the evaluation board.

The Trace Board should already be mounted to the Emulator Board. If applicable for your setup, mount the whole Emulator Assembly to your target board (see chapter 6), your target board must not be powered for this step. To ensure right alignment, pin 1 is marked by the cut edge.

Next check the default Jumper settings for the Trace Board which are described in next chapter for either target mode or standalone operation.

When operating the emulator in target mode (default operation), the whole assembly, in particular the Trace Board is powered from the target board, for standalone operation connect the power supply to connector X2, a regulated DC input voltage of 5V is required.

After powering the Emulation Assembly either way, LEDs D1 - D4 should be lit, if the LEDs do not light up, switch off the power supply and check whether polarity and voltage level are appropriate, check as well that the current capability of the DC supply used is sufficient.

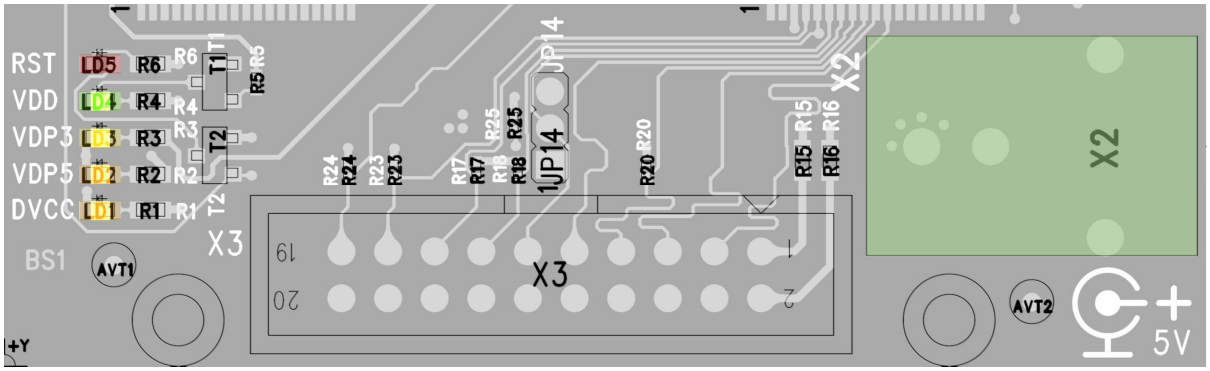


Figure 2-1: Power connector X2 location

The positive voltage (+) must be connected to the central pin, ground (GND) must be connected to shield of the connector X2. LED 4 carries the wrong label and should read ‘VDD’

When operating the emulator in target mode, additional DC power can be applied through X2 to prevent JTAG and trace interfaces to become inoperable when using power-down modes of the MCU. When doing so, carefully check notes on jumper settings (see next chapter).

3 Jumpers and Switches

THIS CHAPTER DESCRIBES ALL JUMPERS THAT CAN BE MODIFIED

3.1 Jumper Locations

The following pictures show the silk plot of the Trace Board with marked default jumper settings for target mode and standalone operation use cases:

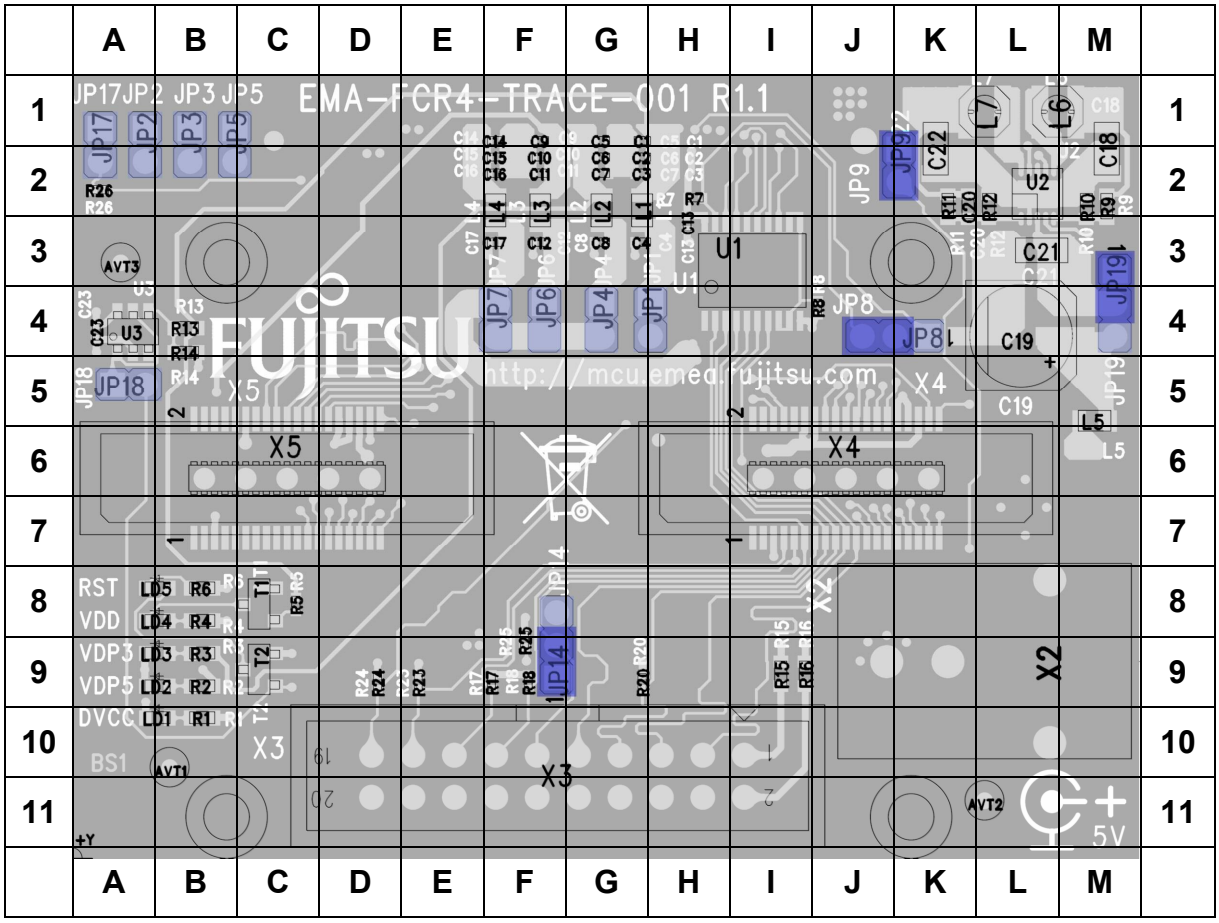


Figure 3-1: Default jumper location and settings (Target Mode)

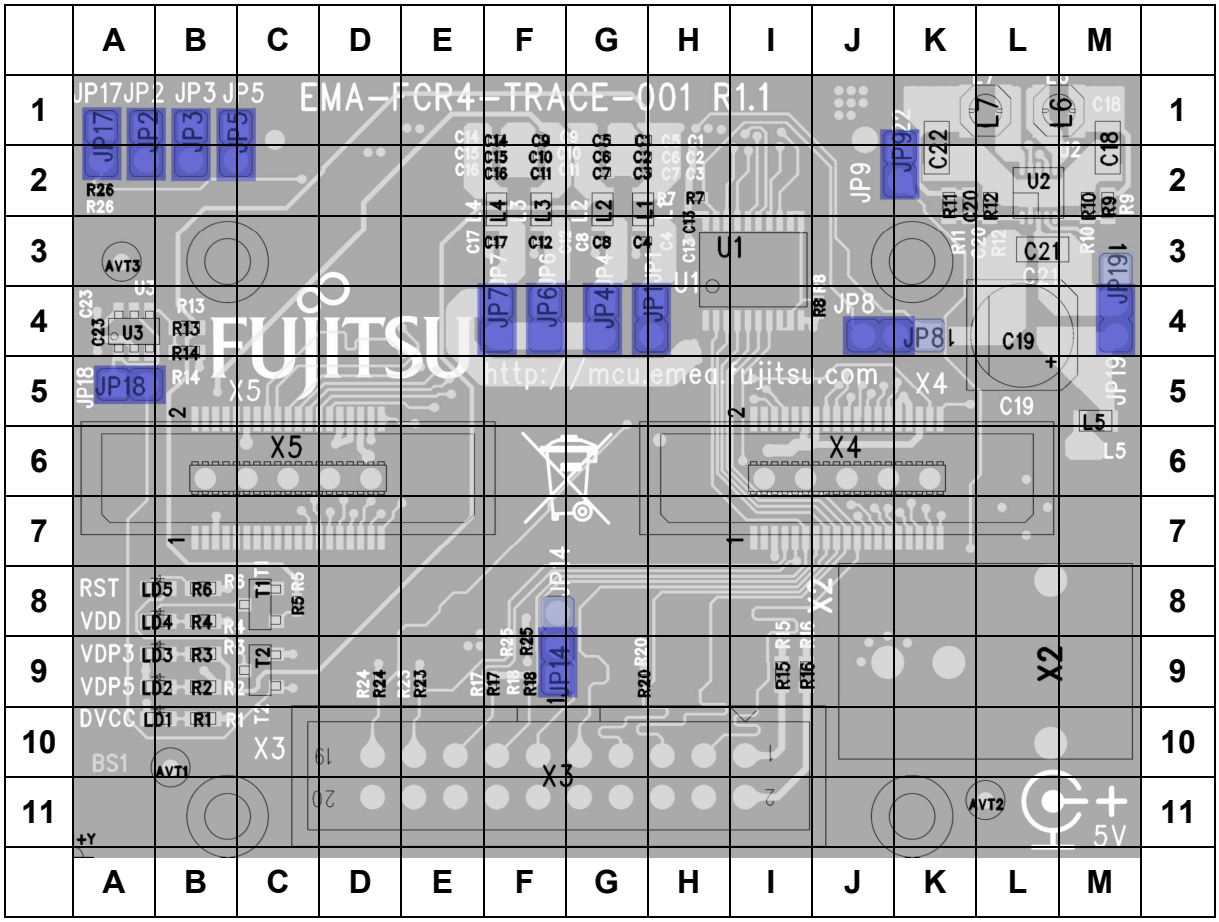


Figure 3-2: Default jumper location and settings (Standalone Mode)

The Emulator Board also carries jumpers (solder bridges populated with 0 Ω resistors) not shown as silk plot picture here nor described in detail further down this chapter. The Emulator Board jumpers might be used to remove VDD from the Trace Board (R6, R8, R9 and R10) for particular use cases. Please consult a Fujitsu application engineer if any modification of solder jumpers is required.

3.2 Default Jumper Settings for Trace Board

The following table lists all jumpers including its default settings and location on the board for target mode (TM) and standalone mode (SM) operation:

Jumper	Description / Function	Type	TM	SM	Coordinates
JP1	Enable 1.2V MCU_VDD supply from Trace Board	2 pin	Open	Closed	H4
JP2	Enable MCU_AVDD5 supply from MCU_VDP5	2 pin	Open	Closed	A1
JP3	Enable MCU_AVRH5 supply from MCU_VDP5	2 pin	Open	Closed	B1
JP4	Enable 3.3V MCU_VDP3 supply from Trace Board	2 pin	Open	Closed	G4
JP5	Enable MCU_AVSS5 supply from GND	2 pin	Open	Closed	B-C1
JP6	Enable 3.3V MCU_DVCC supply from Trace Board	2 pin	Open	Closed	F4
JP7	Enable 3.3V MCU_VDP5 supply from Trace Board	2 pin	Open	Closed	F4
JP8	Debug source select	2 pin	2-3	2-3	J-K4
JP9	Enable reset from target	2 pin	Closed	Closed	K2
JP14	RTCK (Return TCK re-clocked) enable / pull-down	3 pin	1-2	1-2	F9
JP17	Mode select	2 pin	Open	Closed	A1
JP18	Enable reset from power supervisor	2 pin	Open	Closed	A5
JP19	Power source select	3 pin	1-2	2-3	M3-4

Table 3-1: Default jumper settings

3.3 Supply Mode Selection Jumper (JP 17)

The Emulator Assembly will be used related to a target board in most cases (default settings, no external DC power supply required).

The Trace Board also provides 3.3V and 1.2V power supply from an external wall-plug adapter to operate the whole stack-up in standalone mode for usage without a target circuit board. In order to use the Emulator Board either in target or standalone mode, operation mode selection jumper and all power supply jumpers (JP1 - JP7 and JP19, see next section) have to be being set accordingly on the Trace Board (external DC power supply required).

JP17 Selects the operating mode of the Emulator Board. JP17 must be left open when the Emulator Assembly is connected to a target board and to be closed for standalone operation. (Coordinates A1)

Jumper	Setting	Description
JP17 (MODE)	Open	Target Mode
	Closed	Standalone Mode

Table 3-2: Supply mode selection

3.4 Digital Power Supply Jumpers (JP 1, 4, 6, 7, 19)

Emulator Board digital power supply sources for standalone and target powered operation are selectable by the user.

Target Mode: When operating the emulator in target mode (default operation), the whole assembly, in particular the Trace Board is powered from the target board. In General, all digital and analogue (see next paragraph) power supply jumpers JP1 - JP7 as well as just described operating mode selection jumper JP17 have to remain open.

Standalone Mode: For standalone operation the synchronous dual step-down DC-DC converter situated on the Trace Board provides independent 1,2V and 3.3V output voltage rails from a regulated DC input voltage rated +5V to the MCU on the Emulator board and peripherals. In General, all digital and analogue (see next paragraph) power supply jumpers JP1 - JP7 have to be closed (an ampere meter can be used instead for power consumption measurement); jumper closure requirement also applies to the operating mode selection jumper JP17.

> Even though the power regulator is thermally protected against overload, care must be taken when supplying current for additional circuitry. The power supply circuit is not intended for powering the target system

The following picture illustrates the above described general Trace Board settings for target mode (left hand side) and standalone operation (right hand side) of the Emulator board:

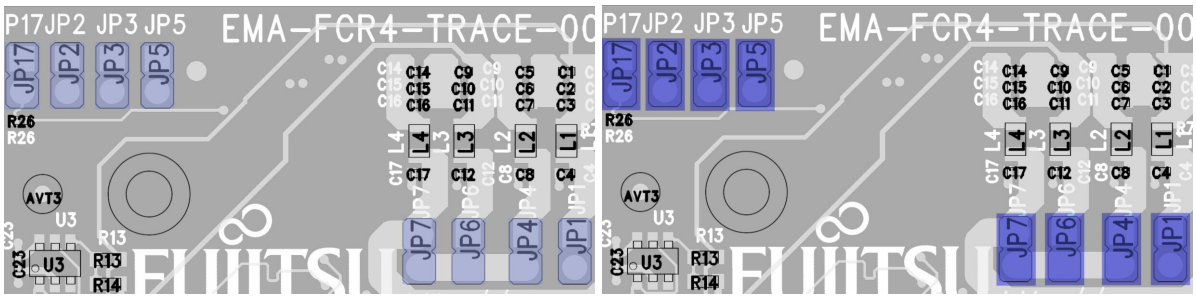


Figure 3-3: Default jumper settings comparison

JP1 Enables Emulator Board 1.2V MCU_VDD core supply from the Trace Board 1.2V power regulator supply chain in standalone operation when closed. If MCU_ VDD is powered from the target JP1 has to be left open. (Coordinates H4)

Emulator Board MCU core voltage MCU_VDD 1.2V domain connects through 4 0R0 bridges (R6, R8, R9 and R10) to its plane. In case customer‘s 1.2V regulator does not provide enough power to the Calypso MCU core supply VDD bridges may be removed and solely Jumper JP1 can be closed to allow powering the MCU core from the Trace Board.

JP4 Enables Emulator Board MCU_VDP3 power domain supply from the Trace Board 3.3V power regulator supply chain in standalone operation when closed.
If MCU_ VDP3 is powered from the target board, JP4 has to be left open.
(Coordinates G4)

JP6 Enables Emulator Board Stepper Motor Driver Voltage MCU_DVCC supply chain from the Trace Board 3.3V power regulator supply chain in standalone operation when closed.
If MCU_ DVCC is powered from the target board, JP6 has to be left open.
(Coordinates F4)

JP7 Enables Emulator Board MCU_VDP5 power domain supply from the Trace Board 1.2V power regulator supply chain in standalone operation when closed.
If MCU_ VDD is powered from the target board, JP7 has to be left open.
(Coordinates F4)

JP19 Selects Trace Board regulated 5V power supply from regulated 5V DC input as power source for standalone operation (2-3 closed) or MCU_VDP5 in target mode operation (1-2 closed) respectively.
(Coordinates M3-4)

When in target mode is selected for JP19 (2-3 closed), jumpers JP1, JP4, JP6 and JP7 must not be closed (except JP1 if all 4 0R0 MCU_VDD bridges R6, R8, R9 and R10 have been removed).

When using target mode VDP5, DVCC, AVCC5 and AVHR5 MCU power domain (for AVCC5 and AVHR5 see description further down) in principle can be operated from 5V or 3.3V power supply chains, when selecting 3.3V for VDP5, care has to been taken about digital input and output voltages.

When operating the Emulator Assembly in standalone mode, VDP5 and DVCC are supplied from the 3.3V power regulator output; AVCC5 and AVHR5 are fed from the same digital VDP5 source as well (as long as analogue power supply voltage jumpers described in next chapters are also closed).

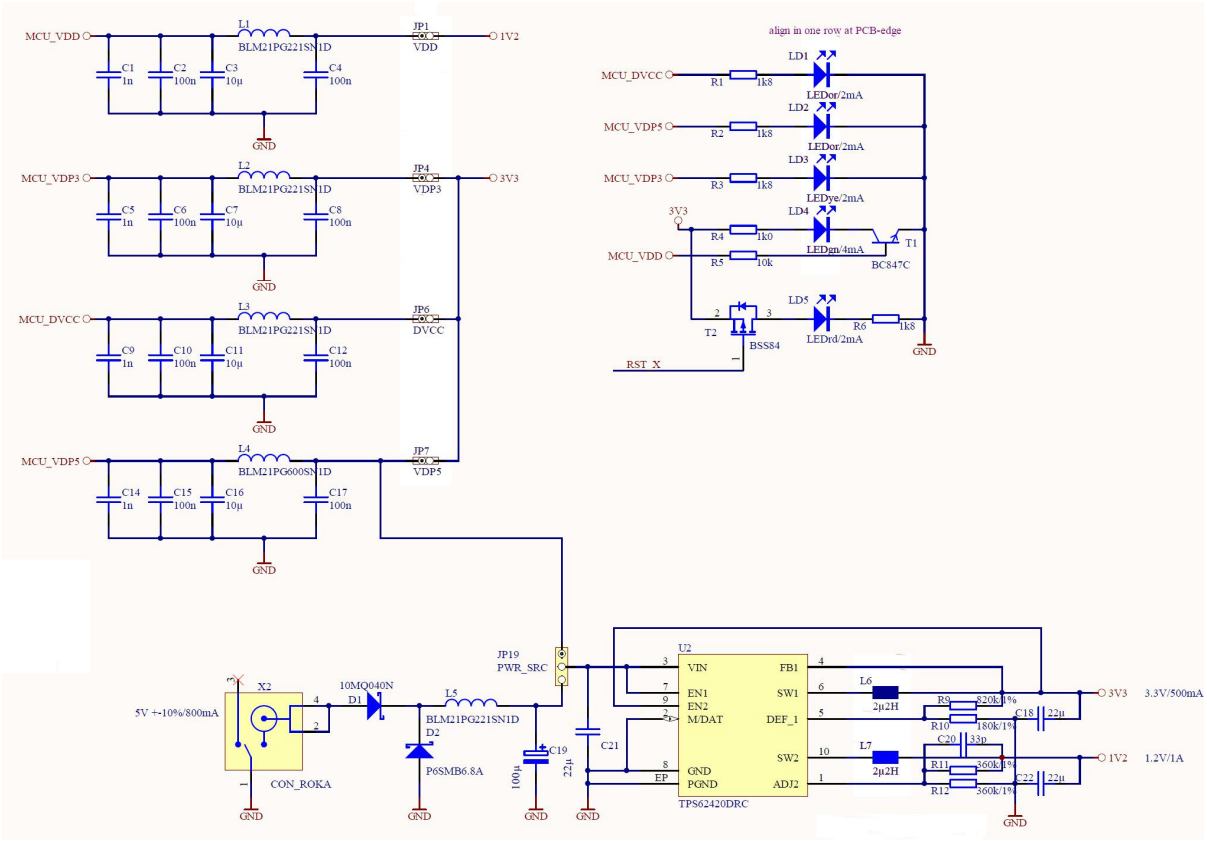


Figure 3-4: Power supply schematics

Jumper	Setting	Description
JP1 (VDD)	Open	MCU_VDD is disconnected from 1V2
	Closed	MCU_VDD is connected to 1V2
JP4 (VDP3)	Open	MCU_VDP3 is disconnected from 3V3
	Closed	MCU_VDP3 is connected to 3V3
JP6 (DVCC)	Open	MCU_DVCC is disconnected from 3V3
	Closed	MCU_DVCC is connected to 3V3
JP7 (VDP5)	Open	MCU_VDP5 is disconnected from 3V3
	Closed	MCU_VDP5 is connected to 3V3
JP19 (PWR_SRC)	1 - 2	Power sourced from target VDP5
	2 - 3	Power sourced from regulated DC 5V input X2

Table 3-3: Power supply configuration

Default settings (target mode) marked grey in table above.

3.5 Analog Power Supply Voltage (JP 2, 3, 5)

Emulator Board analogue power supply sources for standalone and target powered operation are selectable by the user. The power supply as well as the positive reference voltage for the A/D-converter can be provided from the target board (default setting) or from the Trace Board 3.3V digital power supply chain (which also sources MCU_VDP5, MCU_VDP3 and MCU_VDCC). Using separate supply chains for analogue power supply and reference voltage from the target board may result in having less noise.

JP2 Enables Emulator Board analogue supply voltage MCU_AVDD5 power domain supply from MCU_VDP5 digital power domain in standalone operation when closed. If MCU_AVDD5 is powered from the target board, JP2 has to be left open. (Coordinates A1)

JP3 Enables Emulator Board positive reference voltage MCU_AVRH5 power domain supply from MCU_VDP5 digital power domain in standalone operation when closed. If MCU_AVRH5 is powered from the target board, JP2 has to be left open. (Coordinates B1)

JP5 Enables Emulator Board MCU_AVSS5 supply to b e connected to the Trace Board GND layer in standalone operation when closed. If the Emulator Board is supplied from the target, JP5 has to be left open. (Coordinates B-C1)

By default, the A/D-converter supply and reference voltage is the same as the microcontroller supply voltage. AVCC5 and VDP5 must be set to the same voltage. It is required that AVCC5 and AVRH5 do not exceed VDP5 and that the voltage at the analogue inputs does not exceed AVCC5 neither when the power is switched on.

DVCC, AVCC5 and VDP5 must be set to the same voltage during zero point detection (ZPD) on any of the SMC ports. If zero point detection is not required on any of the SMC ports, DVCC can have any value with-in absolute rating, provided switches are disabled).

Jumper	Setting	Description
JP2 (AVDD)	Open	MCU_AVDD5 is disconnected from VDP5
	Closed	MCU_AVDD5 is connected to VDP5
JP2 (AVCC5)	Open	MCU_AVRH5 is disconnected from VDP5
	Closed	MCU_AVRH5 is connected to VDP5
JP3 (AVSS)	Open	AVSS5 is disconnected from GND
	Closed	AVSS5 is connected to GND

Table 3-4: ADC supply and reference

3.6 Reset Generation (JP9, 10)

The MCU can be reset either from the target board, voltage supervisor and JTAG debugger. Using default Jumper settings, all Reset sources mentioned except voltage supervision are enabled for target mode. While a reset signal is asserted the red LED D5 is lit. During normal operation, this LED should be off.

JP9 Enables Reset operation from the target board.
(Coordinates K2)

JP18 Enables Reset operation from the voltage monitor.
(Coordinates A5)

Jumper	Setting	Description
JP9 (T_RST)	Closed	Reset from target board is enabled
	Open	Reset from target board is disabled
JP18 (PWR_RST)	Open	Reset from the voltage supervisor is disabled
	Closed	Reset from the voltage supervisor is enabled

Table 3-5: Reset configuration

3.7 JTAG Interface Configuration (JP 8, 14)

JTAG debugging can be switched from the Trace Board to the target if the target has a JTAG interface is designed in. All other jumpers should be left to the default settings.

JP8 Selects debugging from Trace Board (default 2-3 closed) or target (1-2 closed). Leaving the jumper open will result in having both JTAG ports disabled.
(Coordinates J-K4)

When using target JTAG interface, trace function will not be available.

JP14 Selects JTAG RTCK (Return TCK re-clocked) signal enable or pull-down.
(Coordinates F9)

Jumper	Setting	Description
JP8	2-3	debug from Trace Board
	1-2	debug from Target Board (trace disabled)
JP14 (RTCK-sel)	1-2	RTCK is not used
	2-3	RTCK is used

Table 3-6: JTAG interface configuration

3.8 LED Overview

There are 4 LEDs provided to signal correct 5V 3.3V and 1.2V operation. While a reset signal is asserted the red LED LD5 is lit.

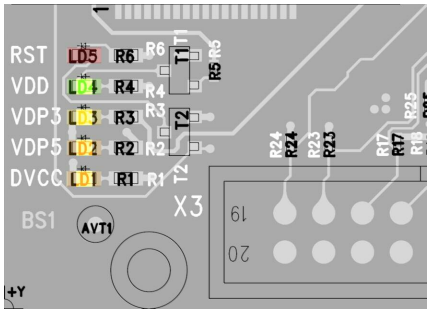


Figure 3-5: LED locations

LED	Colour	Signal	Description / Function	Default
LD1	Orange	MCU_DVCC	3.3V / 5V Power supply ok	ON
LD2	Orange	MCU_VDP5	3.3V / 5V Power supply ok	ON
LD3	Yellow	MCU_VDP3	3.3V Power supply ok	ON
LD4	Green	MCU_VDD	1.2V Power supply ok	ON
LD5	Red	RST_X	Reset active	OFF

Table 3-7: LED function

4 Connectors

THIS CHAPTER DESCRIBES CONNECTOR AND HEADER PIN ASSIGNMENT

4.1 Trace Board Connector Locations

The following pictures show the silk plot of the Trace Board with marked connector locations:

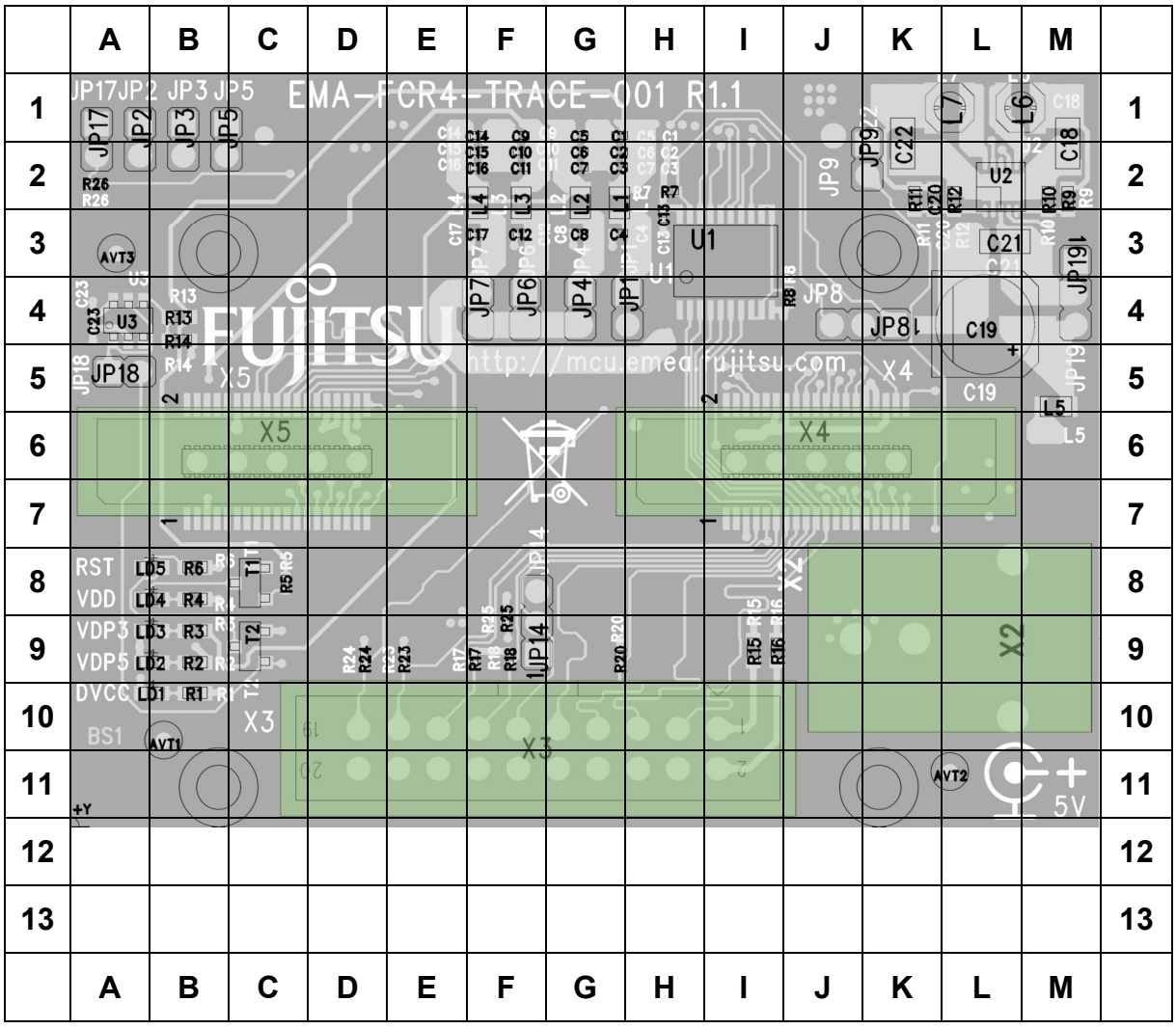


Figure 4-1: Trace Board connector locations

4.2 Connectors available for Trace Board

The following table lists all connectors available:

Header	Description / Function	Type	Direction	Coordinates
X1	B2B connector to Emulator Board (see note)	2 x 40 pin	In/out	Not shown
X2	5V regulated DC power supply	2 pin	power	L9
X3	JTAG connector	20 pin	In/out	F10
X4, X5	Trace connectors	38 pin each	In/out	C6 + J6

Table 4-1: Connectors available for Trace Board

B2B connector X1 connects Trace Board with the Emulator Board connector X1. No further description is delivered as the connector is not to be utilized or modified by the end user.

4.3 Power connector (X2)

The following figure shows the power connection jack X2. This connector is used to connect an external regulated DC power supply voltage (5V DC) to the Trace Board.

Connector X2:

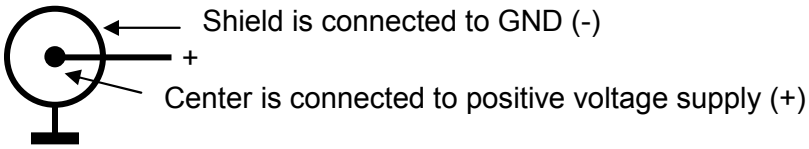


Figure 4-2: Power connector connection scheme

4.4 JTAG Connector (X3)

The JTAG debugging socket on the Trace Board is to be used to debug and program the flash MCU with a special J-LINK adapter. The JTAG reset signal is also available at this connector. Do not use JTAG connector X3 and Trace connectors X4 / X5 in parallel.

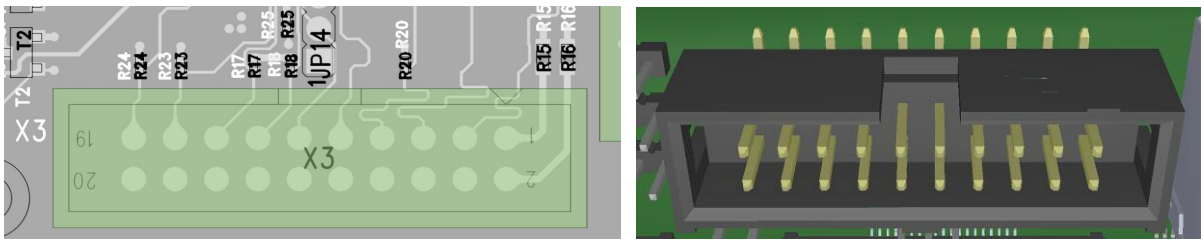


Figure 4-3: JTAG connector X3 location and drawing

Pin Number	Pin Signal	Description	Direction
1	TVsence	Target voltage reference	from target
2	TVcc	Target power	from target
3	nTRST	JTAG TAP Reset, active low	to target
4	GND	Ground	
5	TDI	JTAG Test Data In	to target
6	GND	Ground	
7	TMS	JTAG Test Machine State	to target
8	GND	Ground	
9	TCK	JTAG TAP Clock	to target
10	GND	Ground	
11	RTCK	Return TCK (reclocked)	from target
12	GND	Ground	
13	TDO	JTAG Test Data Out	from target
14	GND	Ground	
15	nRESET	Target reset, active low	bidirectional
16	GND	Ground	
17	DBREQ	Probe Debug Request	to target
18	GND	Ground	
19	TVcc	Probe Debug Acknowledge	from target
20	GND	Ground	

Table 4-2: JTAG connector X3 pin description

4.5 Trace Connectors (X4 and X5)

The Board features a 32-bit Trace Connector (X4 and X5) supporting 4-bit, 8-bit, 16-bit and 32-bit trace data width, the procedures for debug and trace rely on ARM® Coresight technology, additional information regarding debug and trace methodology can be obtained from Coresight TRM provided by ARM® Limited. Signal lines also include JTAG signals on connector J9. Do not use Trace connectors X4 / X5 and JTAG connector X3 simultaneously; connect only one Probe, both connectors are to be used mutually exclusive.

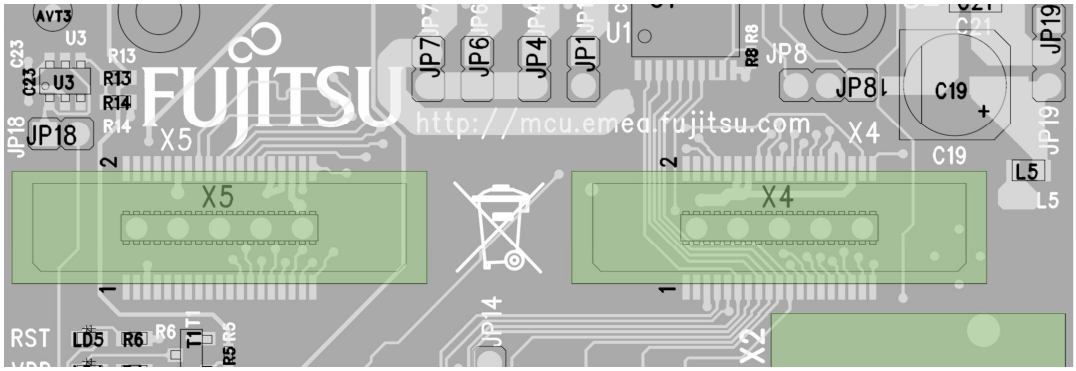


Figure 4-4: Trace connector X4 and X5 locations

Pin Number	Pin Signal	Description	Direction
1-4, 10	NC	No connection	
5, 30, 32	GND	Signal Ground	
14, 34	VSUPPLY	Voltage Supply pin	Not used
12	VTREF	Target debug rail voltage	from target
6	MCU_TRACECLK	Trace Clock pin	from target
7	DBREQ	Probe Debug Request	to target
8	TVcc	Probe Debug Acknowledge	from target
9	nRESET	Target reset, active low	bidirectional
11	TDO	JTAG Test Data Out	from target
13	RTCK	Return TCK (reclocked)	from target
15	TCK	JTAG TAP Clock	to target
16	MCU_TRACE7	Trace data	from target
17	TMS	JTAG Test Machine State	to target
18	MCU_TRACE6	Trace data	from target
19	TDI	JTAG Test Data In	to target
20	MCU_TRACE5	Trace data	from target
21	nTRST	JTAG TAP Reset, active low	to target
22	MCU_TRACE4	Trace data	from target
23	MCU_TRACE15	Trace data	from target
24	MCU_TRACE3	Trace data	from target
25	MCU_TRACE14	Trace data	from target
26	MCU_TRACE2	Trace data	from target
27	MCU_TRACE13	Trace data	from target
28	MCU_TRACE1	Trace data	from target
29	MCU_TRACE12	Trace data	from target
31	MCU_TRACE11	Trace data	from target
33	MCU_TRACE10	Trace data	from target
35	MCU_TRACE9	Trace data	from target
36	MCU_TRACECTL	Trace Control	from target
37	MCU_TRACE8	Trace data	from target
38	MCU_TRACE0	Trace data	from target

Table 4-3: Trace connector X4 pin description

Pin Number	Pin Signal	Description	Direction
1-4, 6-11, 13-15, 17, 19, 21	NC	No connection	
5, 30, 32, 36	GND	Signal Ground	
34	VSUPPLY	Voltage Supply pin	Not used
12	VTREF	Target debug rail voltage	from target
16	MCU_TRACE23	Trace data	from target
18	MCU_TRACE22	Trace data	from target
20	MCU_TRACE21	Trace data	from target
22	MCU_TRACE20	Trace data	from target
23	MCU_TRACE31	Trace data	from target
24	MCU_TRACE19	Trace data	from target
25	MCU_TRACE30	Trace data	from target
26	MCU_TRACE18	Trace data	from target
27	MCU_TRACE29	Trace data	from target
28	MCU_TRACE17	Trace data	from target
29	MCU_TRACE28	Trace data	from target
31	MCU_TRACE27	Trace data	from target
33	MCU_TRACE26	Trace data	from target
35	MCU_TRACE25	Trace data	from target
37	MCU_TRACE24	Trace data	from target
38	MCU_TRACE16	Trace data	from target

Table 4-4: Trace connector X5 pin description

For further information see ARM® architecture and software development tools documentation on the web and documents supplied with your trace tool.

4.6 Emulator Board Connector Locations

The following pictures show the silk plot of the Emulator Board with marked connector locations:

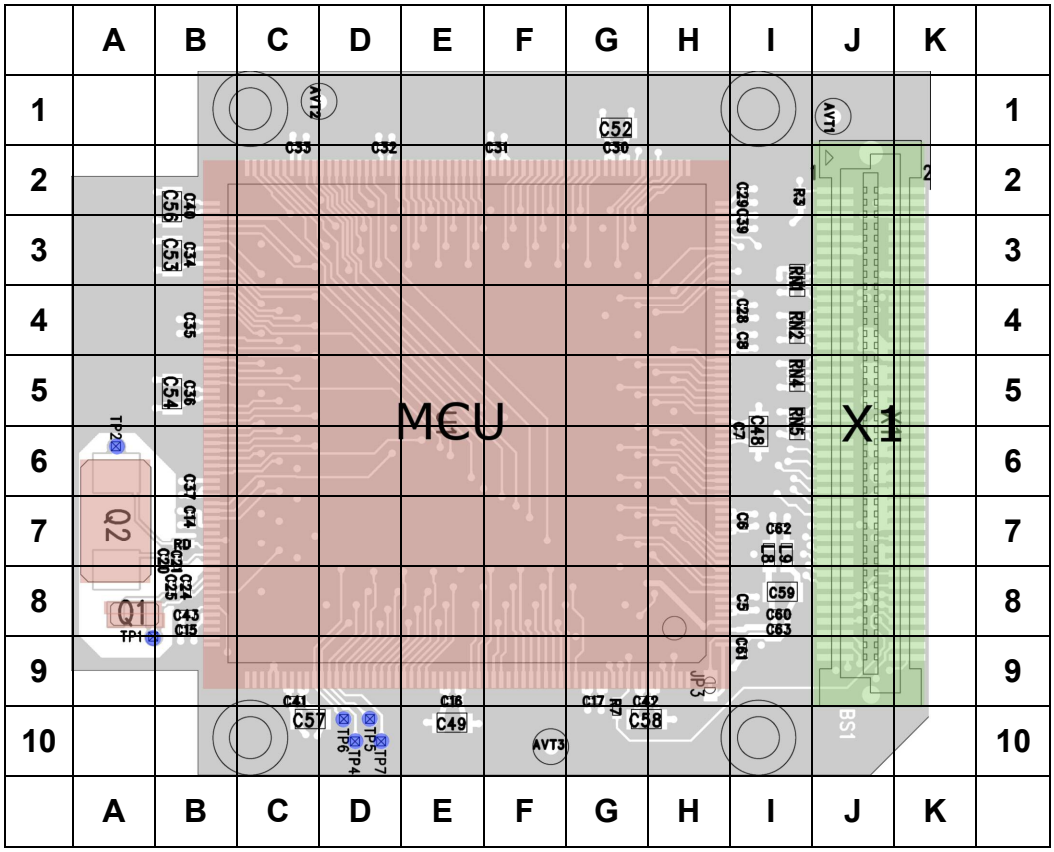


Figure 4-5: Emulator Board connector locations top view

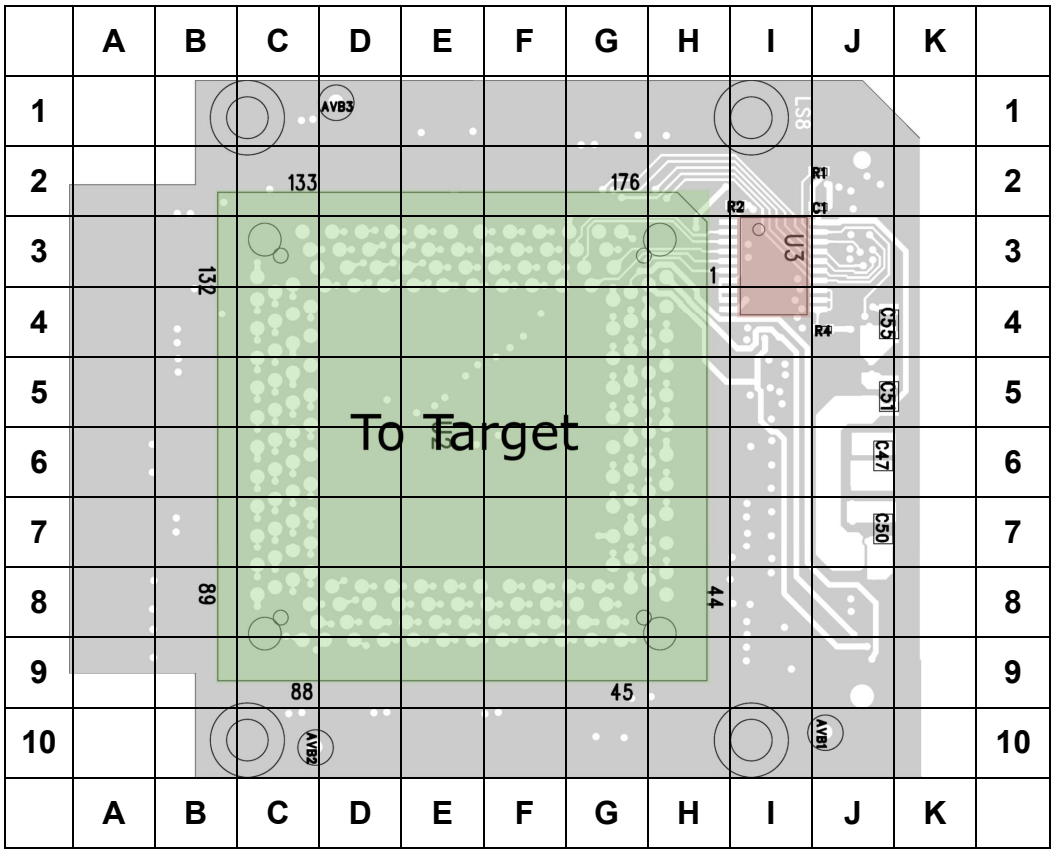


Figure 4-6: Emulator Board connector locations bottom view

4.7 Connectors available for Emulator Board

The following table lists all connectors available:

Header	Description / Function	Type	Direction	Coordinates
X1	B2B connector to Emulator Board (see note)	2 x 40 pin	In/out	Top J2-J9
U2	Target header	176 pin	In/out/power	Bottom F5

Table 4-5: Connectors available for Emulator Board

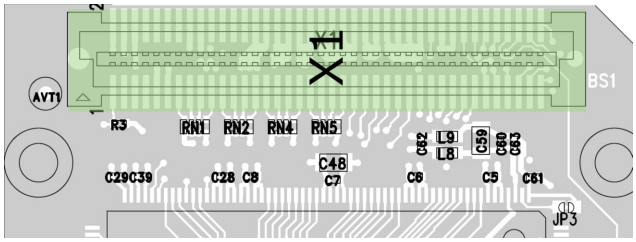


Figure 4-7: Connector X1 location

B2B connector X1 connects Emulator Board with the Trace Board connector X1. No further description is delivered as the connector is not to be utilized or modified by the end user.

4.8 Target Header (U2)

The target header, a receptacle fitting onto the target board's associated footer is placed on the bottom side of the Emulator Board. The footer has the same FPT-176P-M07 footprint as the target MCU and needs to be soldered to the target. When mounting the Emulator Assembly to the target board pin 1 is indicated by a cut edge on the Emulator Board. Firmly, but carefully press the receptacle onto the footer assembly described in chapter 6 following next page.

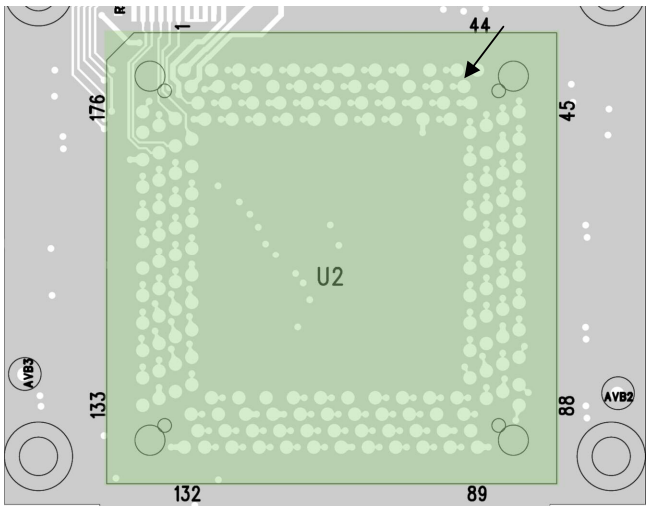


Figure 4-8: Receptacle U5 location

5 Test-points

THIS CHAPTER DESCRIBES TEST-POINTS PIN ASSIGNMENTS

5.1 Test-points available for Emulator Board

The following table lists all Test-Points with their locations on the Emulator Board:

Test-point	Description / Function
TP1	Test-point 4 MHz Main Clock
TP2	Test-point 32.768kHz Sub Clock
TP3	Test-point SYSC_CKOT
TP4	Test-point SYSC_CKOTX
TP5	Test-point RTC_WOT
TP6	Test-point WDG_OBSERVE

Table 5-1: Test-point locations

5.1 Oscillator test-points locations (A6, A8)

Both Oscillator Signals are routed to Test-points TP1 and TP2 (Top-side):

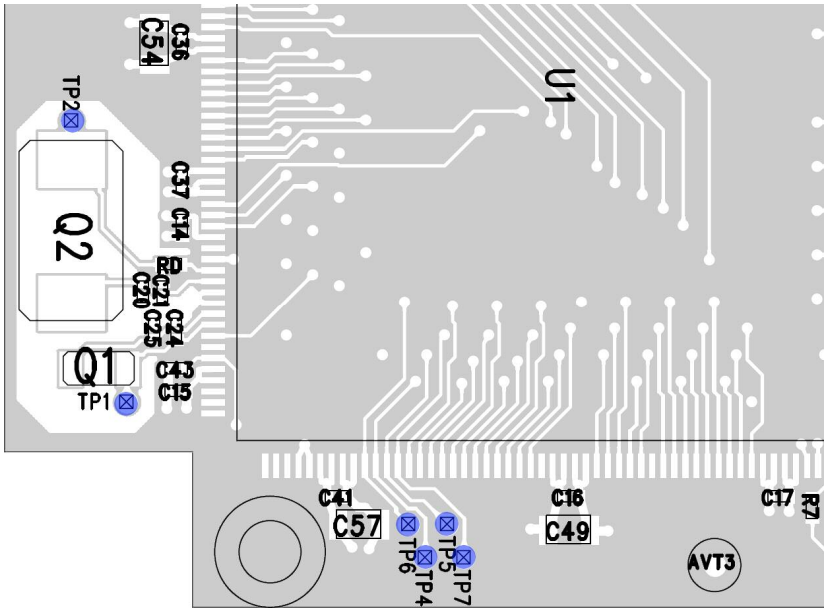


Figure 5-1: Test-point TP1 and TP2 locations

6 Layout Guidelines for Target Board

THIS CHAPTER DESCRIBES LAYOUT GUIDELINES FOR TARGET BOARD DESIGN

6.1 Emulator Assembly Stack-up

Check dimensions indicated in the datasheet available at http://www.tetc.co.jp/e_index.htm to be observed when designing your target board:

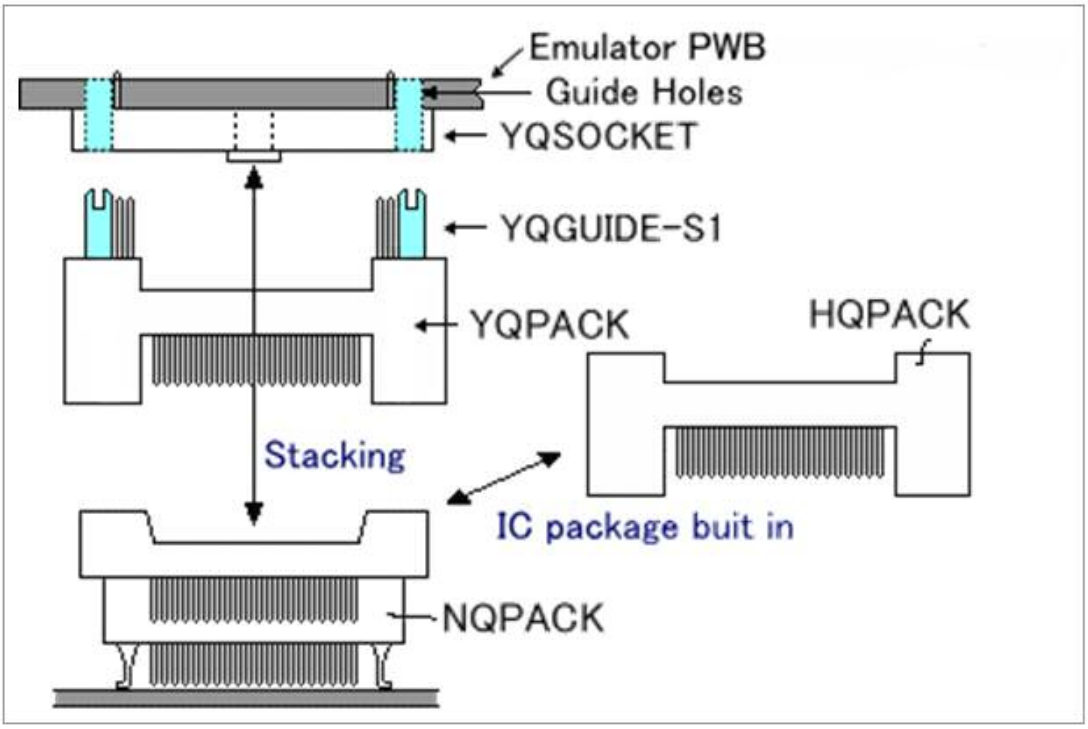


Figure 6-1: Emulator Footer dual use dual use

Footer NQPACK176SD is to be soldered on baseboard (and also available on SK-MB9DF125-002 starter kit) is able to carry either EMA-MBDF125-001 Emulation board with

- YQ-SOCKET176SDF-2 soldered to EMA-MBDF125-001
- YQ-PACK176SD (being part of the delivery) to be fixed to NQPACK176SD using YQGUIDE-S1 (being part of the delivery)

or

- MCU device in 176 pin package using additional HQ-PACK176SD

For the Emulation Board YQ-PACK176SD has to be mounted to the Footer on the baseboard using YQGUIDE-S1 first, second press the Emulator board firmly but carefully onto the footer stackup taking care on orientation of pin 1 (cut edge).

For using an MCU device, see mounting instructions inside SK-MB9DF125-002 user guide:

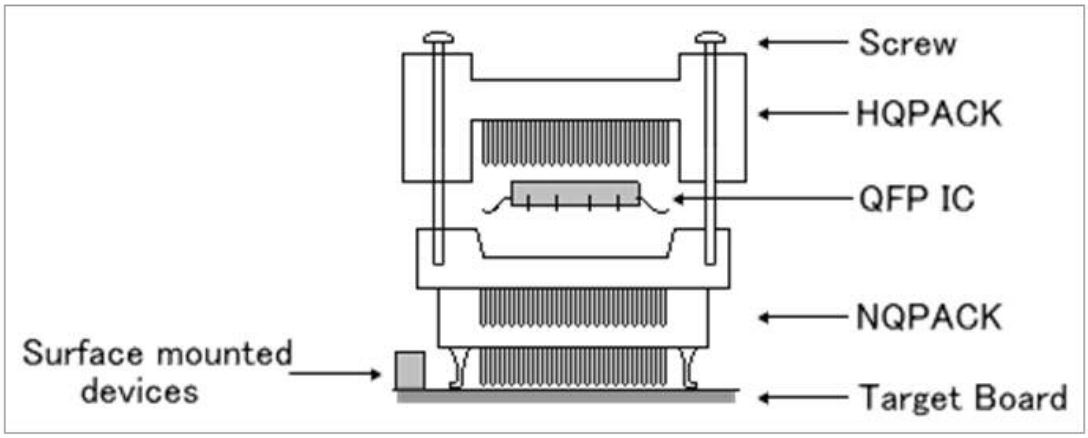
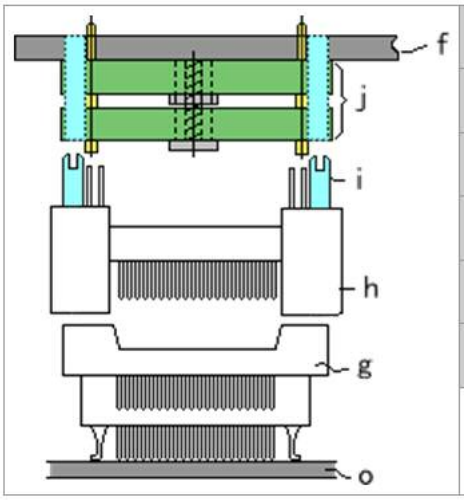


Figure 6-2: Emulator Footer using MCU device

Emulator assembly can be stacked to increase heights of the emulator board_



f	Emulator PWB
g	NQPACK
h	YQPACK
i	YQGUIDE
j	YQSOCKET-F2 type
o	Target PWB

*YQSOCKET-F2 is provided with four YQGUIDE pins.

Figure 6-3: Emulator Assembly Stack-up

6.2 Target Board Recommendations

Power requirements the Emulator Assembly have to be met. In addition to the target board requirements, at least 1A for VDD (1.2V) and 500mA for VDP3, VDP5 and DVDD should be available. All Power pins should be used not only to compensate for target headers contact resistances.

No extensive filtering is done on the Emulator Board with the exception of analogue supply voltages AVDD5, AVSS5 and AVRH5, Filters must be provided on the target board.

7 Getting Started

THIS CHAPTER DESCRIBES HOW TO GET STARTED

.

8 Trouble shooting

THIS CHAPTER DESCRIBES ANY KNOWN PROBLEMS

9 Related Products

NQPACK176SD	Footer for target board
YQ-SOCKET176SDF-2	Extender to footer
SK-MB9DF-125-001	Atlas-L MCU starter kit board with 240 pin trace chip
SK-MB9DF-125-002	Atlas-L MCU starter kit board with NQPACK176SD
ADA-FCR4-MULTIIO-001	Base board for using of MCU board with several IO interfaces like CAN, LIN, Media-LB, Ethernet, Video and Audio accessing
ADA-FCR4-CLUSTER-001	Cluster board to demonstrate using of pointer instruments, dial and pointer illumination, as also TFT display

10 Appendix

10.1 Tables

10.2 Figures

11 Information in the WWW

Information about FUJITSU SEMICODUCTOR Products
can be found on the following Internet pages:

Microcontrollers (8-, 16- and 32bit), Graphics Controllers
Datasheets and Hardware Manuals, Support Tools (Hard- and Software)

http://mcu.emea.fujitsu.com/

Power Management Products

http://www.fujitsu.com/emea/services/microelectronics/powerman/index.html

Media Products: SAW filters, acoustic resonators and VCOs

http://www.yuden.co.jp/us/product/device/device00.html

For more information about FUJITSU MICROELECTRONICS

http://emea.fujitsu.com/semiconductor

Information about the peripheral devices used on the starter kit can be found on the following Internet pages:

- ARM® architecture and software development tools

  http://infocenter.arm.com

- Footer

  http://www.tetc.co.jp/e_index.htm

12 EU-Konformitätserklärung / EU declaration of conformity

Hiermit erklären wir,

Fujitsu Semiconductor Europe GmbH, Pittlerstrasse 47, 63225 Langen, Germany

dass dieses Board aufgrund seiner Konzipierung und Bauart sowie in den von uns in Verkehr gebrachten Ausführung(en) den grundlegenden Anforderungen der EU-Richtlinie 2004/108/EC „Elektromagnetische Verträglichkeit“ entspricht. Durch eine Veränderung des Boards (Hard- und/ oder Software) verliert diese Erklärung ihre Gültigkeit!

We,

Fujitsu Semiconductor Europe GmbH, Pittlerstrasse 47, 63225 Langen, Germany

hereby declare that the design, construction and description circulated by us of this board complies with the appropriate basic requirements according to the EU Guideline 2004/108/EC entitled ’Electro-Magnetic Compatibility’. Any changes to the equipment (hardware and/ or software) will render this declaration invalid!

Note:

All data and power supply lines connected to this starter kit should be kept as short as possible, with a maximum allowable length of 3m. Shielded cables should be used for data lines. As a rule of thumb, the cable length used when connecting external circuitry to the MCU pin header connectors for example should be less than 20cm. Longer cables may affect EMC performance and cause radio interference.

This evaluation board is a **Class A** product according to EN61326-1. It is intended to be used only in a laboratory environment and might cause radio interference when used in residential areas. In this case, the user must take appropriate measures to control and limit electromagnetic interference.

13 China-RoHS regulation

This board is compliant with China RoHS.

14 Recycling

Gültig für EU-Länder:

Gemäß der Europäischen WEEE-Richtlinie und deren Umsetzung in landesspezifische Gesetze nehmen wir dieses Gerät wieder zurück.

Zur Entsorgung schicken Sie das Gerät bitte an die folgende Adresse:

Fujitsu Microelectronics Europe GmbH

Warehouse/Disposal

Monzastraße 4a

D-63225 Langen

Valid for European Union Countries:

According to the European WEEE-Directive and its implementation into national laws we take this device back.

For disposal please send the device to the following address:

Fujitsu Microelectronics Europe GmbH

Warehouse/Disposal

Monzastraße 4a

D-63225 Langen

GERMANY

-- END --