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Errata

This errata sheet is for MB95330H Series Hardware Manual Rev. 1 (CM26-10126-1E).

F²MC-8FX
8-BIT MICROCONTROLLER
MB95330H Series
HARDWARE MANUAL

2012.05.11

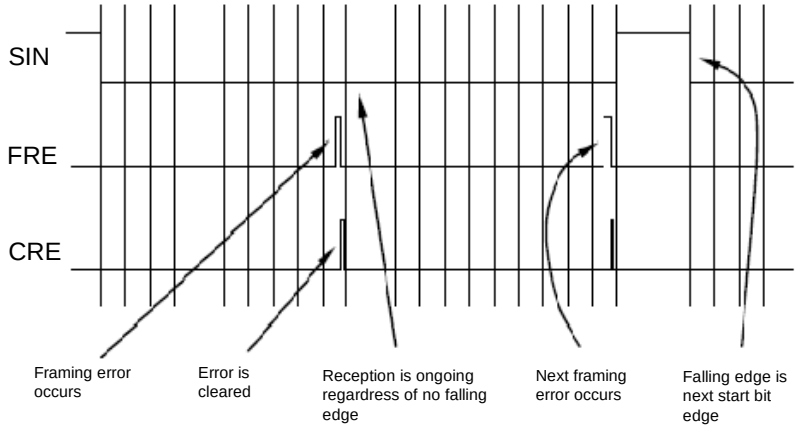
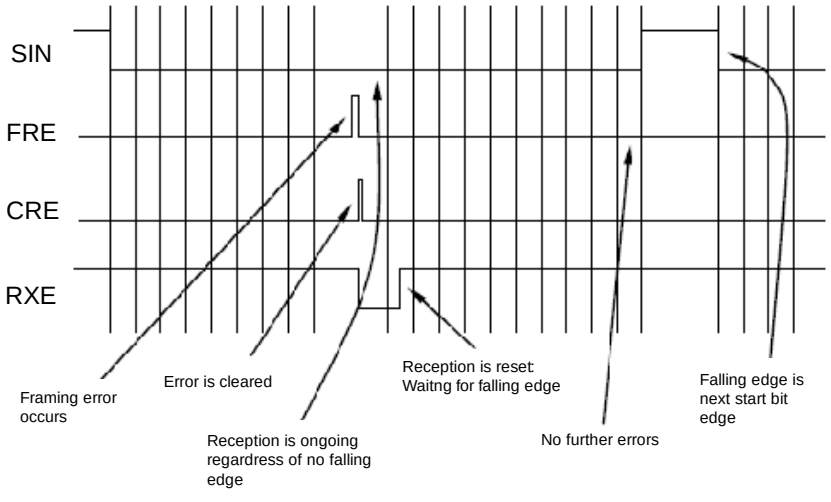
<table>
<tr><th>Date</th><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>2012/
05/11</td><td>82</td><td>6.12</td><td>
"Table 6.12-1 Count Clock Sources Generated by Prescaler" should be corrected as indicated by the shading below.

(Error)
Table 6.12-1 Count Clock Sources Generated by Prescaler
<table>
<tr><th>Count clock source frequency</th><th colspan="2">Frequency
(F_{CH} = 10 MHz,
MCLK = 10 MHz)</th><th colspan="2">Frequency
(F_{CH} = 16 MHz,
MCLK = 16 MHz)</th><th colspan="2">Frequency
(F_{CH} = 16.25 MHz,
MCLK = 16.25 MHz)</th></tr>
<tr><td>MCLK/2</td><td>MCLK/2</td><td>(5 MHz)</td><td>MCLK/2</td><td>(8 MHz)</td><td>MCLK/2</td><td>(8.125 MHz)</td></tr>
<tr><td>MCLK/4</td><td>MCLK/4</td><td>(2.5 MHz)</td><td>MCLK/4</td><td>(4 MHz)</td><td>MCLK/4</td><td>(4.0625 MHz)</td></tr>
<tr><td>MCLK/8</td><td>MCLK/8</td><td>(1.25 MHz)</td><td>MCLK/8</td><td>(2 MHz)</td><td>MCLK/8</td><td>(2.0313 MHz)</td></tr>
<tr><td>MCLK/16</td><td>MCLK/16</td><td>(0.625 MHz)</td><td>MCLK/16</td><td>(1 MHz)</td><td>MCLK/16</td><td>(1.0156 MHz)</td></tr>
<tr><td>MCLK/32</td><td>MCLK/32</td><td>(0.3125 MHz)</td><td>MCLK/32</td><td>(0.5 MHz)</td><td>MCLK/32</td><td>(0.5078 MHz)</td></tr>
<tr><td>$F_{CH}/2^7$</td><td>$F_{CH}/2^7$</td><td>(78 kHz)</td><td>$F_{CH}/2^7$</td><td>(125 kHz)</td><td>$F_{CH}/2^7$</td><td>(127 kHz)</td></tr>
<tr><td>$F_{CH}/2^8$</td><td>$F_{CH}/2^8$</td><td>(39 kHz)</td><td>$F_{CH}/2^8$</td><td>(62.5 kHz)</td><td>$F_{CH}/2^8$</td><td>(63.5 kHz)</td></tr>
</table>
(Correct)
Table 6.12-1 Count Clock Sources Generated by Prescaler (F_{CH})
<table>
<tr><th>Count clock source frequency</th><th>Frequency
(F_{CH} = 20 MHz,
MCLK = 10 MHz)</th><th>Frequency
(F_{CH} = 32 MHz,
MCLK = 16 MHz)</th><th>Frequency
(F_{CH} = 32.5 MHz,
MCLK = 16.25 MHz)</th></tr>
<tr><td>MCLK/2</td><td>5 MHz</td><td>8 MHz</td><td>8.125 MHz</td></tr>
<tr><td>MCLK/4</td><td>2.5 MHz</td><td>4 MHz</td><td>4.0625 MHz</td></tr>
<tr><td>MCLK/8</td><td>1.25 MHz</td><td>2 MHz</td><td>2.0313 MHz</td></tr>
<tr><td>MCLK/16</td><td>0.625 MHz</td><td>1 MHz</td><td>1.0156 MHz</td></tr>
<tr><td>MCLK/32</td><td>0.3125 MHz</td><td>0.5 MHz</td><td>0.5078 MHz</td></tr>
<tr><td>$F_{CH}/2^7$</td><td>156.25 kHz</td><td>250 kHz</td><td>253.9 kHz</td></tr>
<tr><td>$F_{CH}/2^8$</td><td>78.125 kHz</td><td>125 kHz</td><td>126.95 kHz</td></tr>
</table>
</td></tr>
<tr><td>2012/
05/11</td><td>82</td><td>6.12</td><td>
"Table 6.12-2 Count Clock Sources Generated by Prescaler (F_{CRH})" should be added after "Table 6.12-1 Count Clock Sources Generated by Prescaler (F_{CH})".

<table>
<tr><th>Count clock source frequency</th><th>Frequency
(F_{CRH} = 1 MHz,
MCLK = 1 MHz)</th><th>Frequency
(F_{CRH} = 8 MHz,
MCLK = 8 MHz)</th><th>Frequency
(F_{CRH} = 10 MHz,
MCLK = 10 MHz)</th><th>Frequency
(F_{CRH} = 12.5 MHz,
MCLK = 12.5 MHz)</th></tr>
<tr><td>MCLK/2</td><td>500 kHz</td><td>4 MHz</td><td>5 MHz</td><td>6.25 MHz</td></tr>
<tr><td>MCLK/4</td><td>250 kHz</td><td>2 MHz</td><td>2.5 MHz</td><td>3.125 MHz</td></tr>
<tr><td>MCLK/8</td><td>1.25 kHz</td><td>1 MHz</td><td>1.25 MHz</td><td>1.5625 MHz</td></tr>
<tr><td>MCLK/16</td><td>62.5 kHz</td><td>0.5 MHz</td><td>0.625 MHz</td><td>0.78125 MHz</td></tr>
<tr><td>MCLK/32</td><td>31.25 kHz</td><td>0.25 MHz</td><td>0.3125 MHz</td><td>0.390625 MHz</td></tr>
<tr><td>$F_{CRH}/2^6$</td><td>15.625 kHz</td><td>125 kHz</td><td>156.25 kHz</td><td>195.3125 kHz</td></tr>
<tr><td>$F_{CRH}/2^7$</td><td>7.8125 kHz</td><td>62.5 kHz</td><td>78.125 kHz</td><td>97.65625 kHz</td></tr>
</table>
</td></tr>
<tr><td>2012/
05/11</td><td>209</td><td>14.5.1</td><td>
The following statement should be added to details of the function of the IFE bit in "Table 14.5-1 Functions of Bits in 8/16-bit Composite Timer 00/01 Status Control Register 0 (T00CR0/T01CR0)".

During timer operation (T00CR1/T01CR1:STA = 1), the write access to this bit has no effect on operation. Ensure that the timer has stopped before modifying this bit.
</td></tr>
</table>

Date	Page	Section	Description
2012/ 05/11	212	14.5.2	The following statement should be added to details of the function of the IFE bit in “Table 14.5-2 Functions of Bits in 8/16-bit Composite Timer 10/11 Status Control Register 0 (T10CR0/T11CR0)”. During timer operation (T10CR1/T11CR1:STA = 1), the write access to this bit has no effect on operation. Ensure that the timer has stopped before modifying this bit.
2012/ 05/11	313	17.4.5	The following statements should be added to details of the function of the SCES bit in “Table 17.4-4 Functions of Bits in LIN-UART Extended Status Control Register (ESCR)”. With this bit set to "1", executing a software reset is prohibited. Disable reception and transmission before modifying this bit.
2012/ 05/11	318	17.5	The note after “■ Receive Interrupt” should be deleted.
2012/ 05/11	355	17.8	In “■ Notes on Using LIN-UART”, the following content in “● Modifying operation settings” should be corrected as indicated by the shading below. (Error) After modifying operation settings such as the addition of start/stop and changing the data format, reset the LIN-UART. Even though the setting of the LIN-UART serial mode register (SMR) and the resetting of the LIN-UART (SMR:UPCL = 1) are executed simultaneously, that does not ensure that the operation settings are correct. Therefore, after setting the LIN-UART serial mode register (SMR), reset the LIN-UART again. (Correct) With the sampling clock edge select bit (ESCR:SCES) set to "0", before modifying any of the bits listed below, disable reception and transmission. After modifying them, reset the LINUART with a software reset. · Serial control register (SCR) Parity enable bit (PEN), stop bit length select bit (SBL), data length select bit (CL) · Serial mode register (SMR) Operating mode select bits (MD[1:0]) · Extended status control register (ESCR) Continuous clock output enable bit (CCO) · Extended communication control register (ECCR) Serial clock transmission/reception side select bit (MS), serial clock delay enable bit (SCDE), start/stop bits mode enable bit (SSM) To reset the LIN-UART with a software reset (SMR:UPCL = 1), finish modifying the settings of the SMR register first, and then access the register again. In the case of not following the above procedure to modify operating settings, proper operations of this device cannot be guaranteed. Though the transmission bit length of the LIN break field is variable, the detection bit length of the LIN break field is fixed at 11 bits.
2012/ 05/11	355	17.8	In “■ Notes on Using LIN-UART”, a new section “● Modifying sampling clock edge select bit (ESCR:SCES)” should be added after “● Modifying operation settings”. ● Modifying sampling clock edge select bit (ESCR:SCES) With the SCES bit set to "1", executing the LIN-UART software reset is prohibited. · To modify the SCES bit from "0" to "1" Disable reception and transmission, executing a LIN-UART software reset (SMR:UPCL = 1), then modify the SCES bit from "0" to "1". · To modify the SCES bit from "1" to "0" Disable reception and transmission, modify the SCES bit from "1" to "0", then executing a LIN-UART software reset (SMR:UPCL = 1).

Date	Page	Section	Description
2012/ 05/11	356	17.8	In "■ Notes on Using LIN-UART", a new section "● Handling framing errors" should be added after "● Synch break detection". ● Handling framing errors If a framing error occurs (stop bit: SIN = "0") and the next start bit (SIN = "0") immediately follows it, this start bit is recognized regardless of a falling edge for the start bit and reception is started. This sequence is used for detecting the continuous "L" state of the serial data input (SIN) when the next framing error is detected while the data stream is synchronized (See "When reception is always enabled (RXE=1)" in Figure 17.8-1). If this operation is not necessary, disable data reception temporarily after receiving a framing error (RXE = 1→0→1). Therefore, the falling edge of the serial data input (SIN) is detected, the start bit is recognized when "L" is detected at the reception sampling point, and the reception is started (See "When reception is temporarily disabled (RXE=1→0→1)" in Figure 17.8-1).
2012/ 05/11	356	17.8	The following diagram should be added as "Figure 17.8-1 UART Dominant Bus Operation" in "● Handling framing errors". When reception is always enabled (RXE=1)  When reception is temporarily disabled (RXE=1→ 0 → 1) 

<table>
<tr><th>Date</th><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>2012/
05/11</td><td>474</td><td>23.5.1</td><td>In “Figure 23.5-2 16-bit Reload Timer Control Status Register Upper (TMCSRH1)”, the count clock settings of the count clock select bits (CSL[2:0]) should be corrected as indicated by the shading below.

(Error)
<table>
<tr><th rowspan="2">CSL2</th><th rowspan="2">CSL1</th><th rowspan="2">CSL0</th><th colspan="2">Count clock select bits</th></tr>
<tr><th>Operation mode</th><th>Count clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">Internal clock</td><td>MCLK/2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MCLK/4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MCLK/8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MCLK/16</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MCLK/32</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>$F_{CH}/2^7$</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>$F_{CH}/2^8$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Event count</td><td>TI1 pin</td></tr>
</table>
(Correct)
<table>
<tr><th rowspan="2">CSL2</th><th rowspan="2">CSL1</th><th rowspan="2">CSL0</th><th colspan="2">Count clock select bits</th></tr>
<tr><th>Operation mode</th><th>Count clock</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td rowspan="8">Internal clock</td><td>1 MCLK</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>MCLK/2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>MCLK/4</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>MCLK/8</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MCLK/16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MCLK/32</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MCLK/64 or $F_{CH}/2^7$</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Event count</td><td>TI1 pin</td></tr>
</table></td></tr>
<tr><td>2012/
05/11</td><td>729</td><td>31.2</td><td>In “Figure 31.2-1 System Configuration Register (SYSC)”, details of the PGSEL bit should be corrected as indicated by the shading below.

(Error)
<table>
<tr><td>PGSEL</td><td>PG1/PG0 function select bit</td></tr>
<tr><td>0</td><td>Selects the PG1/PG0 pins as subclock oscillator pins.</td></tr>
<tr><td>1</td><td>Selects the PG1/PG0 pins as general-purpose I/O ports.</td></tr>
</table>
(Correct)
<table>
<tr><td>PGSEL</td><td>PG1/PG2 function select bit</td></tr>
<tr><td>0</td><td>Selects the PG1/PG2 pins as subclock oscillator pins.</td></tr>
<tr><td>1</td><td>Selects the PG1/PG2 pins as general-purpose I/O ports.</td></tr>
</table></td></tr>
<tr><td>2012/
05/11</td><td>730</td><td>31.2</td><td>In “Table 31.2-1 Functions of Bits in SYSC Register”, the name of the PGSEL bit should be corrected as indicated by the shading below.

(Error)
PG1/PG0 function select bit

(Correct)
PG1/PG2 function select bit</td></tr>
</table>

Date	Page	Section	Description
2012/ 05/11	730	31.2	In “Table 31.2-1 Functions of Bits in SYSC Register”, details of the PGSEL bit should be corrected as indicated by the shading below. (Error) This bit is used to select the function of the PG1/PG0 pins. If this bit is set to "0", the PG1/PG0 pins are selected as subclock oscillator pins, and the subclock oscillation is enabled or disabled by the subclock oscillation enable bit (SYCC2:SOSCE). If this bit is set to "1", the PG1/PG0 pins are selected as general-purpose I/O ports. (Correct) This bit is used to select the function of the PG1/PG2 pins. If this bit is set to "0", the PG1/PG2 pins are selected as subclock oscillator pins, and the subclock oscillation is enabled or disabled by the subclock oscillation enable bit (SYCC2:SOSCE). If this bit is set to "1", the PG1/PG2 pins are selected as general-purpose I/O ports.