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CM44-10121-7EL

Major Changes

■ Document Information

	Previous edition	→	Revised edition
Document title	F^2MC-16LX 16-BIT MICROCONTROLLER MB90480/485 Series HARDWARE MANUAL		F^2MC-16LX 16-BIT MICROCONTROLLER MB90480/485 Series HARDWARE MANUAL
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■ Major Changes in Revised Edition

See the following pages.

■ Issuance of this list

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Main changes in this edition

Page	Changes (For details, refer to main body.)
594 to 654	Changed the entire part of "APPENDIX D Instructions"

The vertical lines marked in the left side of the page show the changes.

Reference: Main changes (Rev.5 → Rev.6)

Page	Changes (For details, refer to main body.)
-	Product name is changed. (MB90483B → MB90483C) Series name is changed. (MB90480 SERIES → MB90480/485 SERIES)
i	■ License is added.
11	Function, Pin name D00 to D07 and D08 to D15 in Table 1.5-1 Pin Functions (1/7). (output pin → input/output pin)
93	Figure 3.11-2 Operation of Delay Interrupt Generation Module is changed. (ICR_{XX} → IL) (ICR_{XX} → ILM) (NTA → INTA)
157	Figure 7.3-1 Relationship Between Access Areas and Physical Addresses is changed. (No access → Access Inhibited)
350	■ Conditions for External Connection of Peripheral Devices is changed. ((interim value) is deleted.)
390	The Figure is changed in ■ Serial Mode Control Status Register0/1 (SMCS0/SMCS1). (Deleted the description; *1 and *2.)
531	Figure 25.5-2 Pulse Width Measurement Operation (One-shot Measurement Mode/"H" Level Pulse Width Measurement) is changed.
532	Figure 25.5-3 Pulse Width Measurement Operation (Repeated Measurement Mode/"H" Level Pulse Width Measurement) is changed.
574	Note is added.
580	Figure A-1 Memory Map is changed. (No access → Access inhibited)
581	Table A-1 Relationship Among Address #1, Address #2, and Address #3 by Product Type is changed.
582	Figure A-2 MB90F489B Memory Map is changed. (No access → Access inhibited)
583	Figure A-3 MB90483C Memory Map is added.

The vertical lines marked in the left side of the page show the changes.

Main changes in this edition

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-	Product name is changed. (MB90483B → MB90483C) Series name is changed. (MB90480 SERIES → MB90480/485 SERIES)
i	■ License is added.
11	Function, Pin name D00 to D07 and D08 to D15 in Table 1.5-1 Pin Functions (1/7). (output pin → input/output pin)
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532	Figure 25.5-3 Pulse Width Measurement Operation (Repeated Measurement Mode/"H" Level Pulse Width Measurement) is changed.
574	Note is added.
580	Figure A-1 Memory Map is changed. (No access → Access inhibited)
581	Table A-1 Relationship Among Address #1, Address #2, and Address #3 by Product Type is changed.
582	Figure A-2 MB90F489B Memory Map is changed. (No access → Access inhibited)
583	Figure A-3 MB90483C Memory Map is added.

The vertical lines marked in the left side of the page show the changes.

Main changes in this edition

Page	Changes (For details, refer to main body.)
-	All of the following descriptions are changed. (µDMA → µDMAC) (2M BIT FLASH MEMORY → 2M/3M BIT FLASH MEMORY) (MB90F481/MB90F482 → MB90F481B/MB90F482B/MB90F488B/MB90F489B)
4	Table 1.1-2 MB90485 series product configuration is changed.
5	■ Package of corresponding products is added.
6	Figure 1.2-1 Block diagram of MB90480/485 Series is changed.
9	Figure 1.4-1 Pin assignment diagram of MB90480/485 series (QFP-100) is changed. (Text in the figure is changed.)
10	Figure 1.4-2 Pin assignment diagram of MB90480/485 series (LQFP-100) is changed. (Text in the figure is changed.)
21	❍ Crystal oscillation circuit is changed. (Please ask the crystal maker to evaluate the oscillational characteristics of the crystal and this device. is added.)
22	❍ Notes on using external clock is changed. (Use of the external clock requires a connection with an external pin, as shown in Figure 1.7-1 "Use of external clock". → To use external clock, drive only pin XO. Be sure to set up pin X1 to be open.) ❍ Note on operations during PLL clock mode is changed. (If the PLL clock mode is selected, the microcontroller attempt to be working with the selfoscillating circuit even when there is no external oscillator or external clock input is stopped.Performance of this operation, however, cannot be guaranteed. → On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, Fujitsu will not guarantee results of operations if such failure occurs.)
48	Table 3.2-2 Interrupt factors, interrupt vectors, and interrupt control registers is changed. (*2: Please write "0" in the INTE bit, after prohibiting interrupt by setting the IL2 bit to IL0 bit of the interrupt control register to "111_B", if the reload timer underflow interrupt setting is changed from enable (INTE bit of TMCSR registers =1) to prohibit (INTE bit of TMCSR registers =0). is added.)
75	Figure 3.6-7 µDMAC processing procedure is changed.
78 to 88	3.7 Interrupt by Extended Intelligent I/O Service (EI^2OS) is added.
96	■ Reset factors ❍ Power-on reset of 4.1 Overview of Reset is changed. (MB90F488B → MB90F488B/F489B)
115	Figure 5.3-2 Configuration of PLL output selection register (PLLOS) is changed. (------$X0_B$ → ------00_B) (PLL output selection bit → PLL output frequency doubling selection bit) (Reserved bit → PLL input divided selection bit)
116	Table 5.3-2 Functions of bits for PLL output selection register (PLLOS) is changed. (• The readout value is always 1. → • Read value is undefined.)

Page	Changes (For details, refer to main body.)
143	Table 6.7-1 Pin states in single chip mode is changed. (*3: "Input cutoff" means that operations of input gates located very close to the pins are disabled. "Output Hi-Z" means that the pin-drive transistors are disabled and the pins are set to the high-impedance state. → *2: In the state of "Input cutoff", input A is masked and "L" level is transmitted internally. "Output Hi-Z" means that the pin-drive transistors are disabled and the pins are set to the high-impedance state.)
144	Table 6.7-2 Pin states in external bus 16-bit data bus mode and multiplex 16-bit external bus mode is changed. (*6: "Input cutoff" means that operations of input gates located very close to the pins are disabled. "Output Hi-Z"means that the pin-drive transistors are disabled and the pins are set to the high-impedance state. → *5: In the state of "Input cutoff", input A is masked and "L" level is transmitted internally. "Output Hi-Z" means that the pin-drive transistors are disabled and the pins are set to the high-impedance state.)
145	Table 6.7-3 Pin states in external bus 8-bit data bus mode and multiplex 8-bit external bus mode is changed. (*6: "Input cutoff" means that operations of input gates located very close to the pins are disabled. "Output Hi-Z"means that the pin-drive transistors are disabled and the pins are set to the high-impedance state. → *5: In the state of "Input cutoff", input A is masked and "L" level is transmitted internally. "Output Hi-Z" means that the pin-drive transistors are disabled and the pins are set to the high-impedance state.)
146	Table 6.7-4 Pin states in external bus 16-bit data bus mode and non-multiplex 16-bit external bus mode is changed. (*6: "Input cutoff" means that operations of input gates located very close to the pins are disabled. "Output Hi-Z"means that the pin-drive transistors are disabled and the pins are set to the high-impedance state. → *5: In the state of "Input cutoff", input A is masked and "L" level is transmitted internally. "Output Hi-Z" means that the pin-drive transistors are disabled and the pins are set to the high-impedance state.)
205	❍ Clearing of the watchdog timer is changed. (Note: is changed.)
224	■ Compare clear register (CPCLR) is changed. (When this register value matches the value of the 16-bit free-running timer, the 16-bit free-running timer value is initialized to 0000_H and a compare clear interrupt flag is set. When interrupt operation is allowed, an interrupt request is issued to the CPU. → When the MODE bit of the timer counter control status register (TCCS) is set to "1", the freerunning timer value is initialized to "0000_H" at matching this register value and the value of the free-running timer. When this register value matches the value of the free-running timer, a compare clear interrupt flag is set. When the compare interrupt flag is set to "1", an interrupt request issues to the CPU at allowing the interrupt operation.)
227	[bit3] SCLR is changed. (Note: is added.)
229	Figure 12.3-8 Registers of output compare is changed. (ICP1C → ICP1)
235	12.4 Interrupt of 16-bit Input/Output Timer is added.
246	12.6 Program Example of 16-bit Input/Output Timer is added.
275, 276	13.4 Interrupt of 8/16-bit Up/Down Counter/Timer is added.
285 to 290	13.6 Program Example of 8/16-bit Up/Down Counter/Timer is added.
299	[bit3] INTE (Timer interrupt request enable) is changed. (Note: is added.) [bit2] UF (Timer interrupt request flag) is changed. (Note: is added.)
312 to 316	14.5 Program Example of 16-Bit Reload Timer is added.

Page	Changes (For details, refer to main body.)
316	■ Setting method other than program example is changed. (● Method to enable interrupt is added.)
344	■ Interrupt/DTP enable register (ENIR: Enable interrupt request register) is changed. (Note: is added.)
345	■ Interrupt/DTP source register (EIRR: External interrupt request register) in 16.2 Configuration and Functions of DTP/External Interrupt Unit Registers is changed. (Note is changed.)
350	■ Procedures for DTP/external interrupt unit operation is changed. ((1) Set the pin used as an external interrupt input and the general-purpose I/O port used combinedly to the input port. is added.)
362	[bit2, bit1, bit0] ANE2, ANE1, ANE0: ANalog End channel set is changed. (Note: is added.)
367	17.4 Interrupt of 8/10-Bit A/D Converter is added.
368	❍ Single Mode is changed. (Note: is added.)
378	■ Handling of analog input pins is changed. (● Precautions on use of the 8/10-Bit A/D Converter is added.)
379	17.8 Program Example of 8/10-Bit A/D Converter is added
390	BUSY bit of ■ Serial mode control status register0/1 (SMCS0/1) is changed. (R/W → R)
396	18.4 Interrupt of Expanded I/O Serial Interface is added
404 to 406	18.6 Program Example of Expanded I/O Serial Interface is added
413	[bit5, bit4, bit3] CS2, CS1, CS0: Clock Select is changed. (• The use of the clock division ratio 1/1 (CS2 to CS0 = 000_B) during synchronous transfer is prohibited. → • Please do not use the following settings when dedicated baud rate generator is used at synchronous transfer. 1) CS2 to CS0 = 000_B 2) CS2 to CS0 = 001_B, DIV3 to DIV0 = 0000_B)
420	[bit11, bit10, bit9, bit8] DIV3, DIV2, DIV1, DIV0 is changed. (Notes: is changed.)
421	19.4 Interrupt of UART is added
424	Table 19.5-2 Division ratios of the synchronous transfer clock is changed. (The value of CLK synchronous is changed.) (Φ: Calculated based on the machine clock (internal frequency f=16 MHz) for DIV=1. → ϕ: Calculated based on the machine clock (internal frequency f=16 MHz) for DIV=2.) (Note: is changed.)
426	Table 19.5-4 Relationship between baud rate and reload value (machine clock frequency: 7.3728 MHz) is changed. (Note: is added)
427	❍ Transfer data format is changed. (In normal mode of operation mode 0, the data length can be set to 7 bits or 8 bits. → In operation mode 0, data items without parity are fixed at a length of 7 bits, while data items with parity have a length of 8 bits.)

Page	Changes (For details, refer to main body.)
437	❍ Clock setting in synchronous transfer is added
438 to 444	The whole description across 19.7 Program Example of UART is changed.
452	The figure of bit configuration in ■ Chip selection control register (CSCR) is changed. (* : The initial value of this bit is "1" or "0". The value depends on the mode pins (MD2, MD1, D0 pins). is added.)
474	■ Registers of the ROM mirror function selection module is changed. (The figure of bit configuration is changed.)
475	■ ROMM (ROM mirror function selection register) is changed. (The figure of bit configuration is changed.) [bit9] MS is changed. (Note: is added)
478	■ Features of the 2M/3M bit flash memory is changed. (The description of • 3M: 384K words x 8 bits/192K words x 16 bits (16K + 8K + 8K + 32K + 64K + 64K + 64K + 64K + 64K) sector configuration is added.)
479	Figure 23.2-1 Sector Configuration of 2M/3M Bit Flash Memory is changed.
501	■ Suspending sector erasure for the flash memory is changed. (If a sector erase suspend command is entered during the sector erase wait time, sector erase wait ends immediately, the erase operation is interrupted, and the operational state changes to erase stop. If a erase suspend command is entered during a sector erase operation after the sector erase wait time, the system enters the erase suspend mode after 15 µs have elapsed or earlier. → If a erase suspend command is entered during a sector erase operation after the sector erase wait time, the system enters the erase suspend mode after 20 µs have elapsed or earlier. Please execute the sector erase stop command after sector erase command or sector erase resume command issuing and 20 µs or more.)
503	Table 23.7-1 Flash Security Bit Address is changed. (Flash memory size and Security bit address of MB90F489B are added)
506	■ Basic Configuration of Serial Programming Connection with MB90F481B/MB90F482B/MB90F488B/MB90F489B is changed. (It is possible to write it by selecting either of the program that operates by the single chip mode or the internal ROM external ROM bus mode. is added.)
507	Table 24.1-1 Function of pins is changed.
527, 528	25.4 Interrupt of PWC Timer is added
563	[bit12] MSS: Master Slave Select is changed. (Note: is added)
572, 573	27.4 Interrupt of I^2C Interface is added
579	Table A-1 Relationship among address #1, address #2, and address #3 by product type is changed. (Contents of the table is changed.) (*1 and *2 are added.)
580	Figure A-2 MB90F489B memory map is added
589	Table C-1 Relationship between interrupt sources and interrupt vector/interrupt control registers is changed.
625	Table D.8-17 6 Accumulator operation instructions (byte, word) is changed. (SWAPW / XCHW A,T → SWAPW)