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MB90950 Series

16-BIT Microcontroller
F^2MC-16LX
Hardware Manual

Errata Sheet

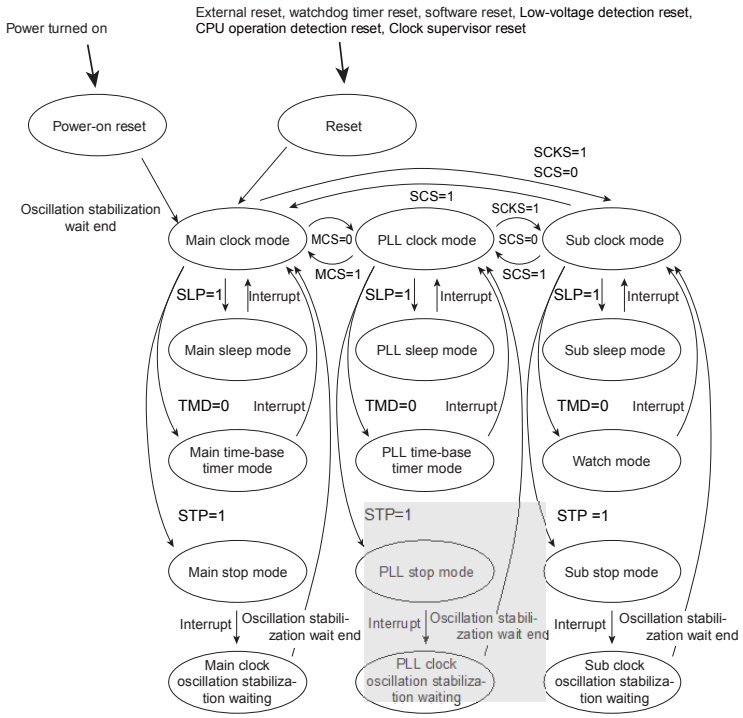
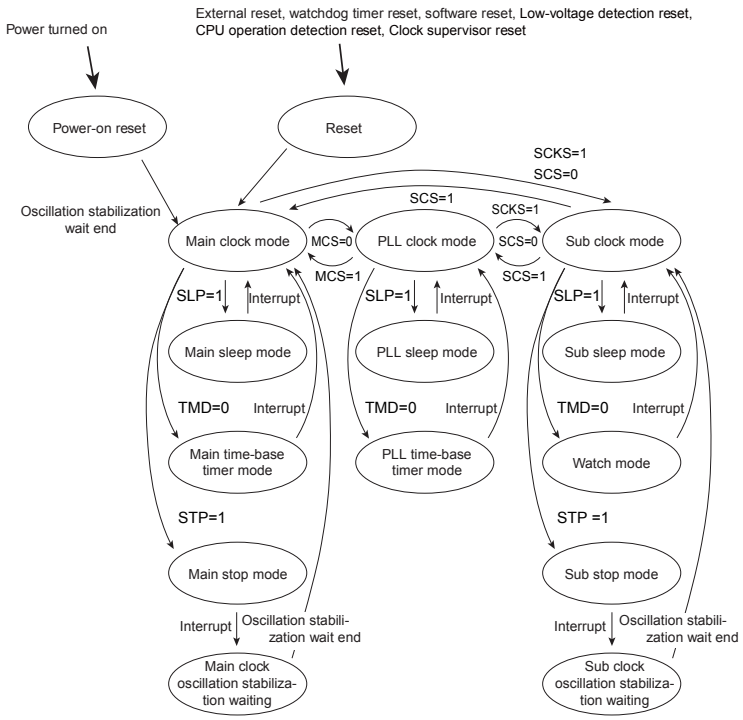
Page	Section	Description
Original document code: CM44-10148-4E		
Revision 1.0 February 2, 2015		
121	5.3	Table 5.3-1 Functions of Clock Selection Register (CKSCR) (1 / 2) of WS1 and WS0 bits were corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) The oscillation stabilization wait time is fixed to 2^{14}/HCLK when switching from the main clock to the PLL clock mode (when the oscillation clock frequency is 4 MHz: approx. 4.1 ms). The oscillation stabilization wait time depends on the value set in the bits when switching from the sub clock to the PLL clock mode or returning from PLL stop to PLL clock mode. Since the PLL clock oscillation stabilization wait time requires 2^{14}/HCLK or more, when switching from sub clock to PLL clock mode or transiting to PLL stop mode, set "10_B" or "11_B" for these bits. (Correct) The oscillation stabilization wait time is fixed to 2^{14}/HCLK when switching from the main clock to the PLL clock mode (when the oscillation clock frequency is 4 MHz: approx. 4.1 ms). The oscillation stabilization wait time depends on the value set in the bits when switching from the sub clock to the PLL clock mode. Since the PLL clock oscillation stabilization wait time requires 2^{14}/HCLK or more, when switching from sub clock to PLL clock mode, set "10_B" or "11_B" for these bits.
164	7.5.4	7.5.4 Stop Mode was corrected to change the description concerned with PLL stop mode as shown the shading below. (Error) ■ Stop Mode If "1" is written in the STP bit of low-power consumption mode control register (LPMCR) while the PLL clock mode is operating (CKSCR: MCS=1, SCS=0), the mode switches to the stop mode based on the settings of MCS bit and SCS bit in the clock selection register (CKSCR). (Correct) ■ Stop Mode If "1" is written in the STP bit of low-power consumption mode control register (LPMCR) while a clock mode is operating, the mode switches to the stop mode based on the settings of MCS bit and SCS bit in the clock selection register (CKSCR).

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>164</td><td>7.5.4</td><td>Table 7.5-3 Clock Selection Register (CKSCR) Settings and Their Stop Modes was corrected to change the description concerned with PLL stop mode as shown the shading below.

(Error)
<table>
<tr><td colspan="2">Clock selection register (CKSCR)</td><td rowspan="2">Stop mode to switch to</td></tr>
<tr><td>MCS</td><td>SCS</td></tr>
<tr><td>1</td><td>1</td><td>Main stop mode</td></tr>
<tr><td>0</td><td>1</td><td>PLL stop mode</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Sub stop mode</td></tr>
<tr><td>0</td><td>0</td></tr>
</table>
(Correct)
<table>
<tr><td colspan="2">Clock selection register (CKSCR)</td><td rowspan="2">Stop mode to switch to</td></tr>
<tr><td>MCS</td><td>SCS</td></tr>
<tr><td>1</td><td>1</td><td>Main stop mode</td></tr>
<tr><td>0</td><td>1</td><td>Setting disabled</td></tr>
<tr><td>1</td><td>0</td><td rowspan="2">Sub stop mode</td></tr>
<tr><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>164</td><td>7.5.4</td><td>The Note was added for the transition to the stop mode as follows.

・The transition to the stop mode must be set at Main clock and Sub clock mode.</td></tr>
<tr><td>166</td><td>7.5.4</td><td>The Note was corrected to delete the description concerned with PLL stop mode as shown the shading below.

When switching to the PLL stop mode, set "10_B" or "11_B" to the oscillation stabilization wait time selection bits in the clock selection register (CKSCR: WS1, WS0).
• During the PLL stop mode, a main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time have to be secured when returning from the PLL stop mode because the main clock and PLL multiplier circuits are stopped. The oscillation stabilization wait time in this case bases upon the values set in the oscillation stabilization wait time selection bits in the clock selection register (CKSCR:WS1, WS0), and the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time will be counted together. Therefore, set a value to the "CKSCR:WS1, WS0" bits in line with the longest one of the oscillation stabilization wait times. However, because 2^{14}/HCLK or more is needed for the PLL clock oscillation stabilization wait time, set "10_B" or "11_B" to the "CKSCR: WS1, WS0" bits.</td></tr>
</table>

Page	Section	Description
167	7.6	Figure 7.6-1 State Transition Chart was corrected to delete the description concerned with PLL stop mode and PLL clock oscillation stabilization wait as shown below figure. (Error)  (Correct) 

Page	Section	Description
173	7.8	7.8 Notes on Using the Low-power Consumption Mode was corrected to add the description concerned with transiting stop mode as shown the shading below. ■ **At Transiting the Stop Mode** The transition to the stop mode must be set at Main clock and Sub clock mode. If the mode is transited to the stop mode during PLL clock mode,set the stop mode after transiting Main clock mode once.
174	7.8	7.8 Notes on Using the Low-power Consumption Mode was corrected to delete the description concerned with PLL stop mode as shown the shading below. ■ **Oscillation Stabilization Wait Time** ● PLL clock oscillation stabilization wait time During the PLL stop mode, a main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time have to be secured when returning from the PLL stop mode because the main clock and PLL multiplier circuits are stopped. The oscillation stabilization wait time in this case bases upon the values set in the oscillation stabilization wait time selection bits in the clock selection register (CKSCR:WS1, WS0), and the main clock oscillation stabilization wait time and PLL clock oscillation stabilization wait time will be counted together. Therefore, set a value to the "CKSCR:WS1, WS0" bits in line with the longest one of the oscillation stabilization wait times. However, because 2^{14}/HCLK or more is needed for the PLL clock oscillation stabilization wait time, set "10_B" or "11_B" to the "CKSCR: WS1, WS0" bits.
215	10.2	10.2 Block Diagram of the Time-base Timer of Counter clearing circuit was corrected to change the description concerned with PLL stop mode as shown the shading below. (Error) ■ **Block Diagram of the Time-base Timer** ● Counter clearing circuit The value of the time-base timer counter will be cleared due to the following sources. • The time-base timer counter clearing bit of the time-base timer control register (TBTC: TBR=0) • Power-on reset • Transition to the main stop mode or PLL stop mode (CKSCR:SCS=1, LPMCR: STP=1) (Correct) ■ **Block Diagram of the Time-base Timer** ● Counter clearing circuit The value of the time-base timer counter will be cleared due to the following sources. • The time-base timer counter clearing bit of the time-base timer control register (TBTC: TBR=0) • Power-on reset • Transition to the main stop mode (CKSCR:MCS=1,SCS=1, LPMCR: STP=1)

<table>
<tr><th>Page</th><th>Section</th><th>Description</th></tr>
<tr><td>218</td><td>10.3.1</td><td>Table 10.3-1 Functions of the Time-base Timer Control Register (TBTC) of TOBF bit was corrected to delete the description concerned with PLL stop mode as shown the shading below.

(Error)
2) The TBOF bit is cleared in the case of writing of "0", transition to the main stop mode, transition to the PLL stop mode, transition from the sub clock mode to the main clock mode, transition from the sub clock mode to the PLL clock mode, transition from the main clock mode to the PLL clock mode, writing of "0" into the time-base timer counter clearing bit (TBR), and reset.

(Correct)
2) The TBOF bit is cleared in the case of writing of "0", transition to the main stop mode, transition from the sub clock mode to the main clock mode, transition from the sub clock mode to the PLL clock mode, transition from the main clock mode to the PLL clock mode, writing of "0" into the time-base timer counter clearing bit (TBR), and reset.</td></tr>
<tr><td>223</td><td>10.5</td><td>Table 10.5-1 Time-base Timer Clearing Conditions and Oscillation Stabilization Wait Time (2 / 2) was corrected to delete the description concerned with PLL stop mode as shown the shading below table.

(Error)
<table>
<tr><th>Operation</th><th>Counter cleared</th><th>TBOF cleared</th><th>Oscillation stabilization wait time</th></tr>
<tr><td colspan="4">Cancellation of stop modes</td></tr>
<tr><td>Canceling the main stop mode</td><td>○</td><td>○</td><td>After the main clock oscillation stabilization wait time is terminated, switches to the PLL clock mode</td></tr>
<tr><td>Canceling the PLL stop mode</td><td>○</td><td>○</td><td>After the main clock oscillation stabilization wait time is terminated, switches to the PLL clock mode</td></tr>
<tr><td>Canceling the sub stop mode</td><td>×</td><td>×</td><td>After the sub clock oscillation stabilization wait time is terminated, switches to the sub clock mode</td></tr>
</table>
(Correct)
<table>
<tr><th>Operation</th><th>Counter cleared</th><th>TBOF cleared</th><th>Oscillation stabilization wait time</th></tr>
<tr><td colspan="4">Cancellation of stop modes</td></tr>
<tr><td>Canceling the main stop mode</td><td>○</td><td>○</td><td>After the main clock oscillation stabilization wait time is terminated, switches to the PLL clock mode</td></tr>
<tr><td>Canceling the sub stop mode</td><td>×</td><td>×</td><td>After the sub clock oscillation stabilization wait time is terminated, switches to the sub clock mode</td></tr>
</table></td></tr>
<tr><td>224</td><td>10.6</td><td>10.6 Notes on Using the Time-base Timer was corrected to delete the description concerned with PLL stop mode as shown the shading below.

(Error)
● When using as an oscillation stabilization wait time timer
• The oscillation clock is not operating after power is turned on or in main stop, PLL stop, and sub clock modes.

(Correct)
● When using as an oscillation stabilization wait time timer
• The oscillation clock is not operating after power is turned on or in main stop and sub clock modes.</td></tr>
</table>

Page	Section	Description
224	10.6	10.6 Notes on Using the Time-base Timer was corrected to delete the description concerned with PLL stop mode as shown the shading below. (Error) ● Peripheral functions to which the time-base timer provides clock • When transiting to the operation mode where the oscillation clock pauses (the PLL stop mode, sub clock mode, and main stop mode), the time-base timer counter is cleared and the time-base timer stops operating. (Correct) ● Peripheral functions to which the time-base timer provides clock • When transiting to the operation mode where the oscillation clock pauses (sub clock mode, and main stop mode), the time-base timer counter is cleared and the time-base timer stops operating.