3300 W 52 V LLC with 600 V CoolMOS™ CFD7 and XMC™

EVAL_3K3W_LLC_HB_CFD7

About this document

Scope and purpose

This document introduces a complete Infineon Technologies AG system solution for a 3300 W DC-DC converter from 400 V to 51.5 V achieving 98.1 percent peak efficiency. The converter (EVAL_3K3W_LLC_HB_CFD7) is a Half-Bridge (HB) LLC with full-bridge rectification, split resonant capacitor and clamping diodes on the primary side. The EVAL_3K3W_LLC_HB_CFD7 has been designed following the requirements of telecom and battery charging applications: wide range input (hold-up time) and wide range output from 43.5 V up to 59.5 V.

This document describes the converter hardware (Figure 1) and the design parameters of the full Infineon solution including 600 V CoolMOS™ CFD7, 80 V OptiMOS™ 5, an innovative magnetic construction and a novel cooling concept.

The main Infineon components used in the 3300 W LLC HB are:

- 600 V CoolMOS™ CFD7 Super-Junction (SJ) MOSFET
- 80 V OptiMOS™ 5 Synchronous Rectifier (SR) MOSFET
- 2EDS8265H safety isolated, 1EDI20N12AF and 2EDF7275F functional isolated gate drivers (EiceDRIVER™)
- XMC4200-F64k256AB microcontroller
- ICE5QSAG CoolSET™ Quasi Resonant (QR) Flyback controller
- 800 V CoolMOS™ P7 SJ MOSFET
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC-DC step-down voltage regulator
- SmartRectifier controller IR1161LPBF

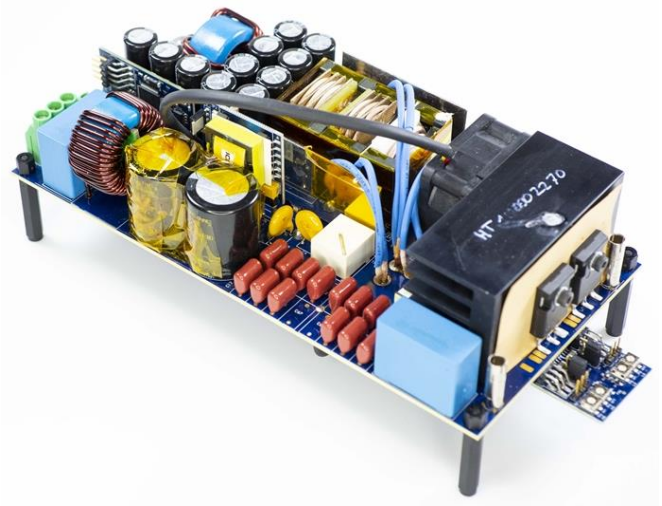

Figure 1 3300 W LLC HB

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

Keypoints

- Introduces a complete design approach for a 3300 W HB LLC DC-DC converter achieving high efficiency and power density
- Explains resonant tank design using First Harmonic Approximation and its impact on gain range and efficiency tuning
- Describes integration of digital control with adaptive algorithms for protection, burst mode, and dynamic load response
- Provides implementation details of innovative cooling and stacked magnetic construction for thermal performance and compact layout
- Compares CoolMOS™ CFD7 device characteristics and RDS(on) options to optimize efficiency across different load conditions

About this product family

Product family

Infineon's CoolMOS™ is a high-voltage N-channel silicon power MOSFET that is designed to provide excellent thermal performance, lowest switching and conduction power losses, and optimal RDS(on) for increased system efficiency, supporting a range of application from low power levels to high power levels.

Target applications

- Consumer electronics
- Industrial applications
- Home appliances
- Server
- Telecom
- Renewables

Table of contents

About this document **1**
About this product family **2**
Table of contents **3**
1 Background and system description **4**
1.1 System description 5
1.1.1 Resonant tank design 7
1.1.2 Converter gain in nominal operation 9
1.1.3 Converter gain in boost operation 10
1.1.4 Converter gain in buck operation 12
1.2 Board description 13
1.3 600 V CoolMOS™ CFD7 in LLC 15
1.3.1 600 V CoolMOS™ CFD7 $R_{DS(on)}$ comparison 17
1.3.2 CoolMOS™ CFD7 to CFD2 comparison 20
1.4 Transformer 21
1.5 Cooling solution 24
1.6 Validation set-up 26
2 Experimental results **27**
2.1 Specification and test results 27
2.2 Performance and steady-state waveforms 27
2.2.1 Primary-side ZVS 27
2.2.2 Synchronous rectifiers 29
2.2.3 Dynamic response: load jumps 32
2.2.4 Soft-start-up 34
2.2.5 Resonant tank 36
2.2.6 Brown-in and brown-out 37
2.2.7 Overcurrent protection 39
2.2.8 Burst mode operation 40
2.3 Thermal map 42
3 User interface **44**
4 Summary **46**
5 Schematics **47**
6 Bill of materials (BOM) **51**
7 Related resources **56**
References **57**
Revision history **58**
Disclaimer **59**

1 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. High efficiency is a key parameter in achieving this increasing power density because the heat dissipation must be minimized. Furthermore, higher efficiency directly impacts the ownership cost during the lifetime of the converter. Toward this goal, fully resonant topologies such as the LLC are often considered to be the best approach in these power and voltage ranges.

The outstanding efficiency shown in Figure 2 can only be achieved by using a 600 V CoolMOS™ CFD7 in TO-247 package together with 80 V OptiMOS™ 5 SRs. The outstanding performance of these semiconductor technologies, the innovative cooling concept solution and the stacked magnetic construction enables power density in the range of 4 W/cm^3 (66 W/in^3).

The board was designed as a testing platform, with easy access to probe points, and easy reworking/replacement of components. The power density can be largely improved; and even more in an enclosed design, which further improves the cooling capability of the proposed solution.

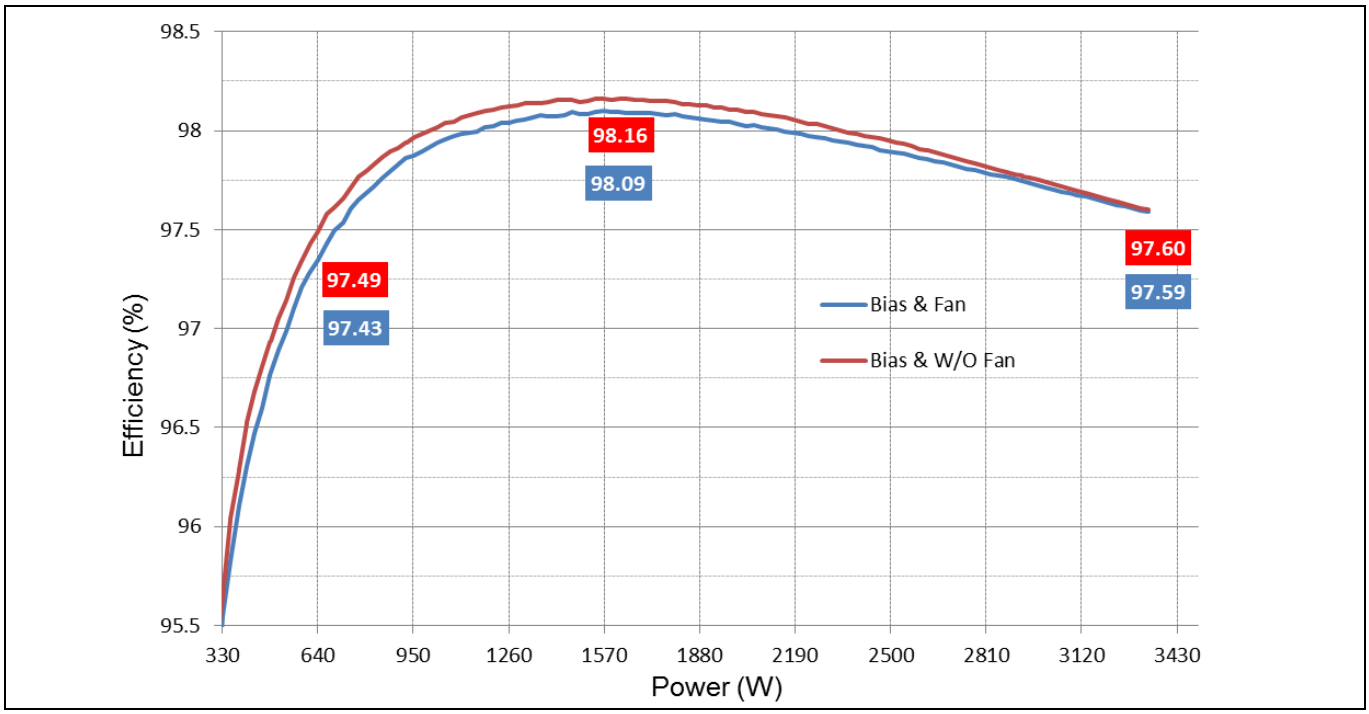

Figure 2 Measured efficiency of the 3300 W LLC HB at 400 V input and 51.5 V output

The 3300 W LLC HB DC-DC converter has been designed with Infineon power semiconductors as well as Infineon drivers and controllers. The Infineon components used in the 3300 W LLC HB are:

- 18 mΩ 600 V CoolMOS™ CFD7 (IPW60R018CFD7) in the HV HB
- 3.7 mΩ 80 V OptiMOS™ 5 in Super SO-8 package (BSC037N80NS5) in the LV bridge
- 2EDS8265H safety isolated, 1EDI20N12AF and 2EDF7275F functional isolated gate drivers (EiceDRIVER™)
- ICE5QSAG QR Flyback controller with external 4.5 Ω 800 V CoolMOS™ P7 (IPU80R4K5P7) for the auxiliary supply [1]
- XMC4200 microcontroller for control implementation (XMC4200-F64k256AB)
- Medium-power Schottky diode BAT165
- IFX91041EJV33 DC/DC step-down voltage regulator

- SmartRectifier controller IR1161LPBF for the control of the SRs

This document describes the system and hardware of the 3300 W LLC HV, as well as the design specification requirements and the main test results. For further information on Infineon semiconductors see the Infineon website, as well as the Infineon evaluation board search tool, and the different websites for the different implemented components:

- CoolMOS™ power MOSFETs
- OptiMOS™ power MOSFETs
- Gate driver ICs
- QR CoolSET™
- XMC™ microcontrollers

1.1 System description

The EVAL_3K3W_LLC_HB_CFD7 design consists of an LLC HB with SR in full-bridge configuration, with split capacitor and clamping diodes on the primary side (Figure 3).

The control is implemented with an XMC4200 Infineon microcontroller, which includes voltage regulation functionality, burst mode operation, output Overcurrent Protection (OCP), Overvoltage Protection (OVP), Undervoltage Protection (UVP), Undervoltage Lockout (UVLO), soft-start, SR control, adaptive dead-times (bridge and SRs) and serial communication interface. Further details about the digital control implementation and additional functionalities of the LLC control with the XMC™ 4000 family can be found in [2].

The converter's nominal output is at telecom level (51.5 V) with wide range capability, also tailored for 48 V battery charger systems working within the 59.5 V to 43.5 V range. The converter is operated at a nominal input voltage of 400 V, whereas it can regulate down to 360 V at full load (at nominal 51.5 V output voltage) providing room for hold-up time whenever the design is part of a full AC-DC converter.

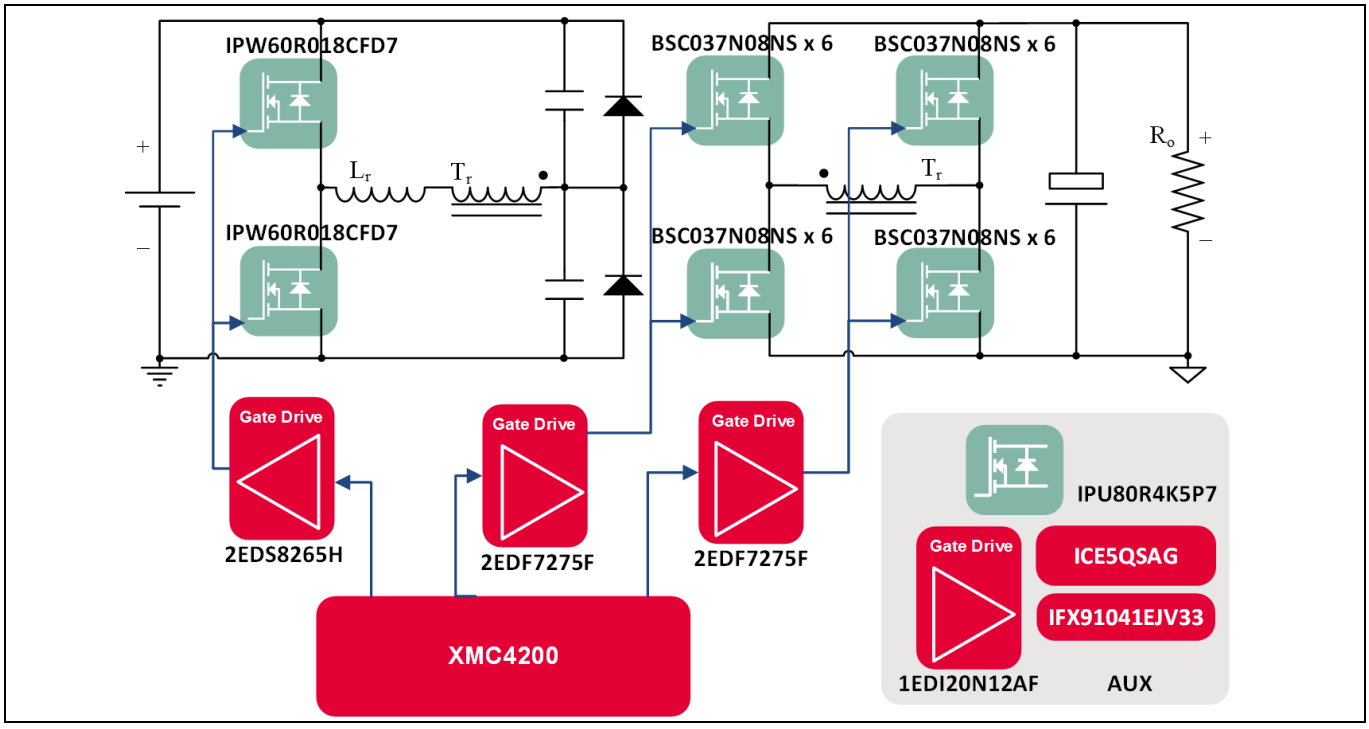

Figure 3 3300 W LLC HB (EVAL_3K3W_LLC_HB_CFD7) – simplified diagram showing the main Infineon semiconductors used

At the nominal input and output voltages the converter operates at nearly fixed frequency (resonance). Above the resonance the switching frequency increases and the switching and core losses become dominant. On the other hand, under resonance the rms currents and their related losses increase. Consequently the overall efficiency of the converter tends to decrease, moving away from the nominal conversion ratio (Figure 4 and Figure 5).

The switching frequency of the converter ranges from 45 kHz up to 250 kHz. The maximum efficiency is achieved around 70 kHz, which corresponds to the resonant tank natural frequency at the nominal input 400 V and output 51.5 V voltages.

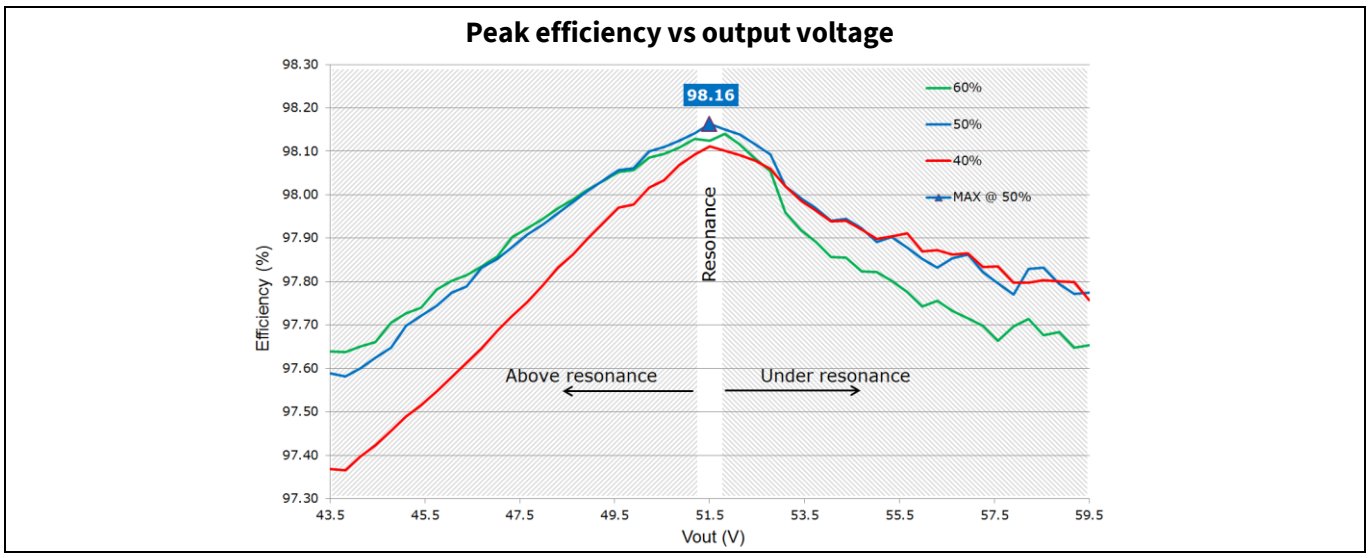

Figure 4 **Estimated efficiency of the 3300 W LLC HB at different output voltages and fixed nominal input 400 V. The maximum efficiency is achieved around the resonance operation. Above resonance the switching losses become dominant. Under resonance the conduction losses dominate**

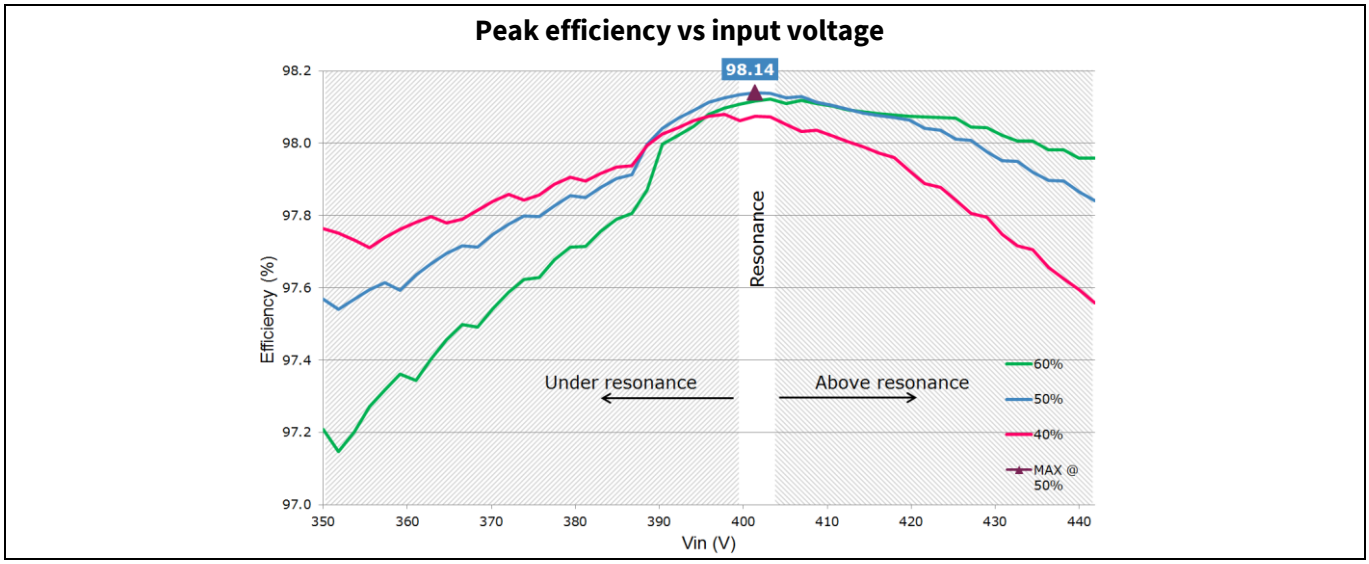

Figure 5 **Estimated efficiency of the 3300 W LLC HB at different input voltages and fixed nominal output 51.5 V. In a full-power supply the converter operates most of the time with the nominal input voltage. During hold-up time conditions only the input voltage drops below nominal**

1.1.1 Resonant tank design

The design of the converter and the resonant tank is based on the widespread First Harmonic Approximation (FHA) for LLC converters. The FHA is extensively covered in the literature and is not explained further here [3].

The quality factor *Q* should be small enough to achieve the maximum output power at the minimum input voltage $V_{in,min}$ and the maximum output voltage $V_{o,max}$ (maximum gain). The given maximum boosting gain required fixes the resonant capacitance C_r for a chosen resonant frequency F_{res}, with F_{res} being a free design parameter the designer can use to tune the maximum efficiency of the converter.

In the 3300 W LLC HB the maximum efficiencies can be achieved with a F_{res} around 70 kHz (Figure 6). This should not be confused with the maximum efficiency of the converter at switching frequencies near resonance, presented in the previous version. The transformer construction, the selection of semiconductor technologies and their $R_{DS(on)}$ influences the maximum achievable efficiency and at which F_{res} it can be achieved. The final selection of F_{res} and other design parameters would require further iterations of the design procedure.

For each F_{res} the corresponding C_r can be calculated with (1) where R_{ac} stands for the reflected load resistance. In this design the resonant frequency was fixed to 70 kHz, which results in a $C_r \approx 465$ nF. In practice C_r and the other resonant tank values are approximated, and not all values can be realized in the real hardware.

$$\begin{cases} Q = \frac{\sqrt{\frac{L_r}{C_r}}}{R_{ac}} \\ F_{res} = \frac{1}{2\pi\sqrt{L_r C_r}} \end{cases} \xrightarrow{\text{yields}} C_r = \frac{1}{2\pi F_{res} R_{ac} Q}$$

Equation 1

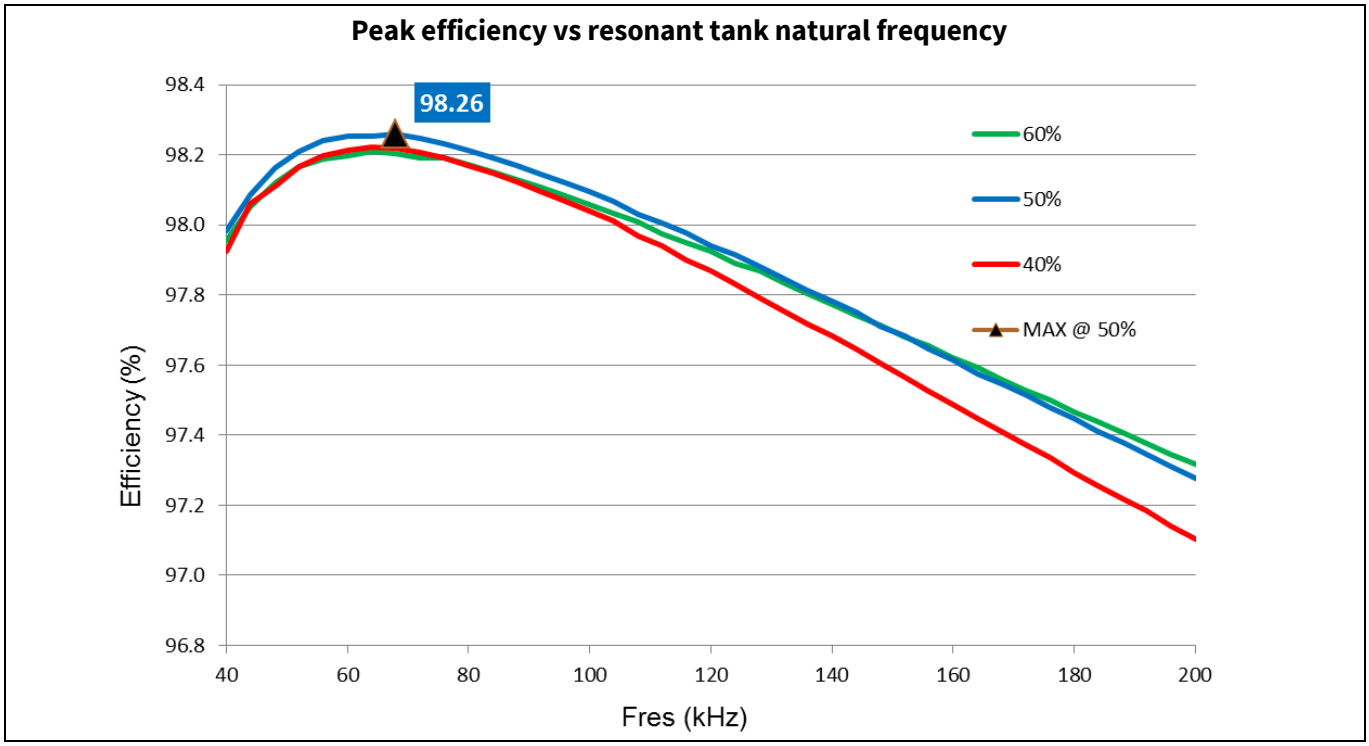

Figure 6 Estimated efficiency of the 3300 W LLC HB for different resonant frequencies (with fixed *Q* and L_r to L_m ratio). Estimated at nominal conditions: 400 V input and 51.5 V output

The corresponding value of L_r for the selected F_{res} can be calculated with (2). In this design the resulting value is $L_r \approx 10.5\ \mu H$.

$$L_r = \frac{1}{C_r(2\pi F_{res})^2}$$

Equation 2

The ratio of the total primary inductance to the resonant inductance *m* is a trade-off between the efficiency at nominal conditions and the converter gain range (3):

$$m = \frac{L_r + L_m}{L_r}$$

Equation 3

- A big ratio *m* reduces the primary-side circulating currents and, consequently, the conduction losses. However, it also reduces the available energy for Zero Voltage Switching (ZVS) in the primary-side HB (Figure 7). Furthermore, it makes it difficult to maintain the regulation at reduced loads and low output voltages (minimum gain) without greatly increasing the F_{switch} (Figure 12)

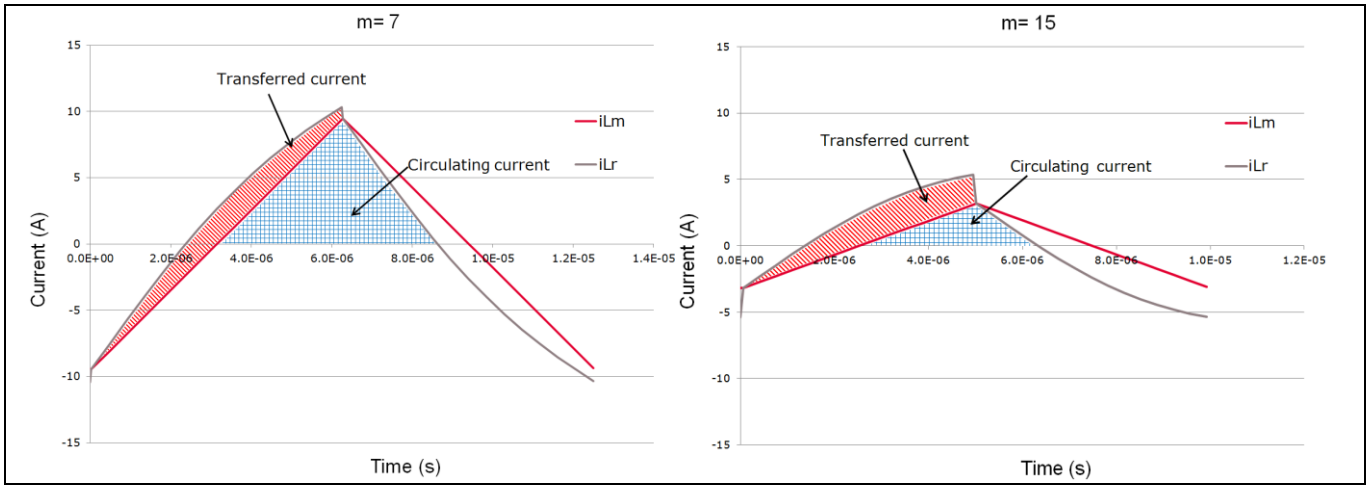

Figure 7 Primary-side current waveforms at 10 percent of load, 400 V input and 51.5 V output. A smaller magnetizing inductance (m = 7) increases the available energy for the HV MOSFET transitions, which ultimately extends the ZVS range

- A small ratio *m* increases the primary-side circulating currents (Figure 8). However, it also increases the available energy for ZVS in the primary-side HB, which ultimately enables a lower $R_{DS(on)}$ and overall higher efficiency along all the load range. Furthermore, the gain range of the converter is extended and the switching frequency span reduced

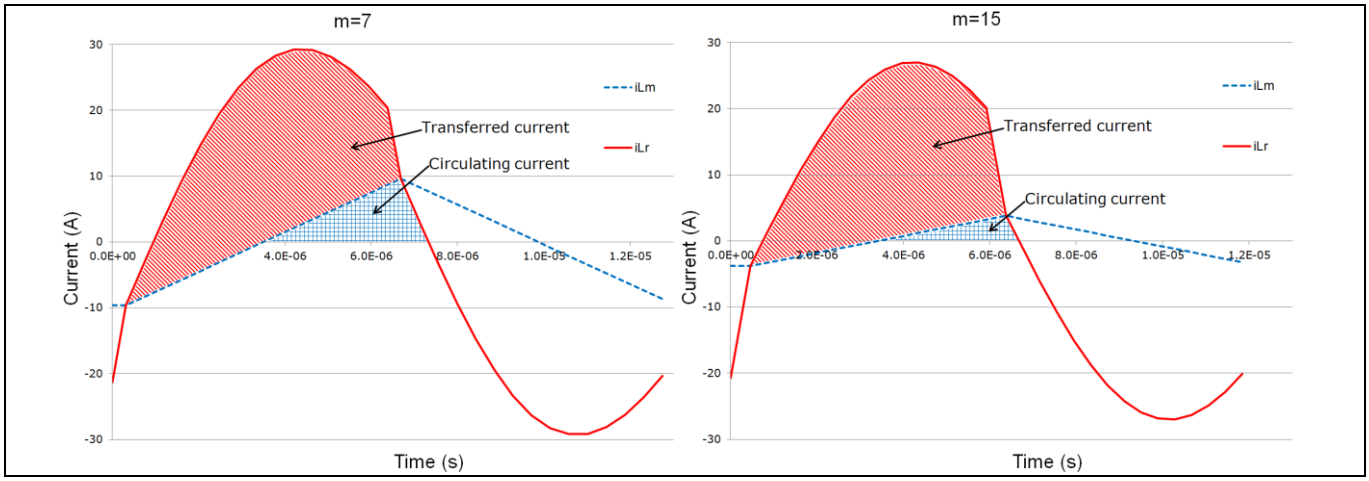

Figure 8 Primary-side current waveforms at 100 percent of load, 400 V input and 51.5 V output. A smaller magnetizing inductance (m = 7) increases the rms currents through the primary side of the converter. However, this can be compensated by a smaller $R_{DS(on)}$ thanks to the extra energy available at a light load

For wide input and/or wide output converters like the 3300 W LLC HB a small ratio *m* is required. However, achieving the full regulation range would still require special considerations, especially at light load and maximum input $V_{in,max}$ or minimum output voltage $V_{o,min}$ (minimum required gain). One of the most widespread solutions for the extension of the gain range (buck operation) is the burst mode control scheme [4].

1.1.2 Converter gain in nominal operation

The gain curves of the 3300 W LLC HB converter at the nominal output voltage and different loads are plotted in Figure 7. It can be observed that the frequency span along the load depends heavily on the operating point of the converter. Near resonance the frequency is almost constant along the load. However, deep under resonance (Figure 8), and especially far above resonance (Figure 9), the required frequency span increases dramatically.

An LLC converter is usually designed for its peak efficiency at the nominal conditions, which corresponds ideally to its most frequent mode of operation. For this design the specifications are 400 V input and 51.5 V output with the peak efficiency at 50 percent of load.

The peak efficiency of the converter (at the point of load of interest) does not necessarily happen exactly at resonance in every LLC converter design. In this converter the peak efficiency (50 percent of load) is achieved at 400 V input and 51.5 V output, as can be observed in Figure 4. This operation point is slightly above resonance, where the sum of frequency-related losses and the conduction-related losses are at their minimum. A different $R_{DS(on)}$ selection, for example, can change the balance of losses and shift the operating conditions for peak efficiency.

Note: It is known that the FHA loses accuracy at switching frequencies far from F_{res}. The required gain at the corner cases ($V_{in,min}$, $V_{in,max}$, $V_{o,min}$, $V_{o,max}$) has to be further investigated in circuit simulations and verified in the final hardware.

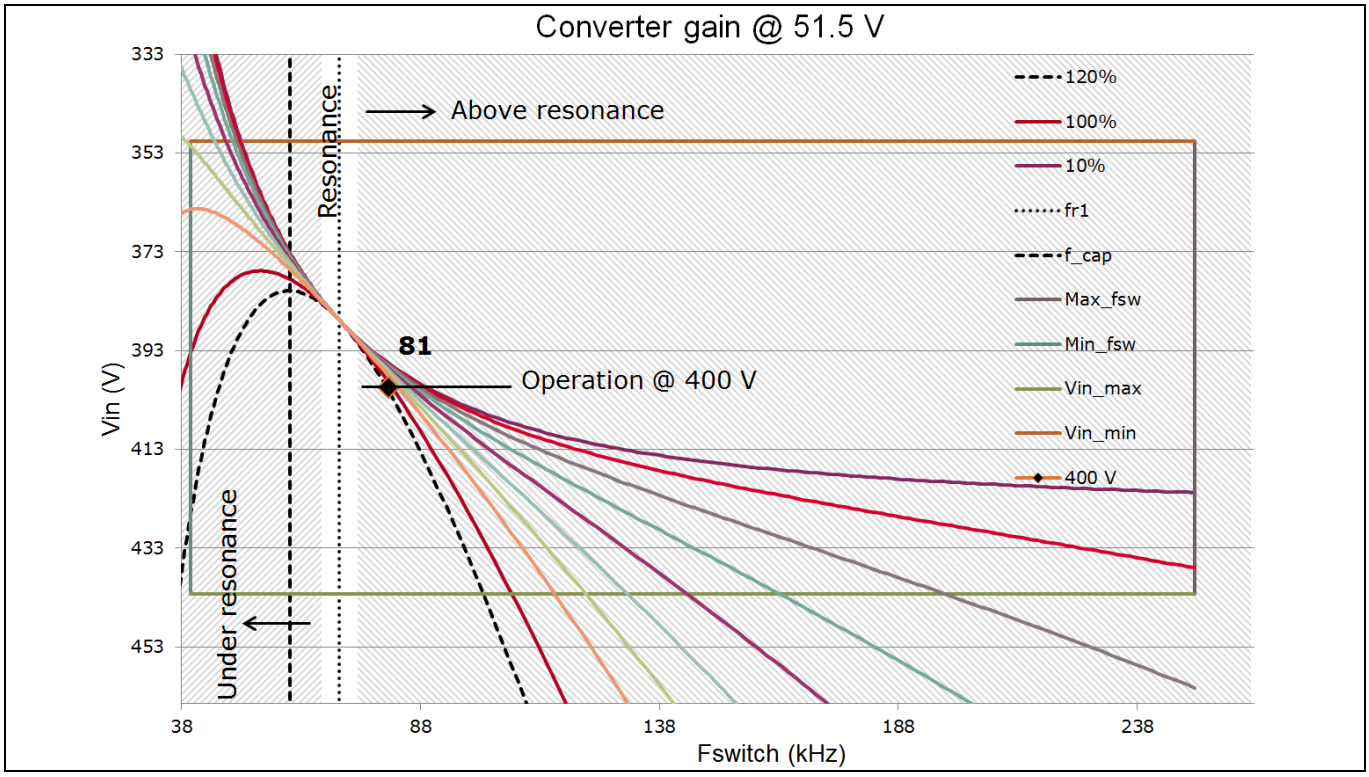

Figure 9 **Estimated gain of the converter while operating at fixed 51.5 V output. Near resonance the switching frequency variation along the load range is small**

1.1.3 Converter gain in boost operation

For output voltages above the nominal (higher than 52 V) the converter operates in the boost region, or the so-called under-resonance (Figure 10). The boost region is also entered with low input voltages, for example during hold-up time.

Under resonance and operating with heavy loads the converter risks entering the so-called capacitive mode where the ZVS of the primary-side MOSFETs is lost and they become hard commutated. This undesired condition can be prevented in several ways: limiting the minimum switching frequency (45 kHz in this design); limiting the maximum output current at the higher output voltages; using clamping diodes in the primary side, which avoids that the primary-side current increases out of control [5].

Although the clamping diodes are a common solution they also limit the maximum output current at the higher output voltages (Figure 11). When the resonant capacitors' voltage swings up to the HV rails, the clamping diodes conduct, which ultimately limits the maximum gain of the converter.

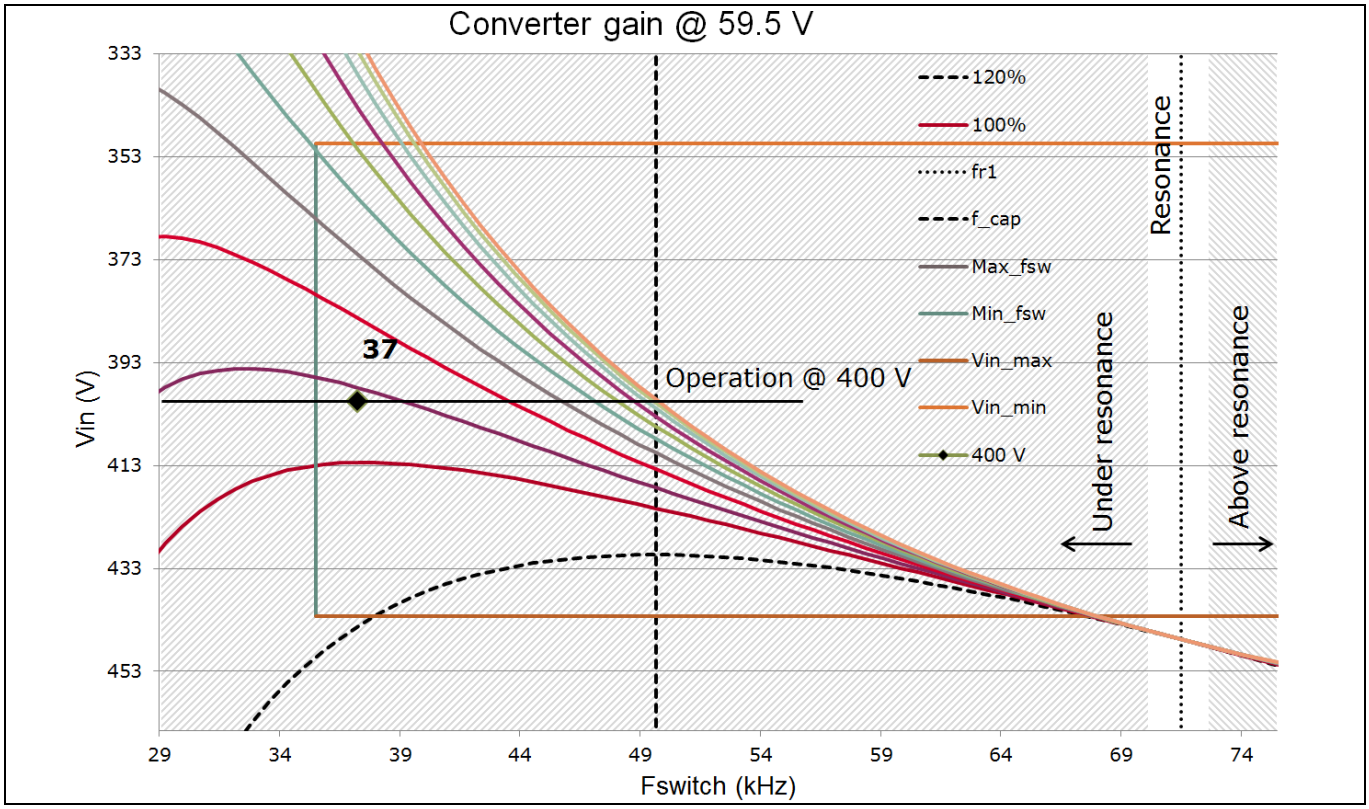

Figure 10 **Estimated gain of the converter while operating at fixed 59.5 V output voltage. The converter cannot deliver the full peak power at the maximum output voltage while operating at 400 V input: the gain of the converter is limited in this region**

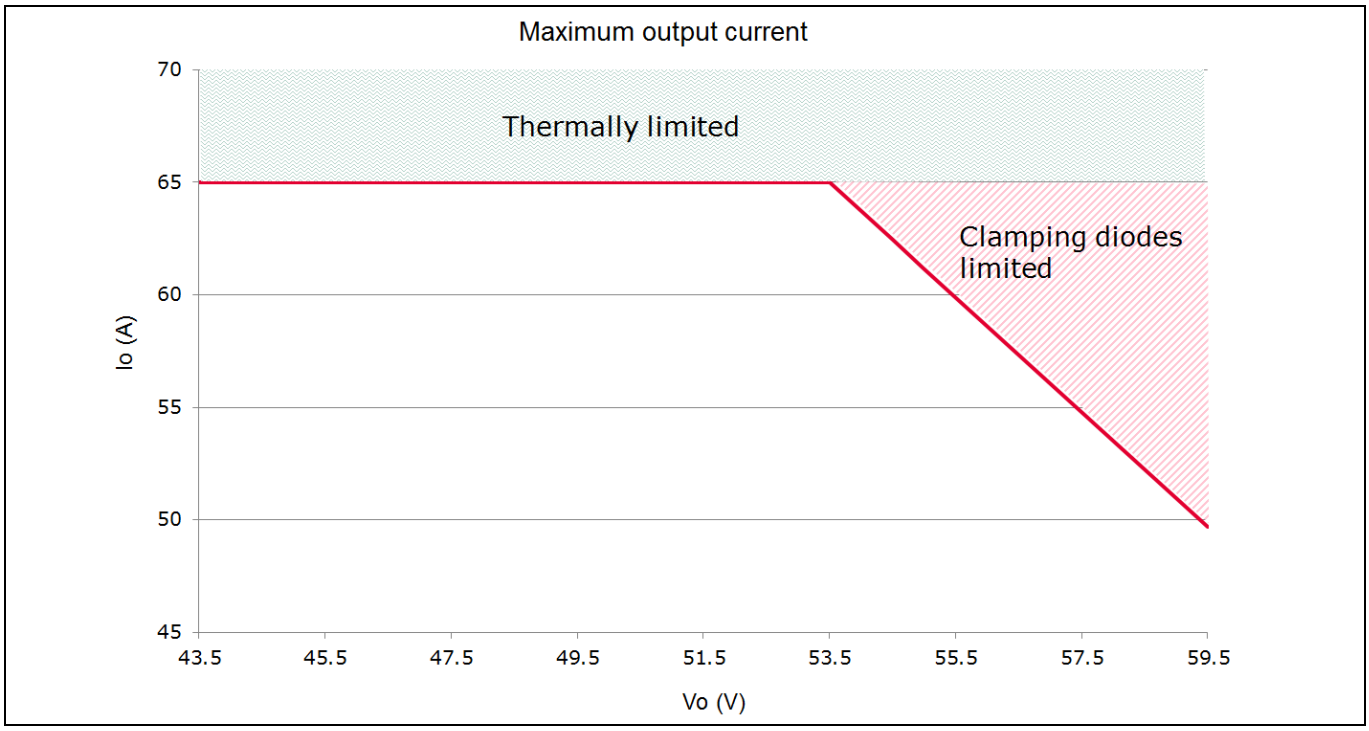

Figure 11 **Adaptive burst threshold. The switching frequency increases and the range extends at the lower output voltages (buck operation, above resonance)**

1.1.4 Converter gain in buck operation

For output voltages under the nominal (lower than 51 V) the converter operates in the buck region, or the so-called above resonance (Figure 12).

At light loads the gain of the converter becomes almost flat. Moreover, in reality the gain can actually rise again for increasing switching frequencies due to circuit parasitics and phenomena not considered in the FHA [3]. There are several state-of-the-art solutions for the extension of the minimum gain range in LLC. The solution adopted in this design is burst mode operation.

The burst mode threshold is given by the maximum switching frequency, which is adapted in the control of this converter to the different output voltages Figure 13. The adaptive threshold is required because of the dissimilar switching frequency ranges at the different output voltages (Figure 7, Figure 8 and Figure 9).

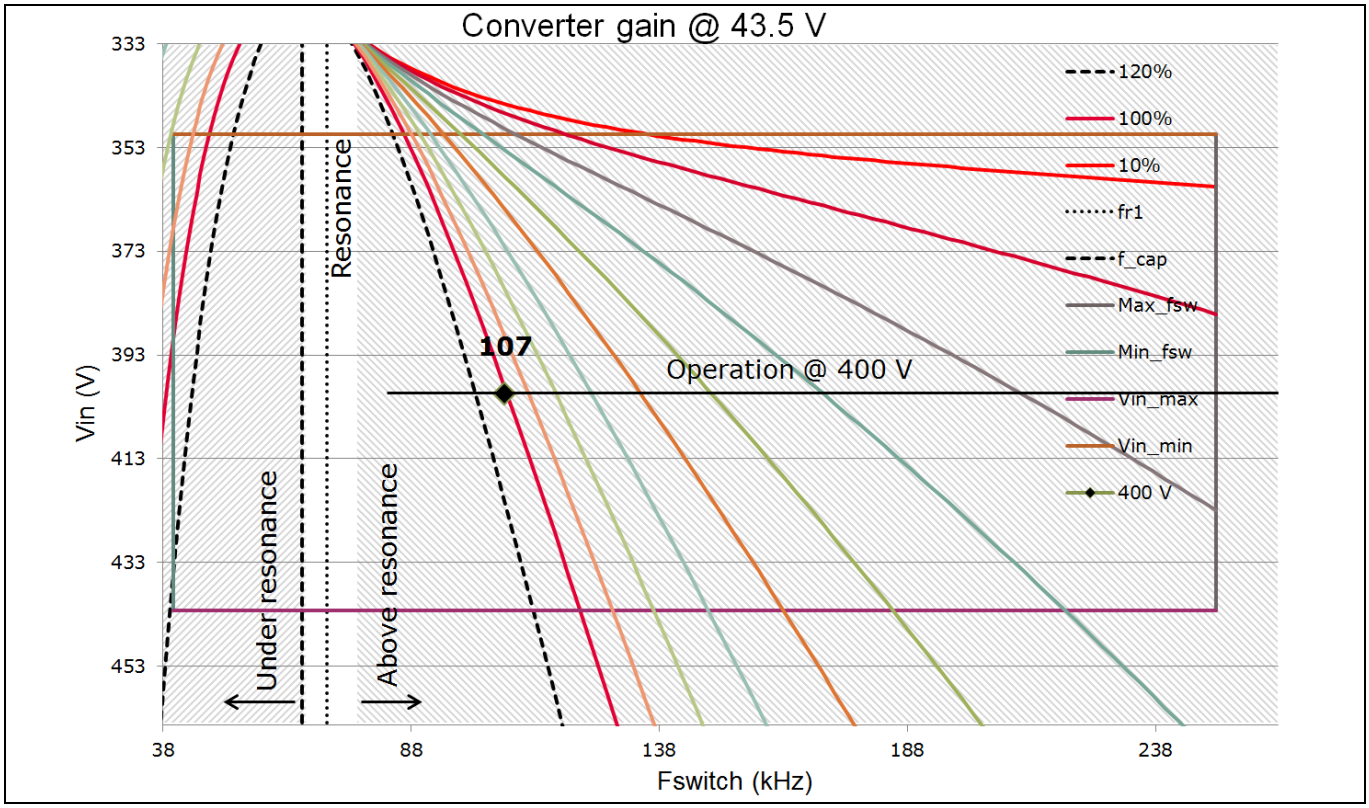

Figure 12 Estimated gain of the converter while operating at fixed 43.5 V output voltage. The frequency span is very wide. However, special control techniques can be used to reduce the gain and maintain the regulation at light loads

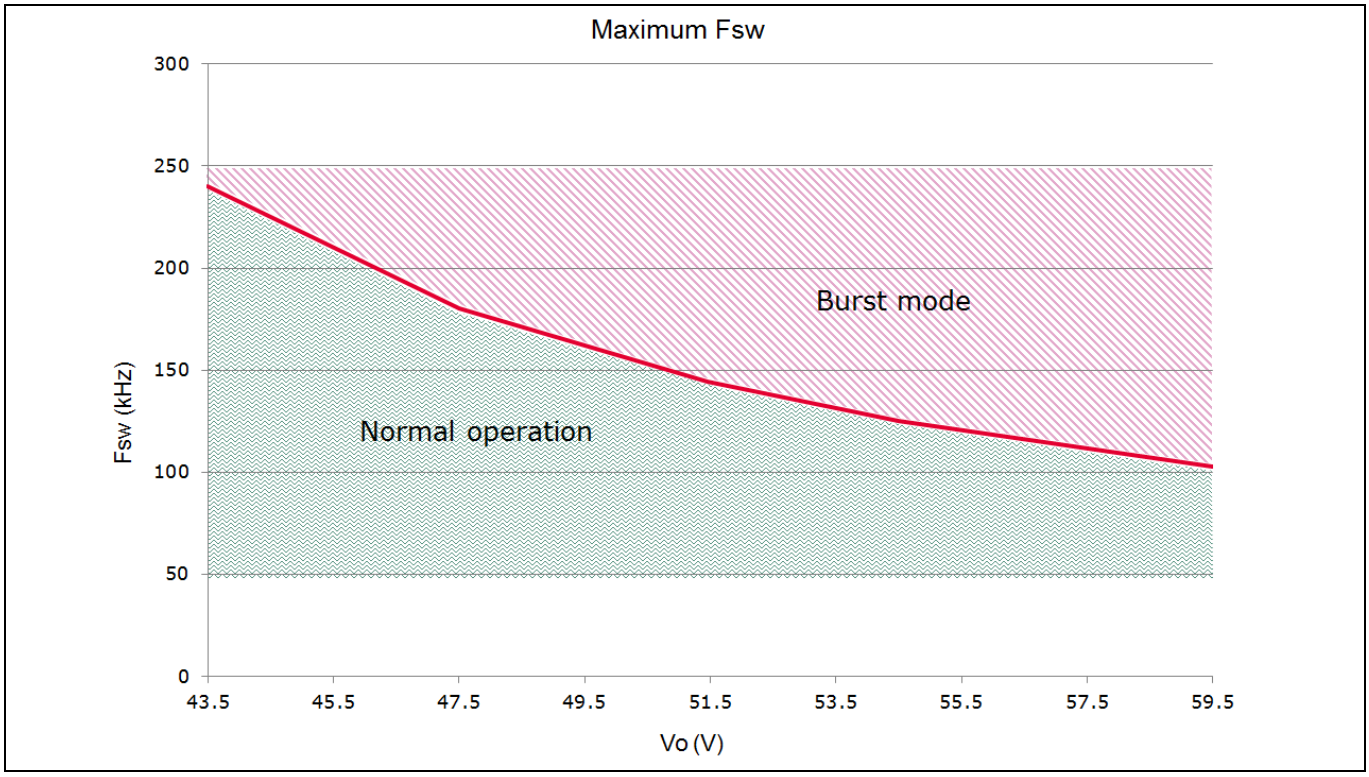

Figure 13 **Adaptive burst threshold. The switching frequency increases and the range extends at the lower output voltages (buck operation, above resonance)**

1.2 Board description

Figure 14 shows the placement of the different components on the 3300 W LLC HB DC-DC converter. The outer dimensions of the board, designed without enclosure, are 205 mm x 100 mm x 40 mm, which results in a power density in the range of 4 W/cm^3 (66 W/in^3).

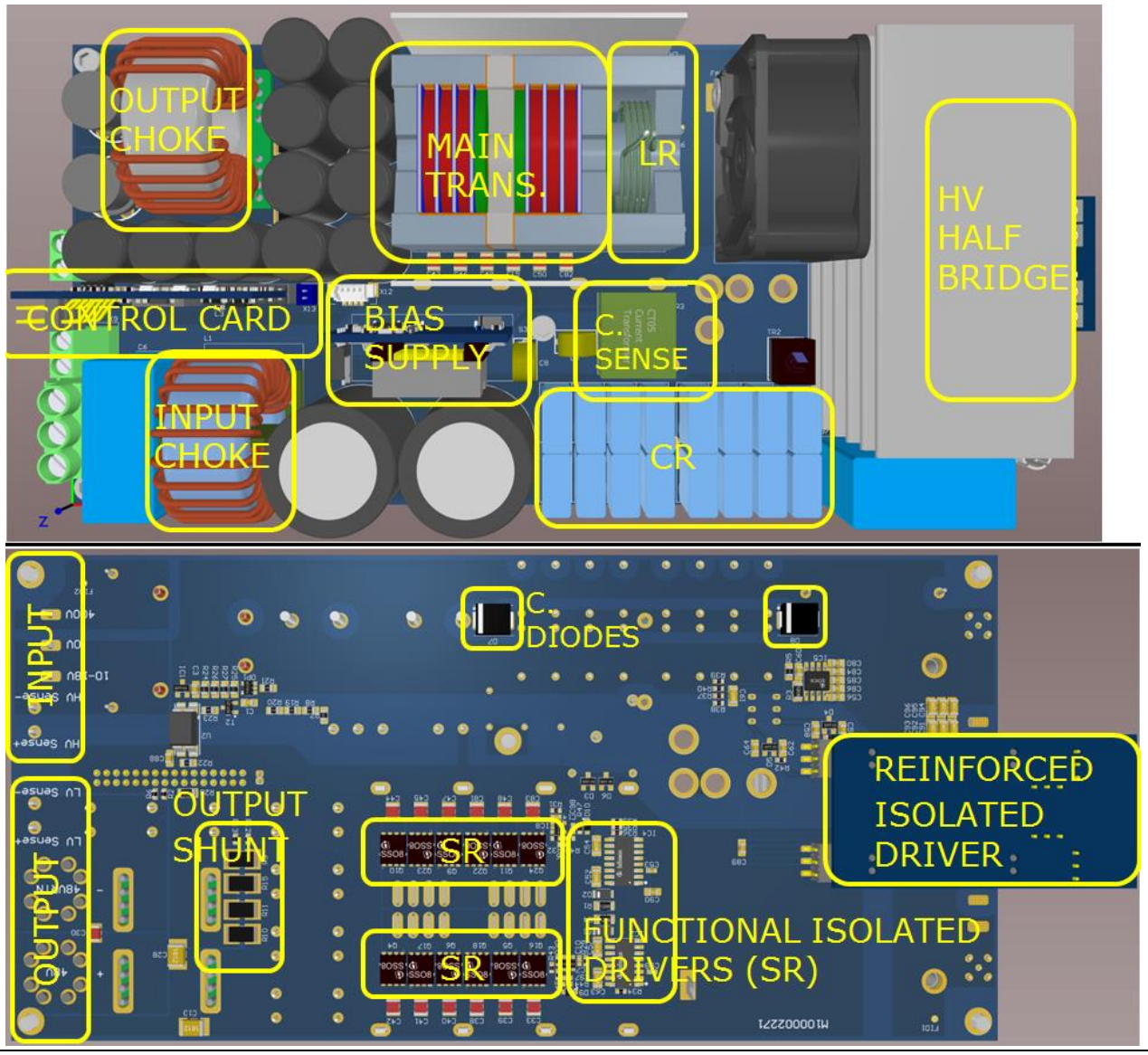

Figure 14 **Placement of the different sections in the 3300 W LLC HB with Infineon 600 V CoolMOS™ CFD7 and 80 V OptiMOS™ 5. Current Sense (CS), resonant inductor (LR), Synchronous Rectifiers (SR), clamping diodes (C. DIODES), resonant capacitor (CR)**

The estimated overall distribution of losses of the converter along the load proves the main transformer and the resonant inductance as the main sources of loss (Figure 15). The semiconductors, both the 600 V CoolMOS™ CFD7 and the 80 V OptiMOS™ 5, which are their best-in-class performing parts, exhibit very low and good balanced switching, driving and conduction losses.

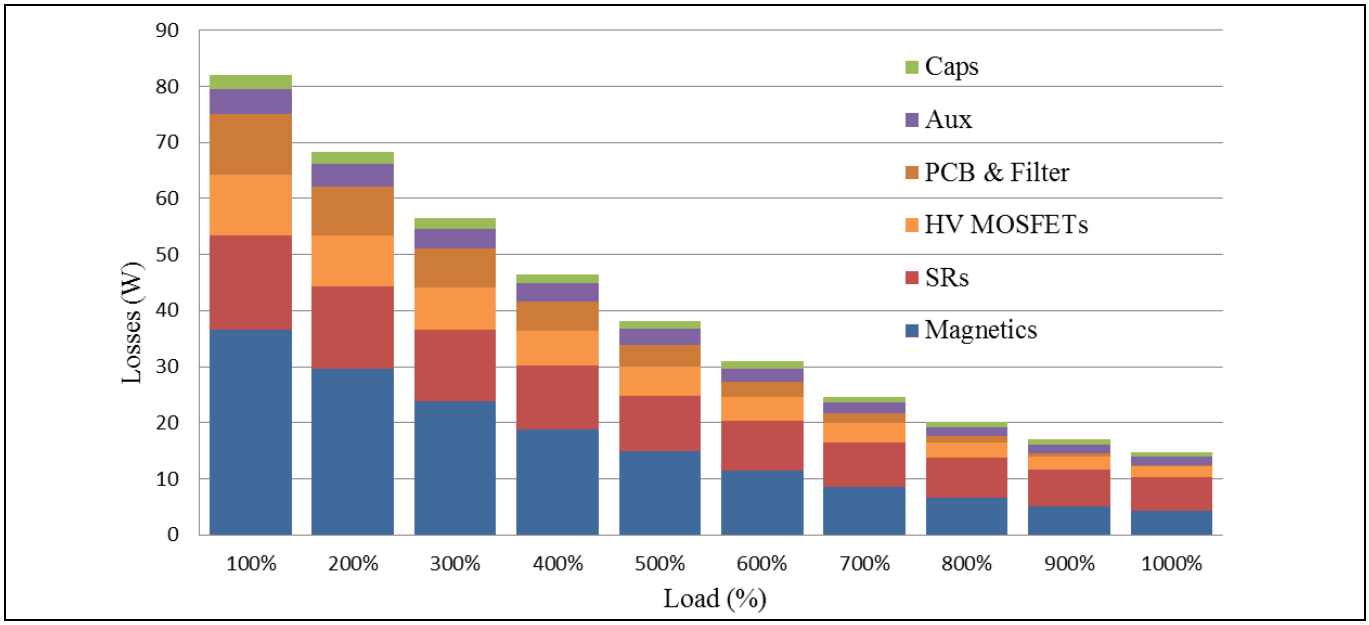

Figure 15 **Overall losses breakdown of the 3300 W LLC HB along the load range of the converter. Estimated at nominal conditions: 400 V input and 51.5 V output**

1.3 600 V CoolMOS™ CFD7 in LLC

IPW60R018CFD7 stands for the 18 mΩ 600 V CoolMOS™ CFD7 in TO-247 package, the latest and best-performing fast body diode device from Infineon.

IPW60R018CFD7 has a low loss contribution along all load ranges and exhibits a good balance of conduction, driving and switching losses at the 50 percent load point, becoming the right device and $R_{DS(on)}$ class when optimizing for the highest peak efficiency at that point (Figure 16).

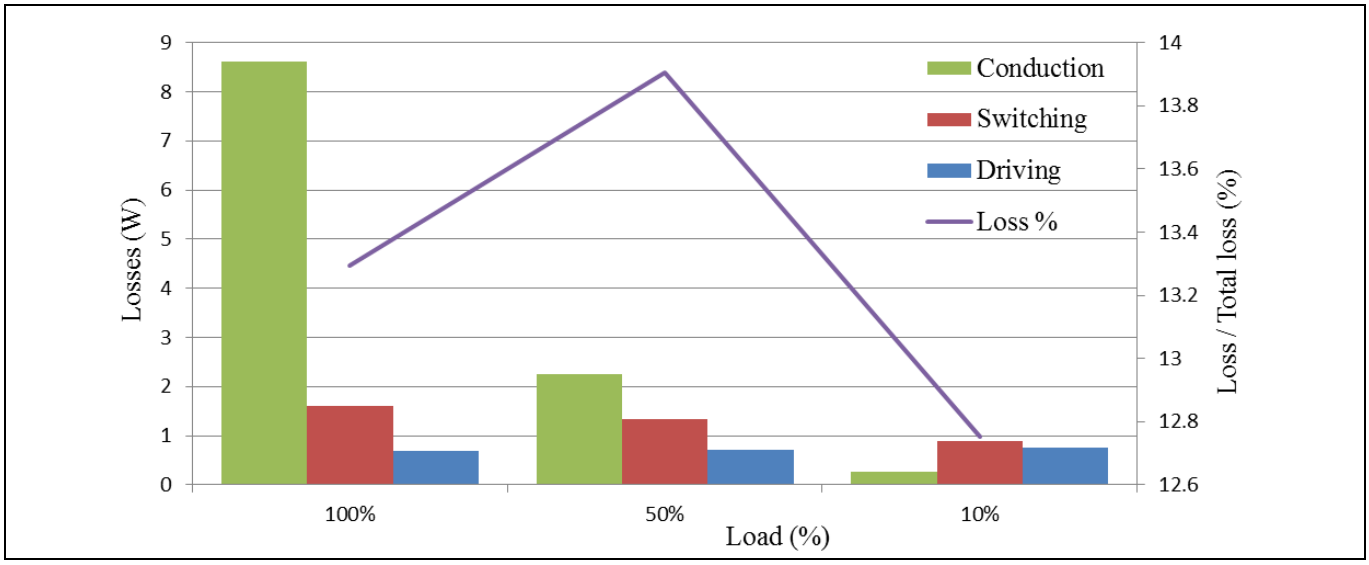

Figure 16 **IPW60R018CFD7 loss distribution along load in the 3300 W LLC HB. Absolute MOSFETs loss and its relative proportion to the total losses is given as a percentage. Estimated at nominal conditions: 400 V input and 51.5 V output**

The proposed driving circuitry includes an external turn-on resistor (10 Ω) in series to a medium-power Schottky diode BAT165, and an external turn-off resistor (2.5 Ω) also in series to a BAT165 (Figure 17).

The external turn-on resistor (10 Ω) plus the embedded MOSFET gate resistance (RG) has little or no impact on turn-on losses under ZVS and keeps dv/dt and di/dt under control in the event of eventual hard-switched turn-on transitions (soft-start or no-load operation).

The external turn-off resistor helps to dampen voltage ringing in the gate driving loop of the MOSFET at high current turn-off transitions. Moreover, the external turn-off resistor does not have an impact on the switching losses thanks to the early channel shut-down mechanisms in CoolMOS™ where the dv/dt is limited by the external capacitance and the resonant current (4).

Note: *The 3300 W LLC HB was designed as a testing platform for HV devices. The drivers are mounted on a daughter card, which eases their replacement and a variety of driving alternatives.*

In summary the 600 V CoolMOS™ CFD7 achieves incomparable switching performance in all load conditions (Figure 16).

$$\begin{cases} \frac{dv}{dt_1} = \frac{\left(V_{plateau} - V_{driver}\right)}{C_{dg} R_{g,OFF}} = \frac{V_{plateau}}{C_{dg} R_{g,OFF}} & , \frac{dv}{dt} \leq \frac{dv}{dt_1} \\ \frac{dv}{dt_2} = \frac{I_{OFF}}{2C_{oss,tr}} & , \frac{dv}{dt} \leq \frac{dv}{dt_2} \end{cases}$$

Equation 4

Replacing the parameters in the equation (4) with the data from IPW60R018CFD7, the values of the proposed driving circuit and the maximum expected turn-off current in the application (I_{OFF}) we obtain the results in (5). In these conditions the turn-off speed would be limited by the driving path and not entirely lossless.

$$\begin{cases} \frac{dv}{dt_1} = \frac{5.25\ V}{75\ pF\ 2.5\ \Omega} \approx 28\ \frac{V}{ns} \\ \frac{dv}{dt_2} = \frac{30\ A}{722\ pF} \approx 41.5\ \frac{V}{ns} \end{cases}$$

Equation 5

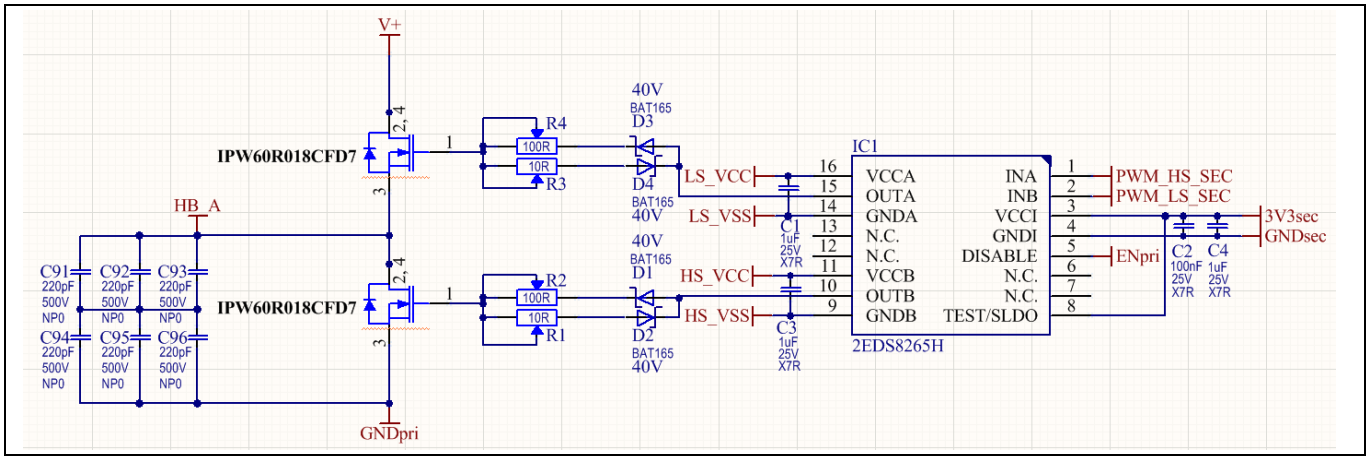

Figure 17 **Proposed driving circuit for the 3300 W LLC HB including the additional external capacitance for linearization and early channel shut-down range extension**

However, it is a standard practice to add external ceramic capacitors to linearize the MOSFET switching behavior and extend the early channel shut-down range. In the proposed circuit we have added 330 pF that must be considered in the previous analysis (6). In this case the turn-off transition becomes limited by the resonant charge of the output capacitance of the switches and can be considered entirely lossless.

$$\begin{cases} \frac{dv}{dt_1} = \frac{5.25\ V}{75\ pF\ 2.5\ \Omega} \approx 28\ \frac{V}{ns} \\ \frac{dv}{dt_2} = \frac{30\ A}{(722+330)\ pF} \approx 28.5\ \frac{V}{ns} \end{cases}$$

Equation 6

The supply of the High-Side (HS) driver has been realized by an auxiliary supply built around the single-channel Infineon driver 1EDI20N12AF (Figure 18). The proposed biasing circuit self-oscillates, generating a fixed-frequency square wave, which is fed to a safety isolated transformer and rectified afterward in two separate secondary windings. Each of the secondary windings supplies one of the HB safety isolated channels of the 2EDS8265H driver: one for the HS MOSFET and other for the low-side MOSFET.

The supply voltage of the HB driver is given by the auxiliary transformer turns ratio (13:16, stepping up) and the input voltage of the auxiliary supply circuit. The input of the auxiliary supply can be selected between the internally available 12 V (resulting in approximately 14.8 V maximum driving voltage) or supplied externally from 10 V up to 18 V.

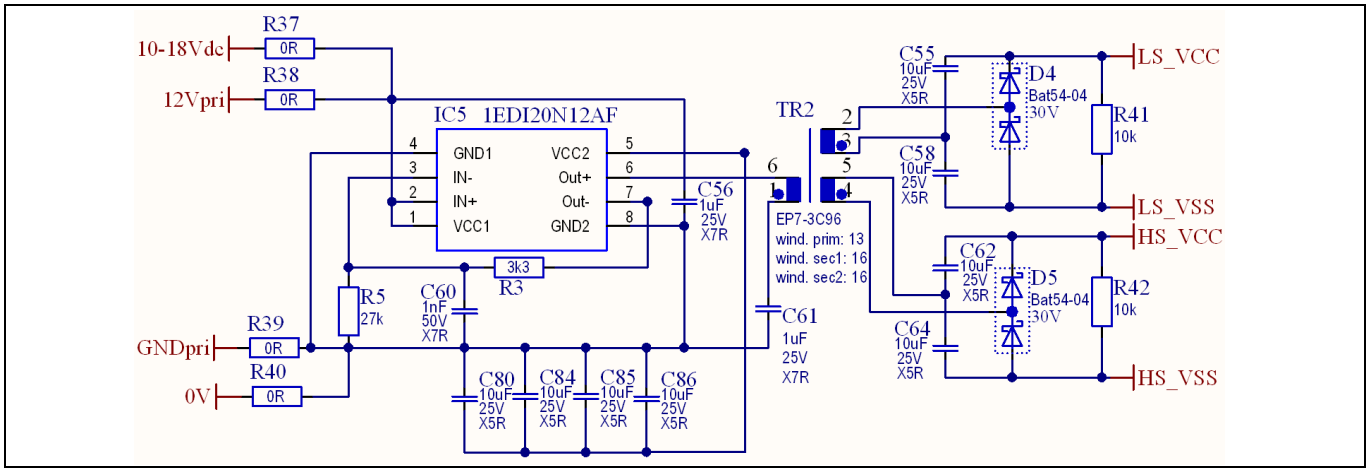

Figure 18 **Proposed isolated supply for the driving of the HV HB devices. The supply can be set to 12 V from the internal supply or within a 10 V up to 18 V range from an additional external supply**

1.3.1 600 V CoolMOS™ CFD7 $R_{DS(on)}$ comparison

The 600 V CoolMOS™ CFD7 current portfolio in TO-247 package (Figure 19) ranges from 170 mΩ (maximum) to the best-in-class 18 mΩ (minimum).



600 V CoolMOS™ CFD7 SJ MOSFETs

$R_{DS(on)}$ [Ω]	TO-247	$R_{DS(on)}$ [Ω]	TO-247
18	IPW60R018CFD7	90	IPW60R090CFD7
31	IPW60R031CFD7	105	IPW60R105CFD7
40	IPW60R040CFD7	125	IPW60R125CFD7
55	IPW60R055CFD7	145	IPW60R145CFD7
70	IPW60R070CFD7	170	IPW60R170CFD7

Figure 19 $R_{DS(on)}$ portfolio for 600 V CoolMOS™ CFD7 in TO-247.

For this design IPW60R018CFD7 was chosen as the best performance compromise between 100 percent, 50 percent and 10 percent load points. However, other $R_{DS(on)}$ could be used to achieve a different distribution of losses whenever there is interest in increasing performance at a different working point of the converter.

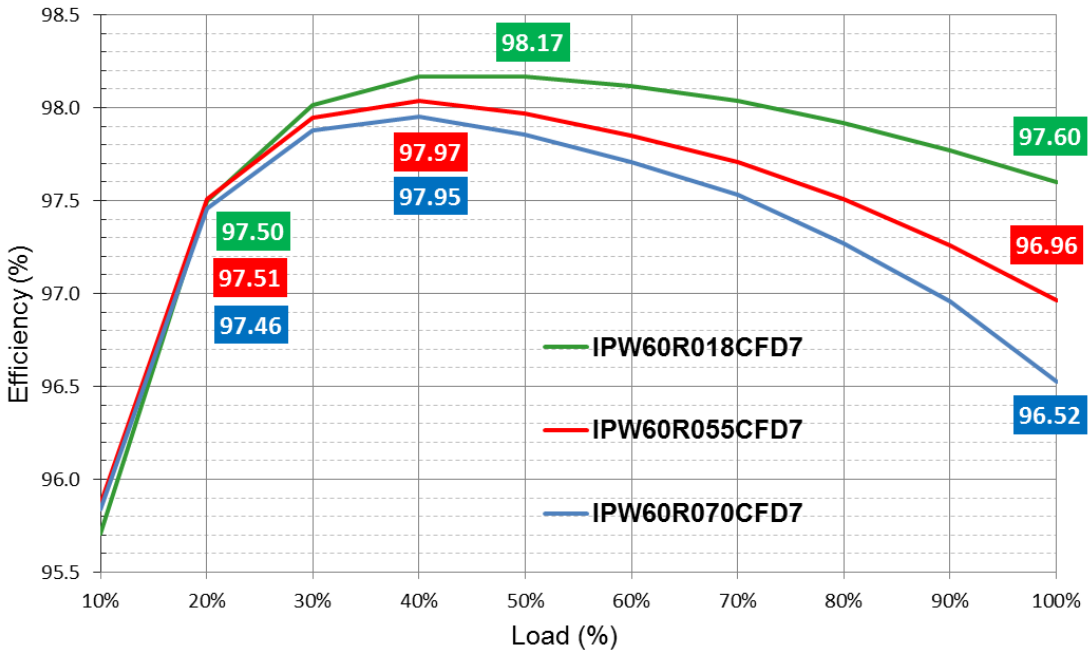

Figure 20 Estimated efficiency of the 3300 W LLC HB with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output

For example, in Figure 20 and Figure 21 we present an estimated performance comparison for three different $R_{DS(on)}$ available in the 600 V CoolMOS™ CFD7 portfolio: IPW60R018CFD7 (device currently on the design), IPW60R070CFD7 and IPW60R055CFD7 (in between the two previous $R_{DS(on)}$).

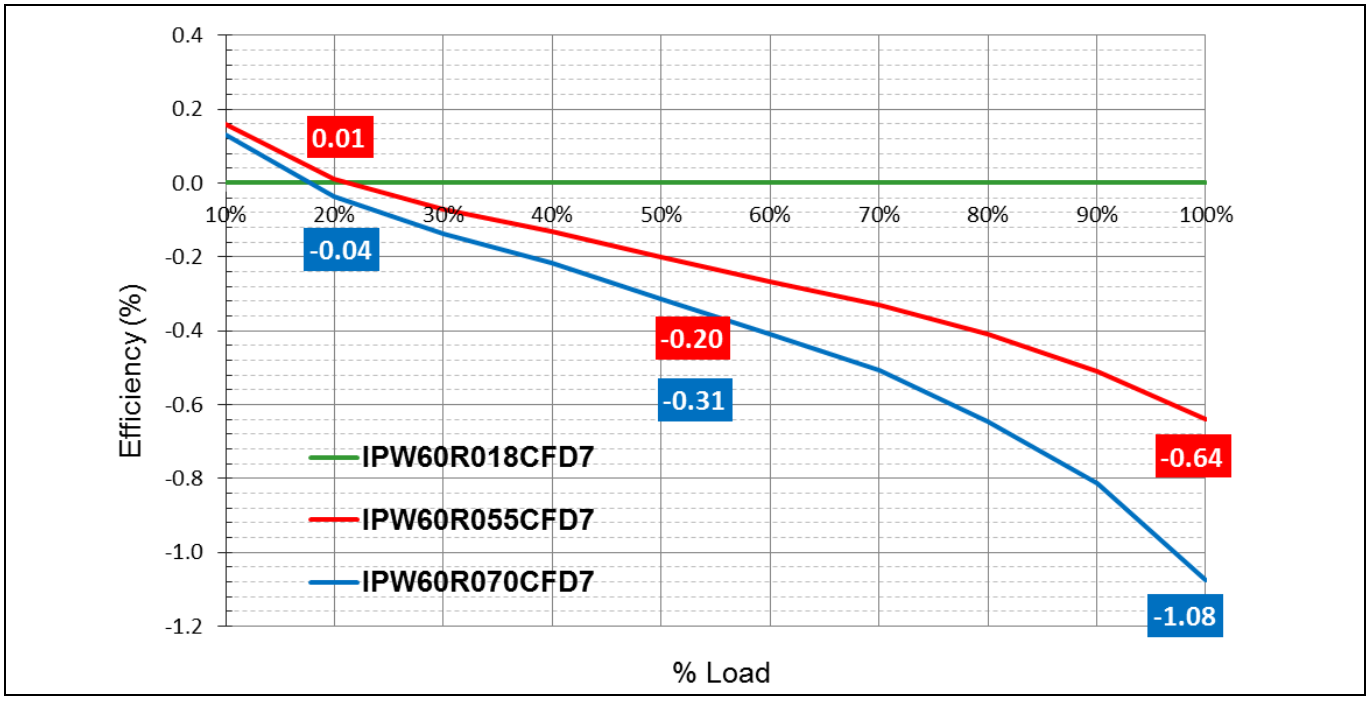

Figure 21 **Differential estimated efficiency of the 3300 W LLC HB with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output**

In Figure 22 the estimation of losses at three main working points and how they balance for the three different $R_{DS(on)}$ values can be seen. Although the difference in losses at 50 percent and 10 percent is small in comparison to the difference in losses at 100 percent of load, the impact on efficiency is still noticeable, as can be observed in Figure 21. The steep change on the differential efficiency comparison between 20 percent and 10 percent is due to the partial loss of full ZVS at 10 percent and the proportionally higher $E_{oss(er)}$ values for each of the $R_{DS(on)}$ values.

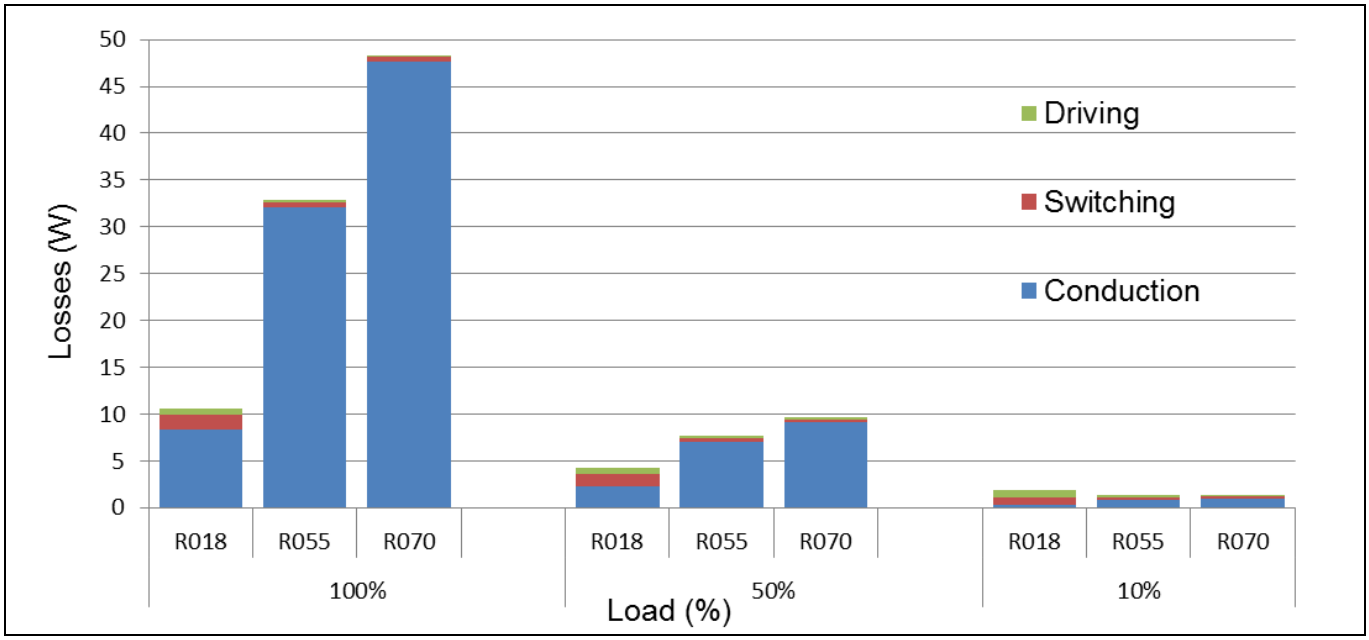

Figure 22 **Estimated distribution of losses of the 3300 W LLC HB with different 600 V CoolMOS™ CFD7 $R_{DS(on)}$ in TO-247. Estimated at nominal conditions: 400 V input and 51.5 V output**

1.3.2 CoolMOS™ CFD7 to CFD2 comparison

CoolMOS™ CFD2 current portfolio in TO-247 packages ranges from 660 mΩ (maximum) to the best-in-class 41 mΩ (minimum).

For a fair comparison between technologies we compare IPW65R041CFD with a maximum $R_{DS(on)}$ of 41 mΩ against IPW60R040CFD7 with a maximum $R_{DS(on)}$ of 40 mΩ.

Thanks to the Figure of Merit (FOM) of CFD7 technology we have the benefit of lower $R_{DS(on)}$ at mid and full load without any compromise in switching losses at light or medium loads. Thanks to this, the converter performs better in all load ranges when comparing CFD7 against CFD2 devices (Figure 23 and Figure 24).

Figure 25 shows the distribution of losses for the main working points. The lower input and output charge of CFD7 makes it have lower switching and driving losses for an equivalent and even for a lower $R_{DS(on)}$.

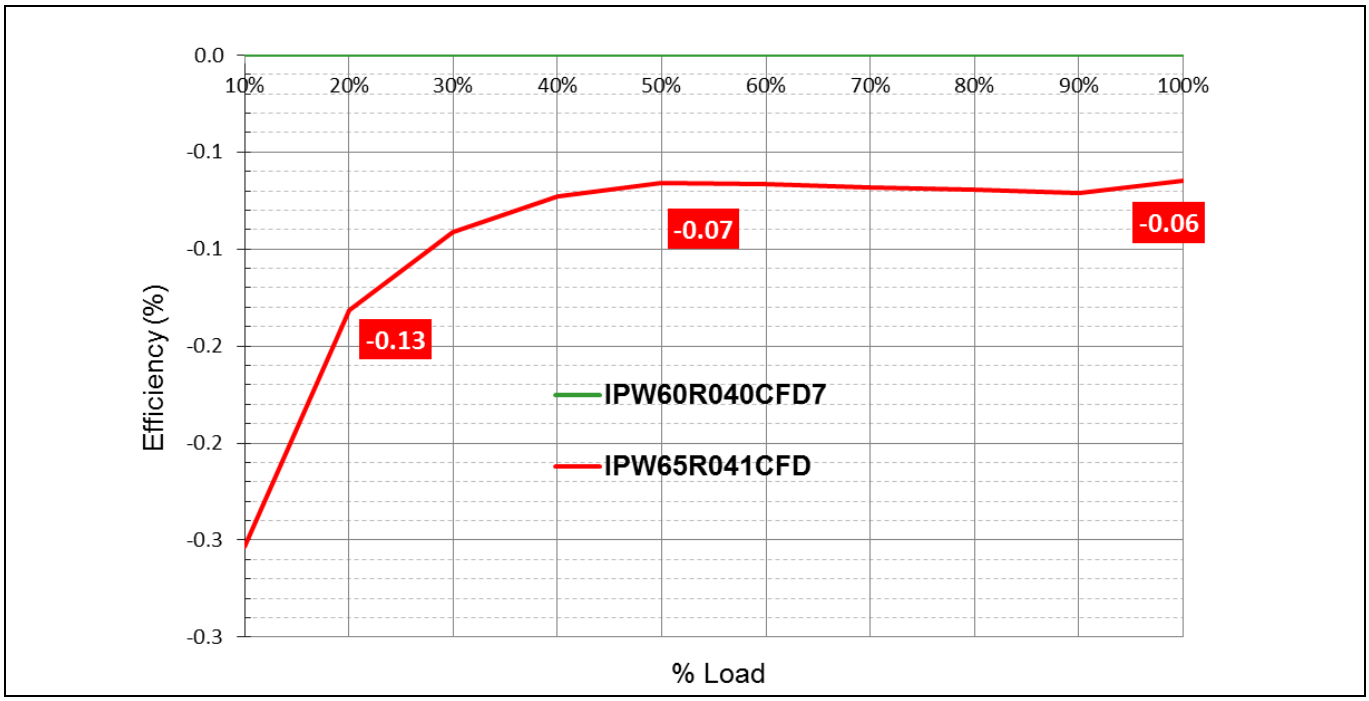

Figure 23 Differential estimated efficiency of the 3300 W LLC HB with different CoolMOS™ fast body diode technologies. Estimated at nominal conditions: 400 V input and 51.5 V output

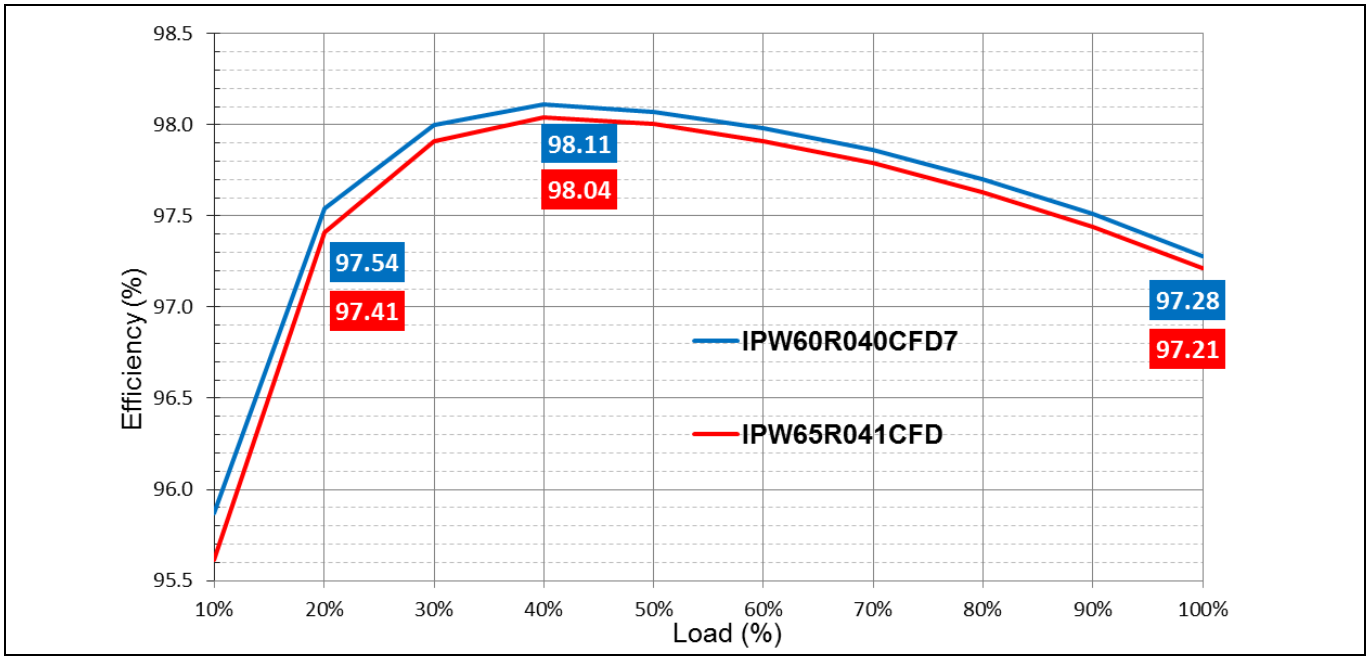

Figure 24 **Estimated efficiency of 3300 W LLC HB with different CoolMOS™ fast body diode technologies. Estimated at nominal conditions: 400 V input and 51.5 V output**

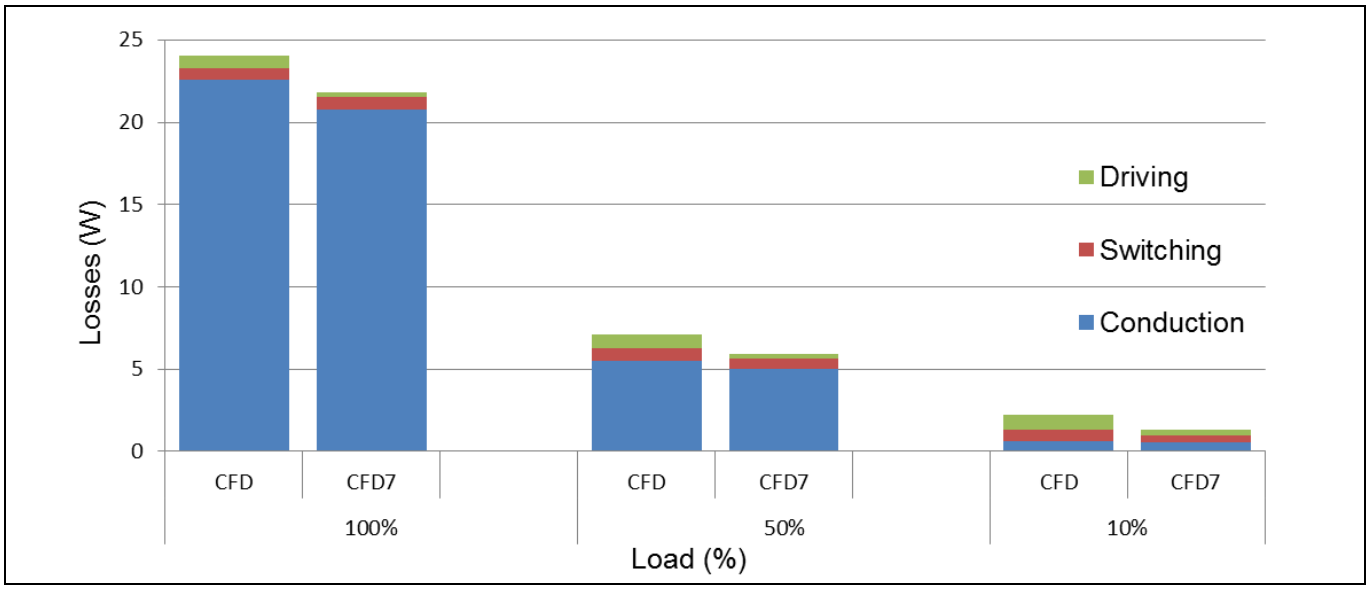

Figure 25 **Estimated distribution of losses of 3300 W LLC HB with different CoolMOS™ fast body diode technologies. Estimated at nominal conditions: 400 V input and 51.5 V output**

1.4 Transformer

The transformer has a conversion ratio of 15 primary turns to four secondary turns with a planar-like construction. The core geometry is PQ35/28 with ferrite material DMR95 from DMEGC manufacturer. Primary winding has been realized with triple-insulated Litz wire made of 175 strands x 0.1 mm diameter from Pack Litz Wire. Secondary winding is made of parallel tinned copper plates of 0.5 mm thickness.

The resonant inductance is stacked on the side of the transformer, also realized with half of a PQ35/28 core and six turns of 175 x 0.1 mm Litz wire (of the same type as for the primary-side winding of the transformer).

Note: The main transformer structure actually comprises two parallel transformers integrated with the external resonant inductance. This enables realization of the required low L_m with several small gaps instead of a single large one.

Figure 26 shows an estimated loss distribution of the full stacked magnetic structure at nominal conditions. Notice that the transformer core loss is nearly constant along the load (apart from the material temperature dependence) due to the small switching frequency variation operating near resonance.

Maximum flux peak depends on the load and the operating point of the converter. It was estimated well below saturation flux density of the chosen core material (DMR95 from DMEGC) under any of the normal working conditions of the converter. An advantage of the integrated magnetic construction is the partial cancelation of flux within the parallel transformers and between the external resonant inductance and the main transformer block (Figure 27).

The winding technique and geometry of the core achieves good coupling (low leakage inductance, in the order of 500 nH) with relatively low intra- and inter-winding capacitances (in comparison to a full planar realization). This enables low drain voltage overshoot on the secondary-side devices and optimum voltage class selection. Moreover, the interleaving of primary and secondary windings achieves nearly full window utilization and minimizes proximity losses. A detailed description of the construction can be seen in Figure 28.

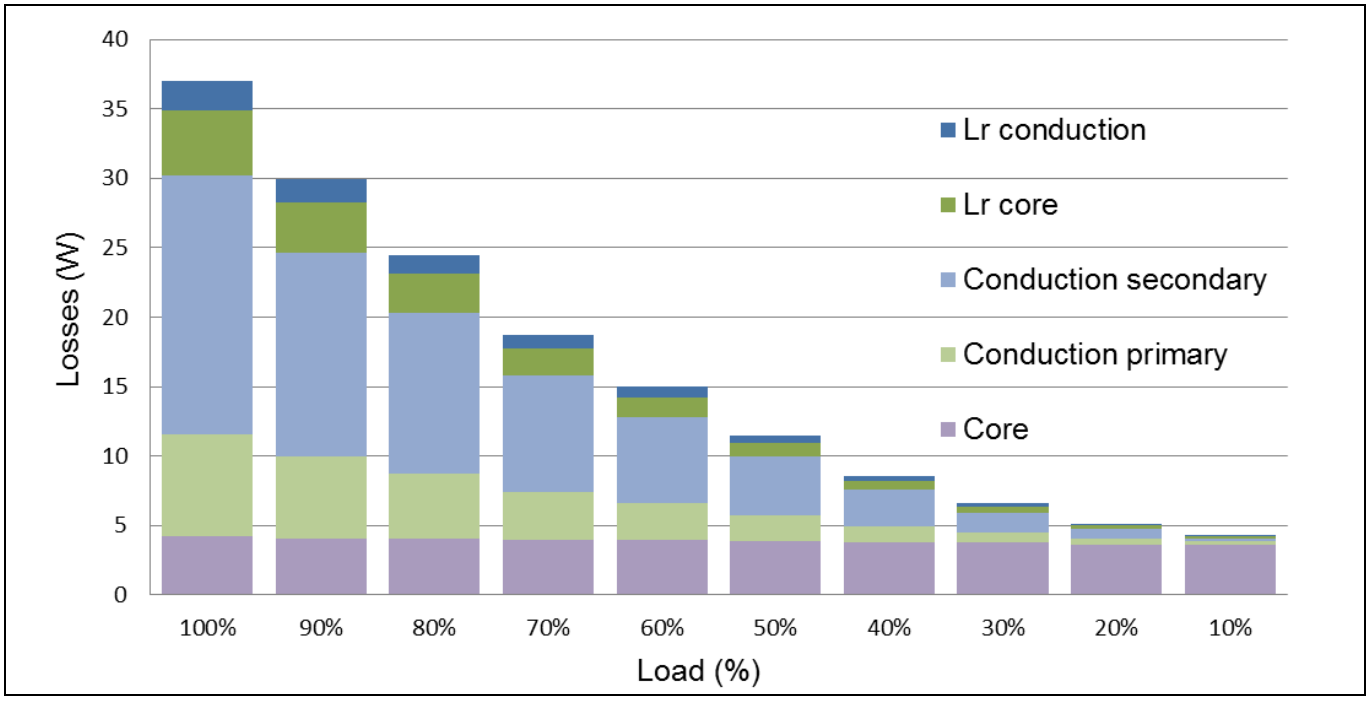

Figure 26 Estimated distribution of losses of stacked magnetic structure: transformer and resonant inductance (Lr). Estimated at nominal conditions: 400 V input and 51.5 V output

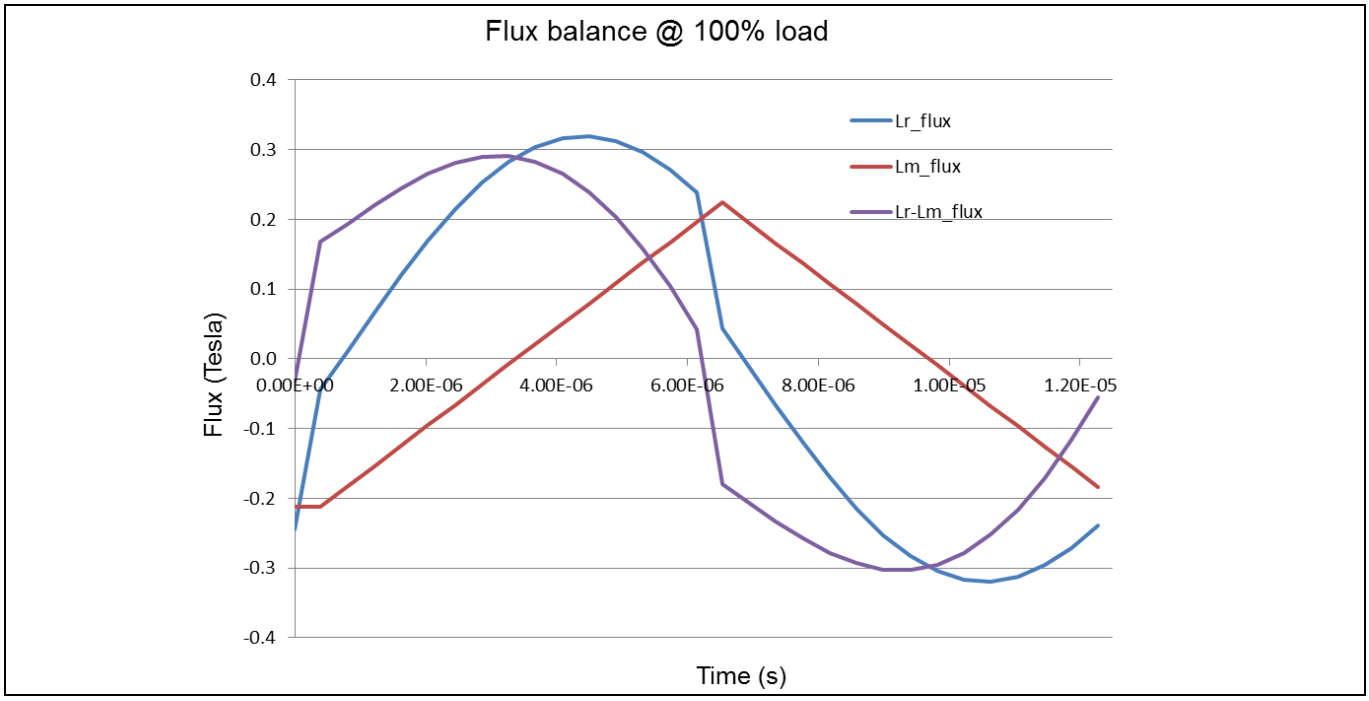

Figure 27 **Estimated distribution of flux at full load and nominal operating conditions: 400 V input and 51.5 V output**

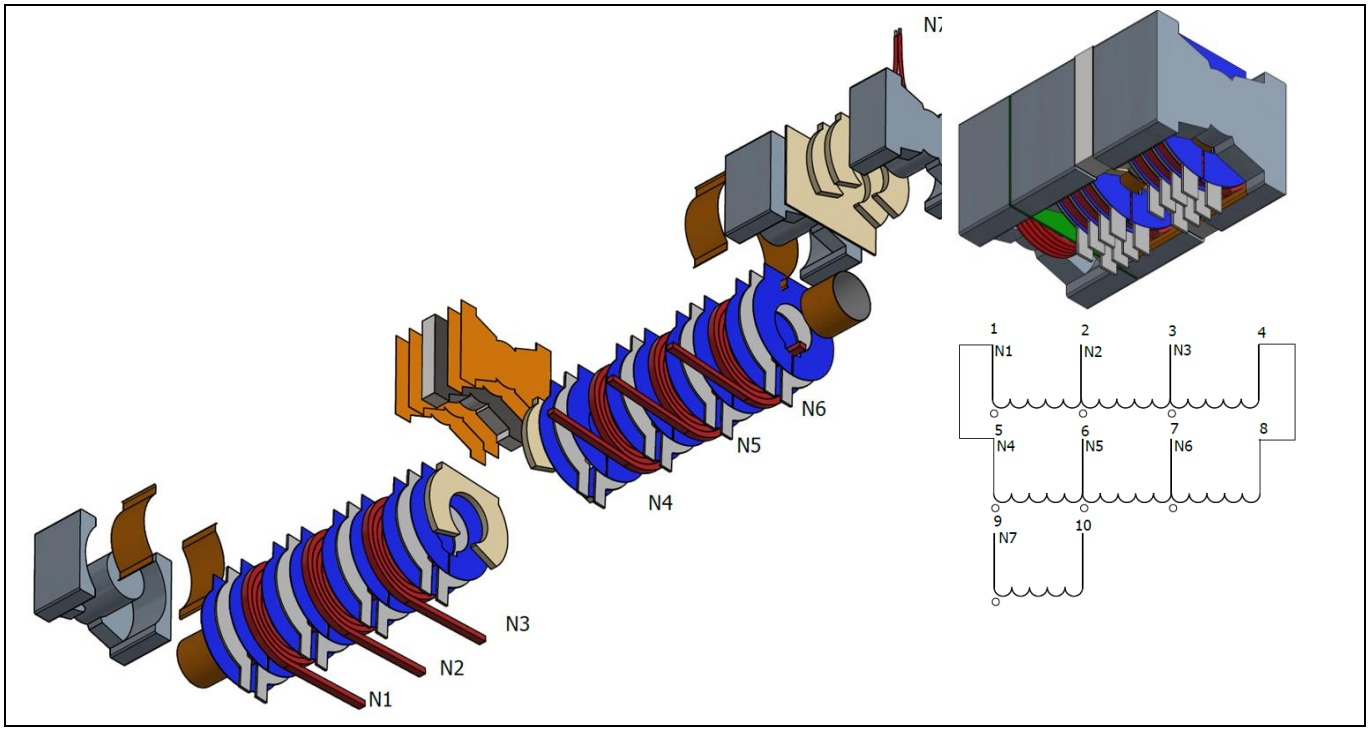

Figure 28 **Main transformer and external resonant inductance. Mechanical drawing and simplified schematic. N1, N2, N3, N4, N5, and N6 correspond to primary side windings. N7 corresponds to the secondary side copper plates**

1.5 Cooling solution

The proposed cooling solution in this design comprises an off-the-shelf aluminum heatsink for the HV HB devices and a set of two custom copper plates for the SR LV devices (Figure 29). The construction of the transformer, where secondary-side winding is made out of copper plates, also constitutes part of the secondary-side heatsink for the LV devices.



Figure 29 Heatsinks for HV HB devices and LV secondary devices in a partially assembled 3300 W LLC HB converter board

A single fan blows air into the integrated magnetics and the secondary-side heatsinks. The same fan extracts air from the primary-side heatsink, which does not have much of an airflow requirement because of the heavily oversized cooling for the HV devices.

Note: The 3300 W LLC HB was designed as a testing platform for HV devices. The heatsink is oversized to accommodate diverse $R_{DS(on)}$ and packages.

The fan speed is modulated along the load for best overall system efficiency (see Figure 30). Because of the high efficiency of the converter, little cooling effort is required at light and medium loads.

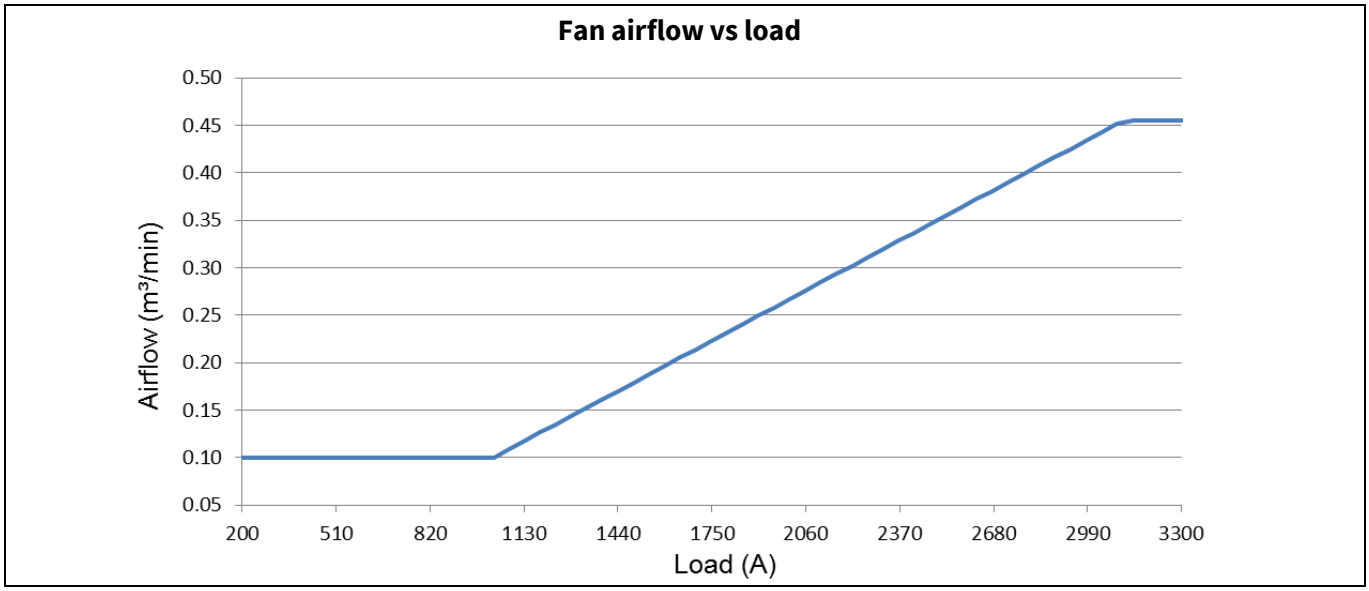

Figure 30 **Fan airflow control along the converter load (estimated from fan datasheet and assuming the fan is working with low pressure)**

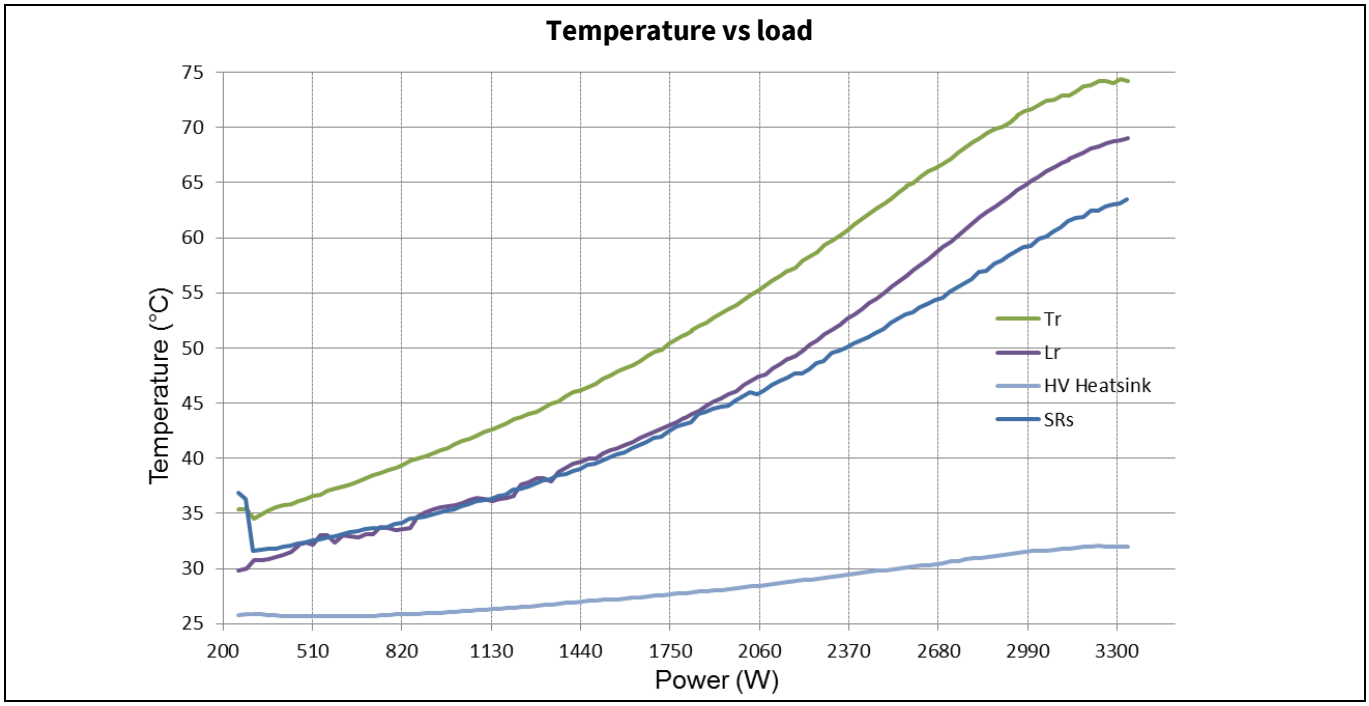

Figure 31 **Measured temperatures on the 3300 W LLC HB converter at 25°C room temperature and without enclosure. Tr: Transformer. Lr: Resonant Inductance**

The temperatures of the main components of the converter are plotted in Figure 31. Prior to the measurement of the temperatures the converter achieved thermal stability running for 30 minutes at 100 percent of load. Only afterward, as for the efficiency measurements, the temperatures were registered while decrementing the load.

The temperatures in Figure 31 demonstrate the effectiveness of the proposed cooling solution, besides their simple manufacture and assembly, and low cost. The cost saving enables a lower $R_{DS(on)}$ for an improved performance.

1.6 Validation set-up

For validation of the operation of the 3300 W LLC HB, the suggested set-up includes:

- HV supply capable of 400 V and at least 3500 W (when testing up to full load)
- LV electronic load (0 to 60 V), in constant current mode, capable of at least 3300 W (when testing up to full load)

Nominal input voltage of the converter is 400 V. The converter starts to operate above 375 V, turning back off under 350 V (hysteresis window), as summarized in Figure 32.

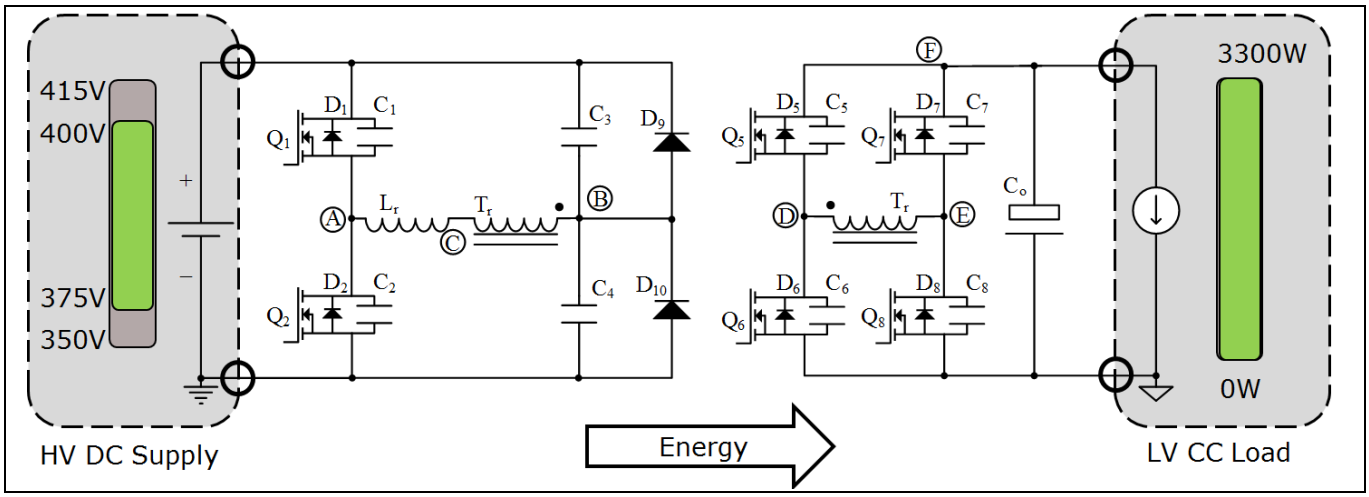

Figure 32 Recommended validation set-up

2 Experimental results

2.1 Specification and test results

This chapter describes the specifications, performance and behavior of the 3300 W LLC HB with 600 V CoolMOS™ CFD7. Table 1 summarizes the demonstrator specifications and results under several steady-state and dynamic conditions.

Table 1 Summary of specifications and test conditions for the 3300 W LLC HB

Test	Conditions	Specification
Input voltage V_{in}	350 V to 415 V	400 V nominal
Output voltage V_{ref}	59.5 V to 43.5 V	51.5 V nominal
Output power	3300 W	At nominal conditions
Efficiency test	400 V input, 51.5 V output	η_{pk} = 98.09 percent at 1650 W (50 percent of load)
Steady-state V_{out} ripple	400 V input, 51.5 V output	$\lvert\Delta V_{out}\rvert$ less than 200 mV_{pk-pk}
Dynamic response	Vref ± 1 V	5 A to 35 A, 35 A to 65 A
Input UVLO	375 V on to 350 V off	Analog hysteresis window comparator
Output UVLO, OVLO	Vref ± 3 V	Shut-down and latch
Load transient	5 A ↔ 35 A, 1 A/µs	$\lvert\Delta V_{out}\rvert$ less than 1 V_{pk}
	35 A ↔ 65 A, 1 A/µs	
OCP	68 to 75 A	Shut-down and resume
	More than 75 A	Shut-down and latch
	Output terminals in short-circuit	Detection within switching period Shut-down and latch

2.2 Performance and steady-state waveforms

2.2.1 Primary-side ZVS

The low $E_{oss(er)}$ energy of IPW60R018CFD7 results in full ZVS of the HB above 30 percent of load at nominal conditions: 400 V input and 51.5 V output (Figure 33). Moreover, IPW60R018CFD7 still achieves nearly full ZVS down to no load (Figure 34). With partial ZVS only a small part of the E_{oss} is lost. Thanks to this the switching loss contribution of the primary-side HB devices is negligible or relatively low in all working conditions of the converter (Figure 15 and Figure 16).

An additional benefit of the CoolMOS™ output capacitance profile is the reduced impact of long dead-times. The effective increase of output capacitance near the end of the transition delays the start of the body diode conduction while having a negligible impact on the switching losses (nearly no E_{oss} left at that point). Unlike other semiconductor devices, a conservative and robust, excessively long dead-time is forgiving in CoolMOS™ converters (Figure 35).

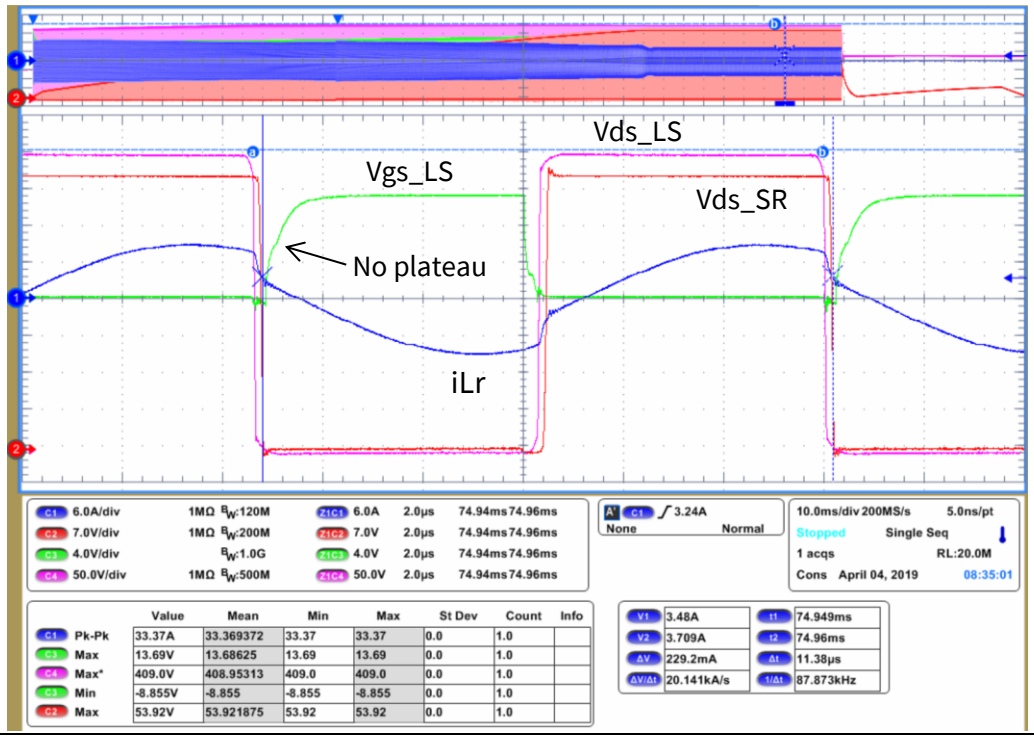

Figure 33 **Converter waveforms in the threshold of full ZVS. Operating at 20 A of load, 400 V input and 51.5 V output**

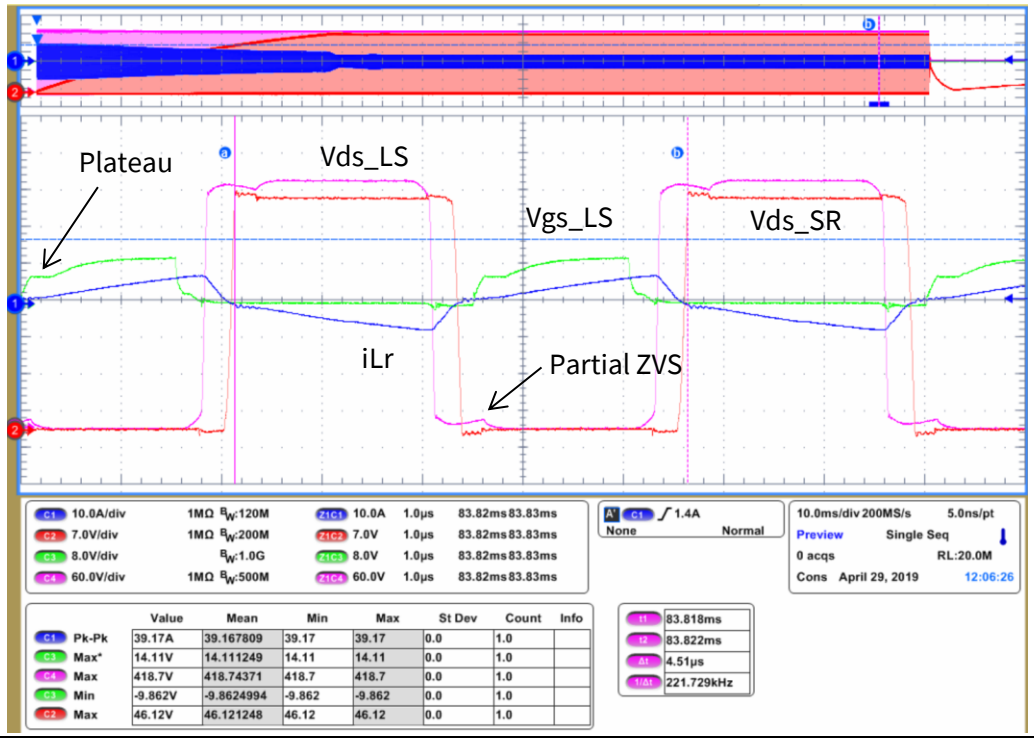

Figure 34 **Converter waveforms at light load and minimum output voltages: maximum switching frequencies, lowest case energy for ZVS transitions. Operating at 15 A of load, 400 V input and 43.5 V output**

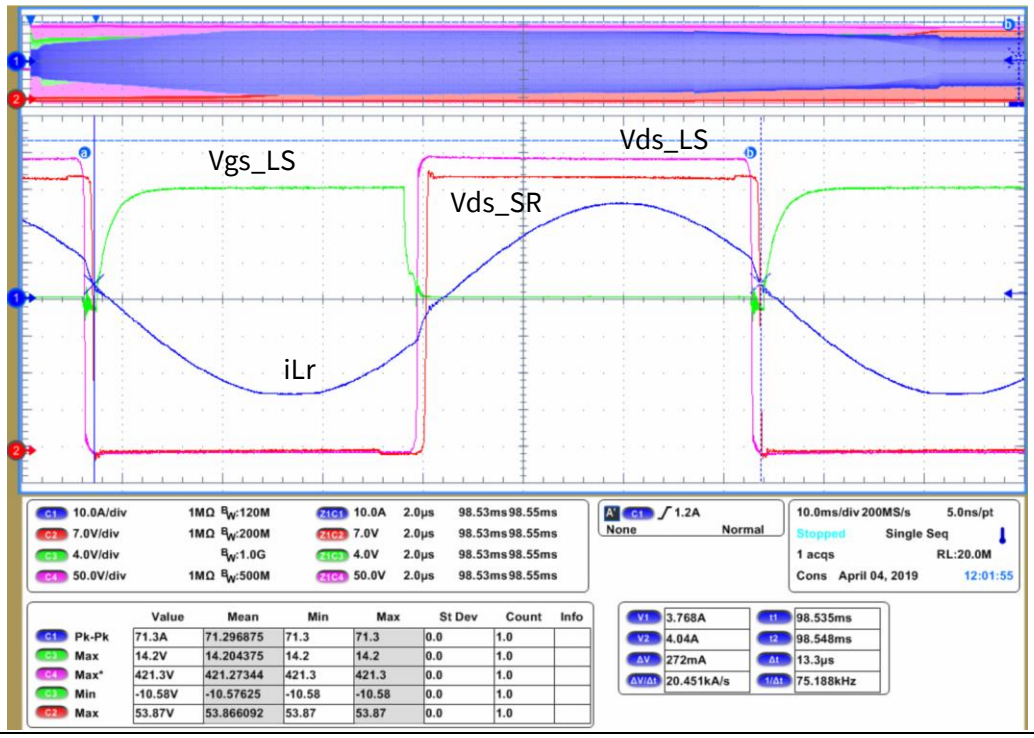

Figure 35 Converter waveforms at full load and nominal operating conditions: 65 A of load, 400 V input and 51.5 V output

The highest drain voltage overshoot in the HV MOSFETs happens at full-load start-up due to relatively high-current turn-off transition (see soft-start-up section). In these transitions the di/dt on the parasitic inductances of the MOSFET package and the layout induces certain voltage overshoot. However, the overshoot is well under the derated maximum voltage limits in any operating conditions of the converter. A commonly rated limit would be 480 V (80 percent derating of 600 V at T_j = 25°C).

2.2.2 Synchronous rectifiers

The rectifying stage has a full-bridge configuration with 24 3.7 mΩ 80 V OptiMOS™ 5 in Super SO-8 package. With the numerous packages the dissipated power can be better spread, which brings higher cooling capability and performance (lower $R_{DS(on)}$ increase due to temperature).

The FB rectifying configuration enables low losses for medium output voltage and medium output current converters. Thanks to the transformer construction with its low leakage, the optimized layout with minimal loop inductances, the OptiMOS™ 5 optimized output capacitance and low reverse recovery charges (Qrr) it is possible to use 80 V voltage-class devices with more than enough margin for the maximum drain voltage overshoot. The common 80 percent rated limit for the 80 V devices would be 64 V maximum.

The controller includes adaptive turning-on and turning-off delays for the SRs along the load for a minimum body diode conduction time. The adaptive delays reduce conduction losses and generation of Qrr, which translates into better efficiency and lower drain voltage overshoot (Figure 36).

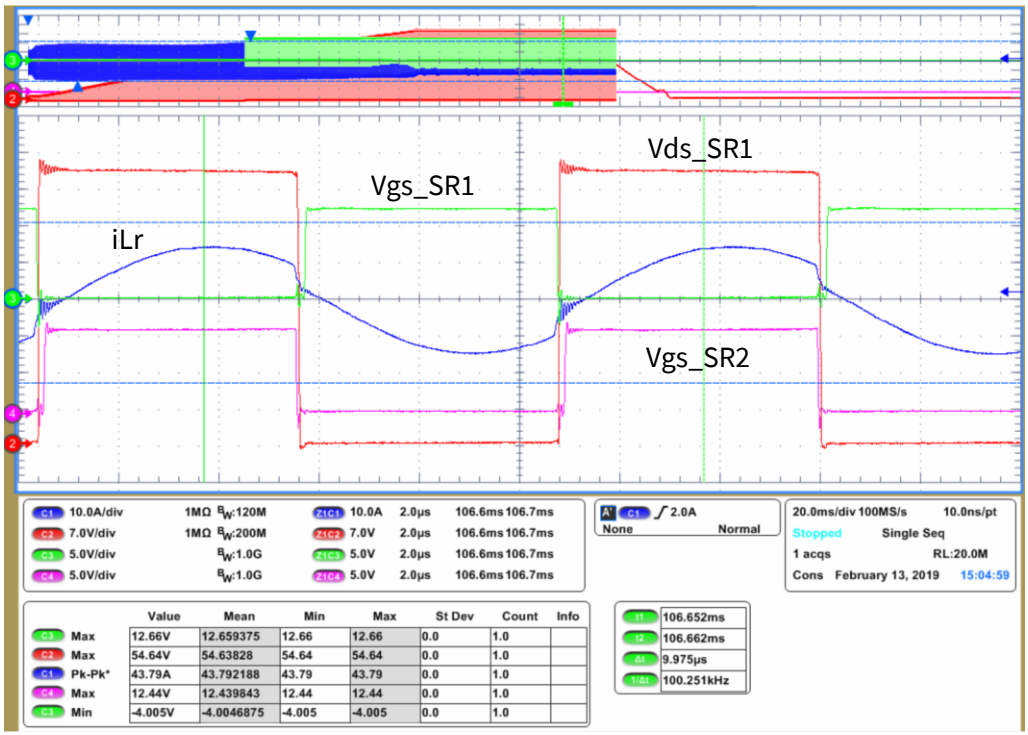

Figure 36 Gate driving pulses of the SRs near resonance. The SR turn-on is aligned to the primary-side HB. The SR turn-off is also aligned to the primary-side HB

In LLC converters, especially in wide output designs, the SRs have three main modes of operation:

- At resonance (Figure 36) the gate signals of the SRs and the primary-side HB are synchronous and have equal or similar duration
- Above resonance (Figure 37) the SRs are delayed in relation to the primary-side HB gate signals, although the pulse duration is still equal or similar. The delay between the primary and secondary corresponds to the commutation time of the secondary-side current, which also corresponds to the commutation time of the primary-side current through L_r
- Under resonance (Figure 38) the activation of the SRs is synchronous to the primary-side HB. However, the pulse duration of the SR is shorter than the one of the primary, in accordance with the natural frequency of the resonant tank

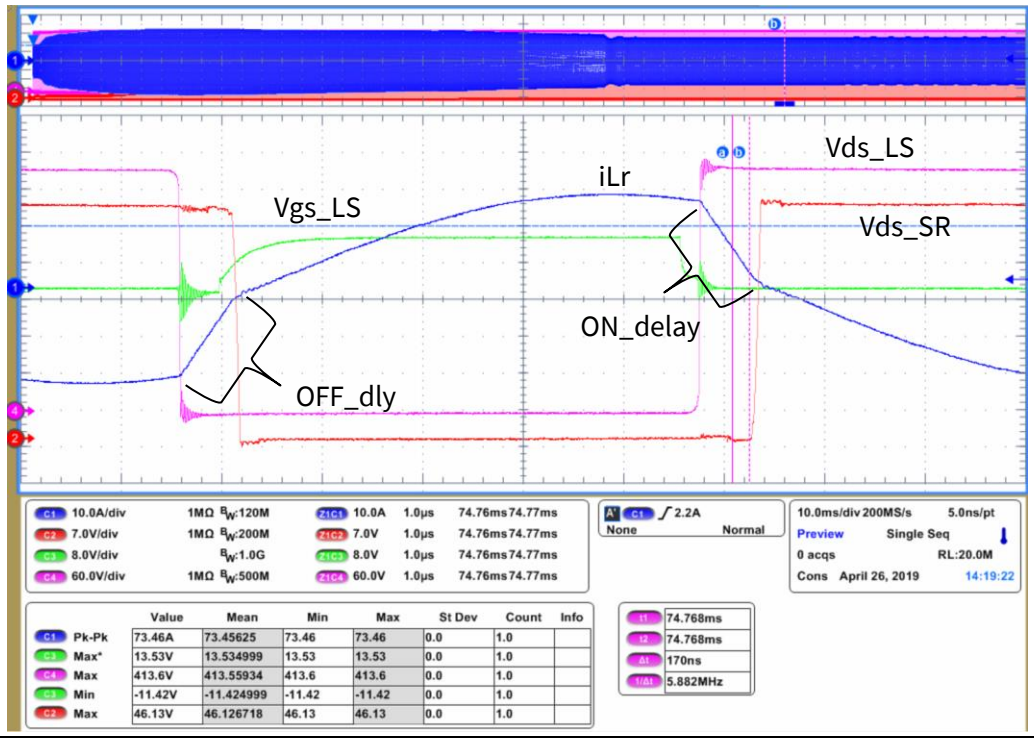

Figure 37 **Gate driving pulses of the SRs above resonance. The SR turn-on is delayed in relation to the primary-side HB. The turn-off is also delayed in relation to the primary-side HB**

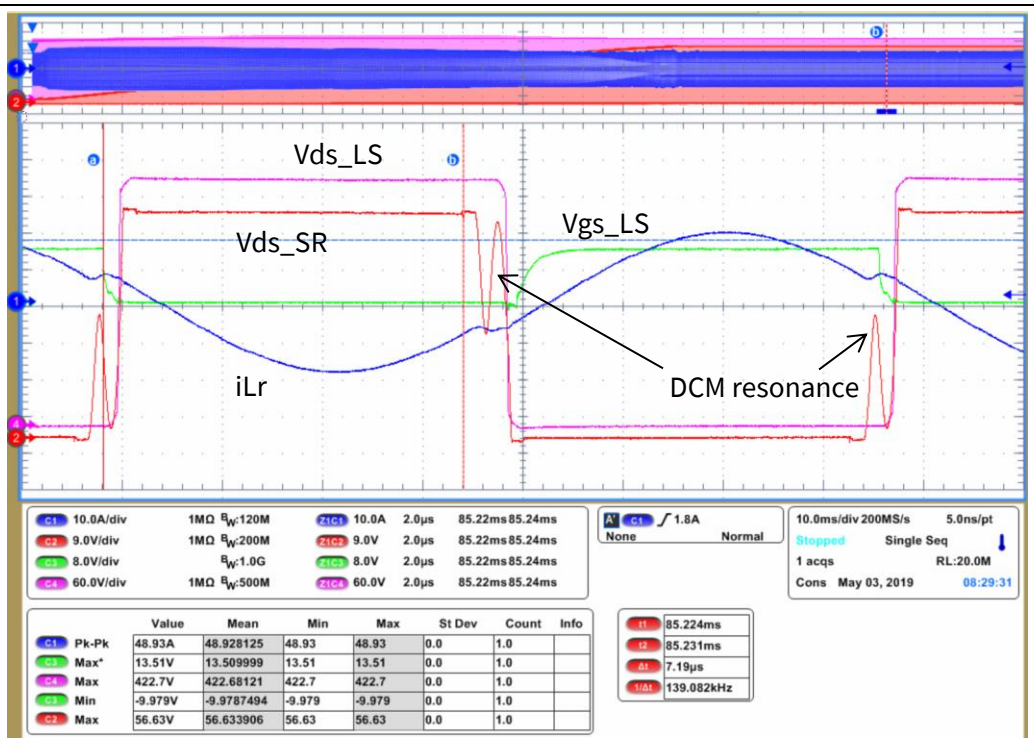

Figure 38 **Gate driving pulses of the SRs under resonance. The SR turn-on is aligned to the primary-side HB. However, the SR turn-off happens earlier than the primary-side HB**

2.2.3 Dynamic response: load jumps

The controller includes a software-implemented digital compensator designed for a bandwidth of 2 kHz with a phase margin of 45 degrees and a gain margin of 12 dB, well within the standard stability criteria requirements.

The dynamic response to load jumps (Figure 39, Figure 40, and Figure 41) correlates well with the expected response of the designed compensation, with an overshoot and undershoot within 2.5 percent of the nominal output voltage for 50 percent of load jump.

The small signal gain and phase of an LLC converter depends strongly on the load and operation point. The usual approach is to design the compensation network for the worst case and accept the lossy performance in the other conditions.

In this design an adaptive compensator was implemented with variable proportional and derivative constants along the output voltage range. This enables a more consistent response of the converter (Figure 39, Figure 40, and Figure 41).

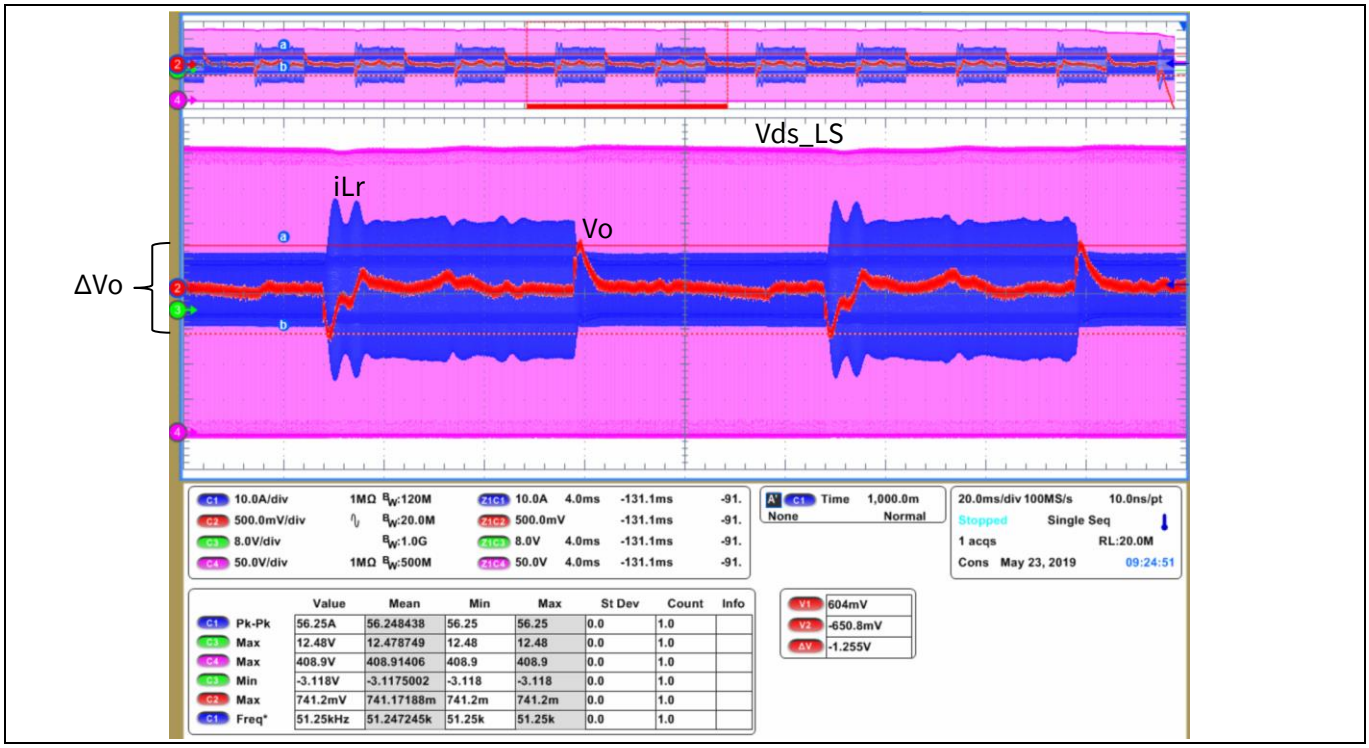

Figure 39 Load jump 5 A to 35 A at 59.5 V output. The converter gain increases and the phase margin decreases, operating under resonance

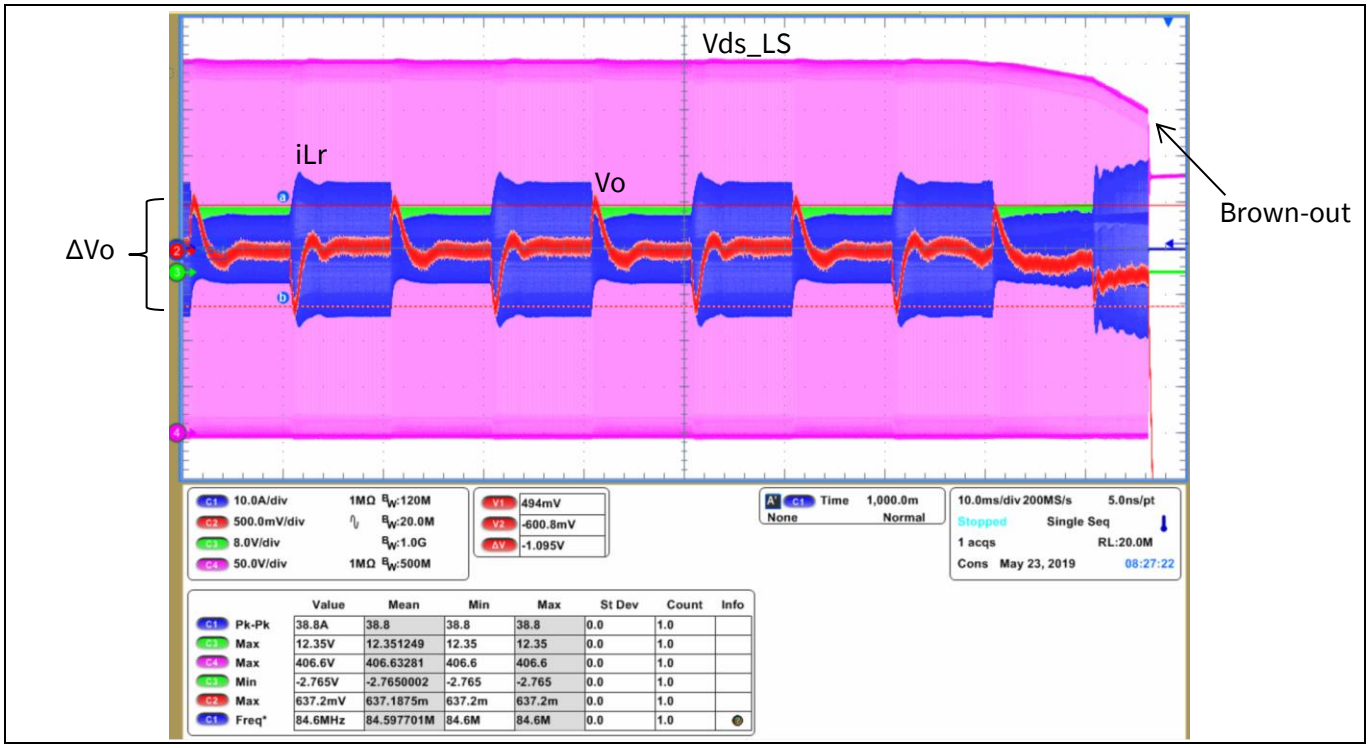

Figure 40 **Load jump 5 A to 35 A at 51.5 V output**

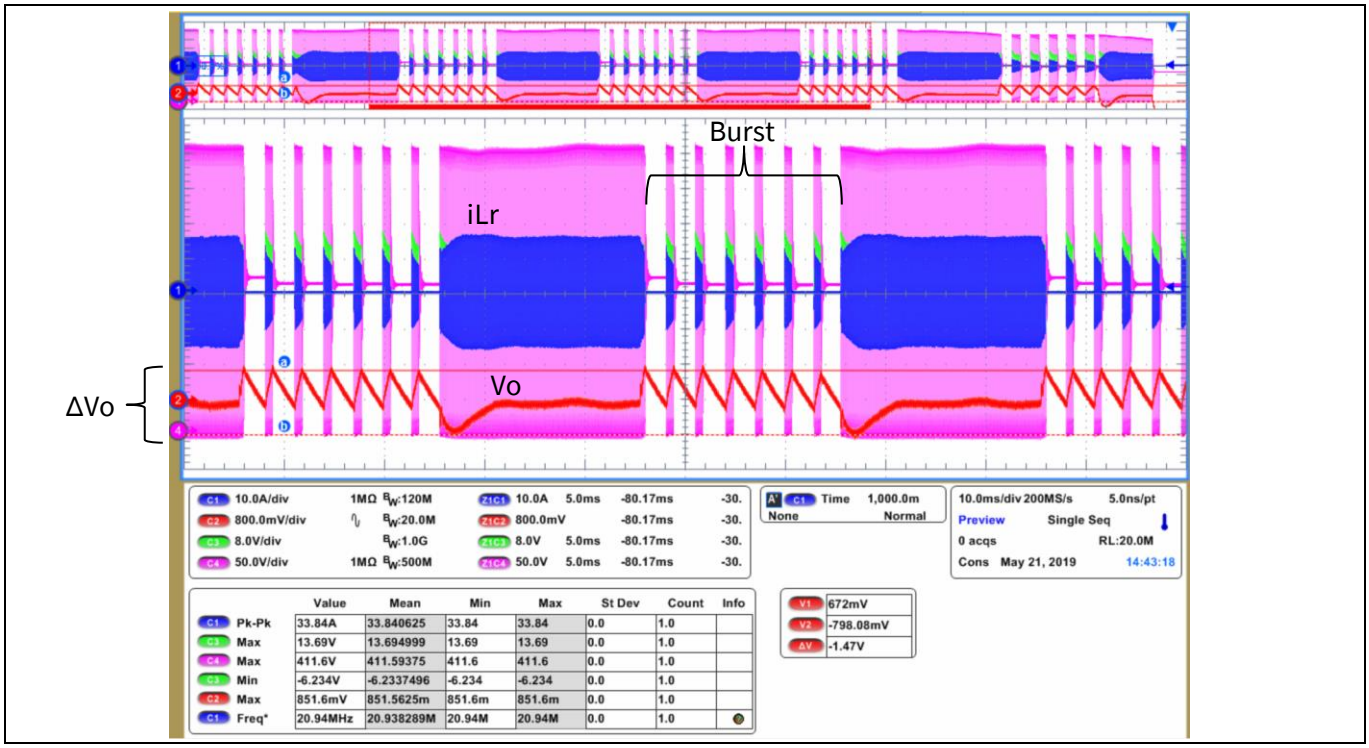

Figure 41 **Load jump 5 A to 35 A at 47.5 V output. The converter gain decreases and the phase margin increases operating above resonance. At the lower output voltages the converter operates in burst mode at light loads**

2.2.4 Soft-start-up

The controller implements a soft-start sequence to ensure the converter powers up with minimal stress (voltage and current) on any of the components. During the start-up sequence the output voltage is ramped up in closed-loop operation. The controller increments the output voltage reference within a timed sequence (Figure 42, Figure 43).

The starting pulses follow a predefined timing sequence to ensure ZVS and avoid hard commutation on the primary-side HB (Figure 44).

The maximum stress occurs on the drain and gate voltages of the primary-side devices due to the high turn-off current transitions. However, the maximum peak voltages can be controlled, increasing the turn-off resistor in the driving path. The main benefit of turning off the resistor is reduced ringing, although extreme values may increase switching losses.

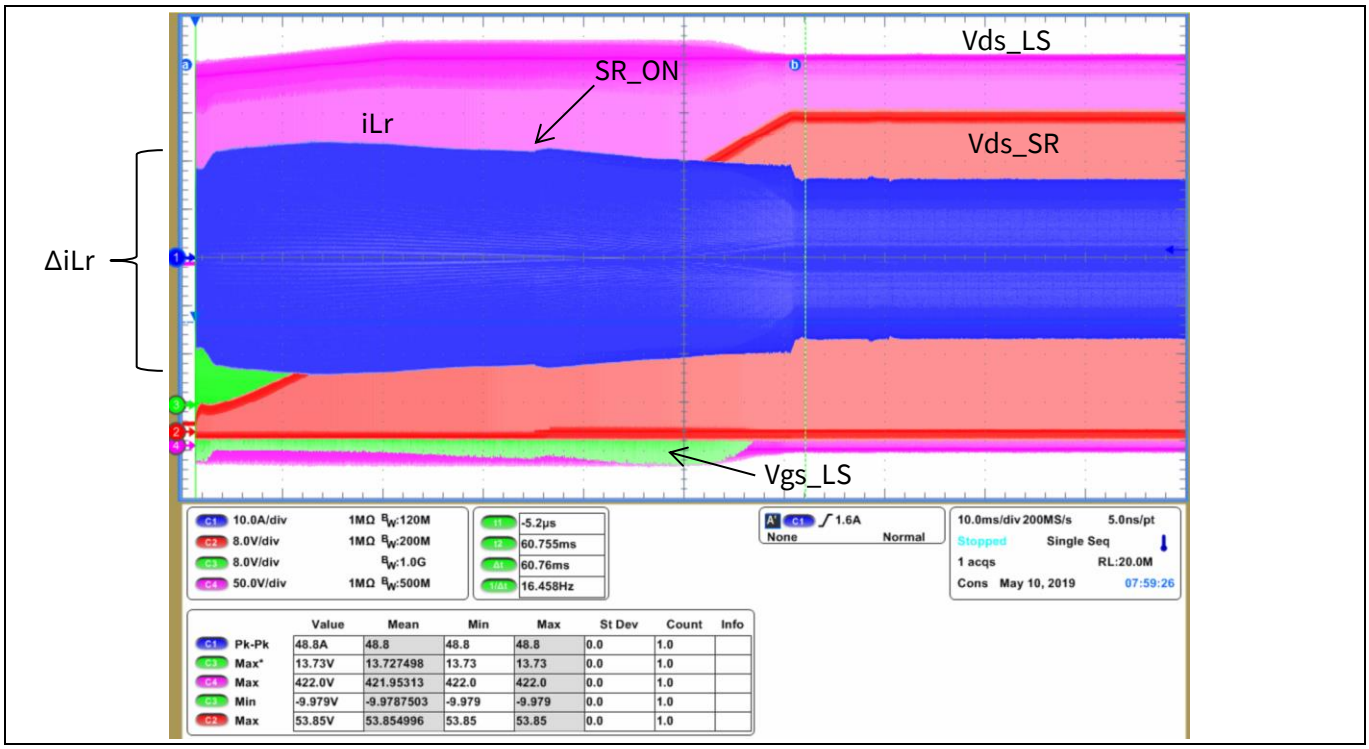

Figure 42 Start-up sequence at 40 A load, 400 V input and 51.5 V output. The maximum voltage overshoot-undershoot in drain and gate of the HV MOSFETs occurs during the start-up, where the HB operates with the highest turn-off currents

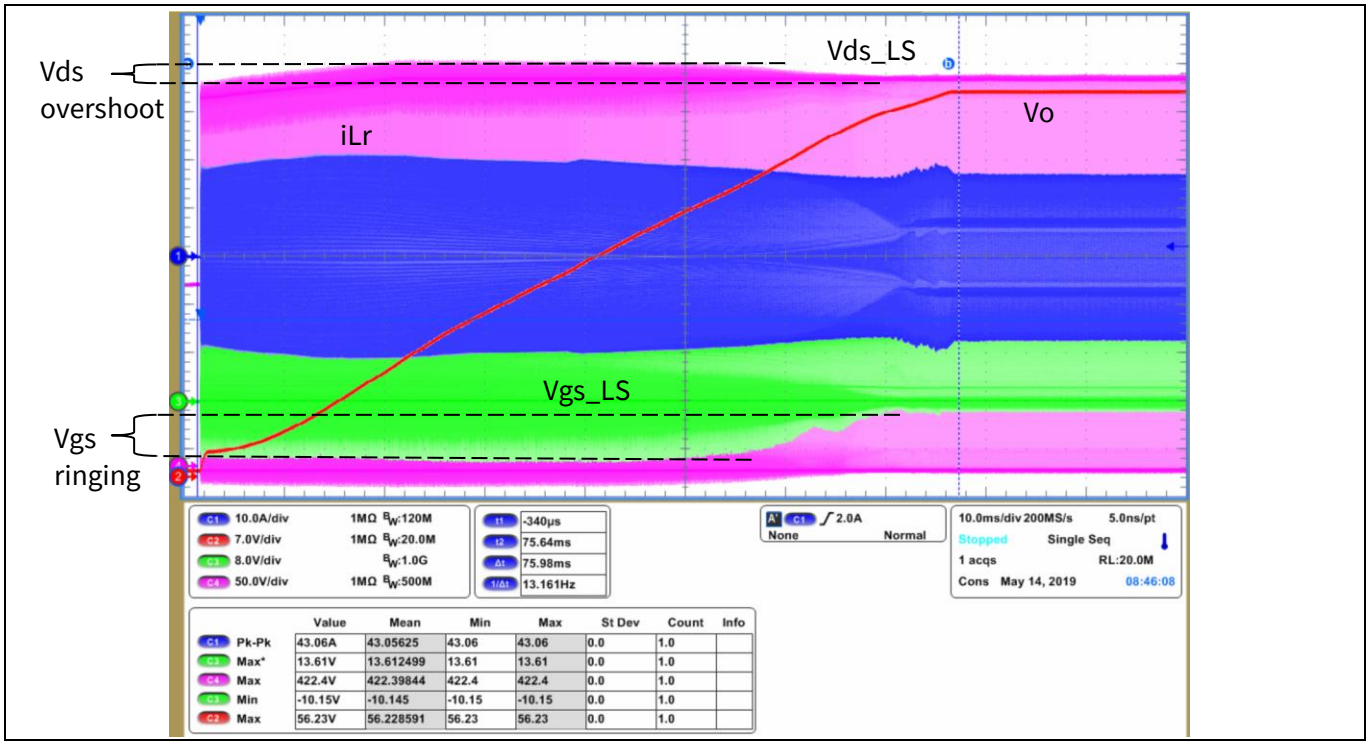

Figure 43 **Start-up sequence at 40 A load, 400 V input and 55.5 V output. The maximum voltage overshoot-undershoot in drain and gate of the HV MOSFETs occurs during the start-up, where the HB operates with the highest turn-off currents**

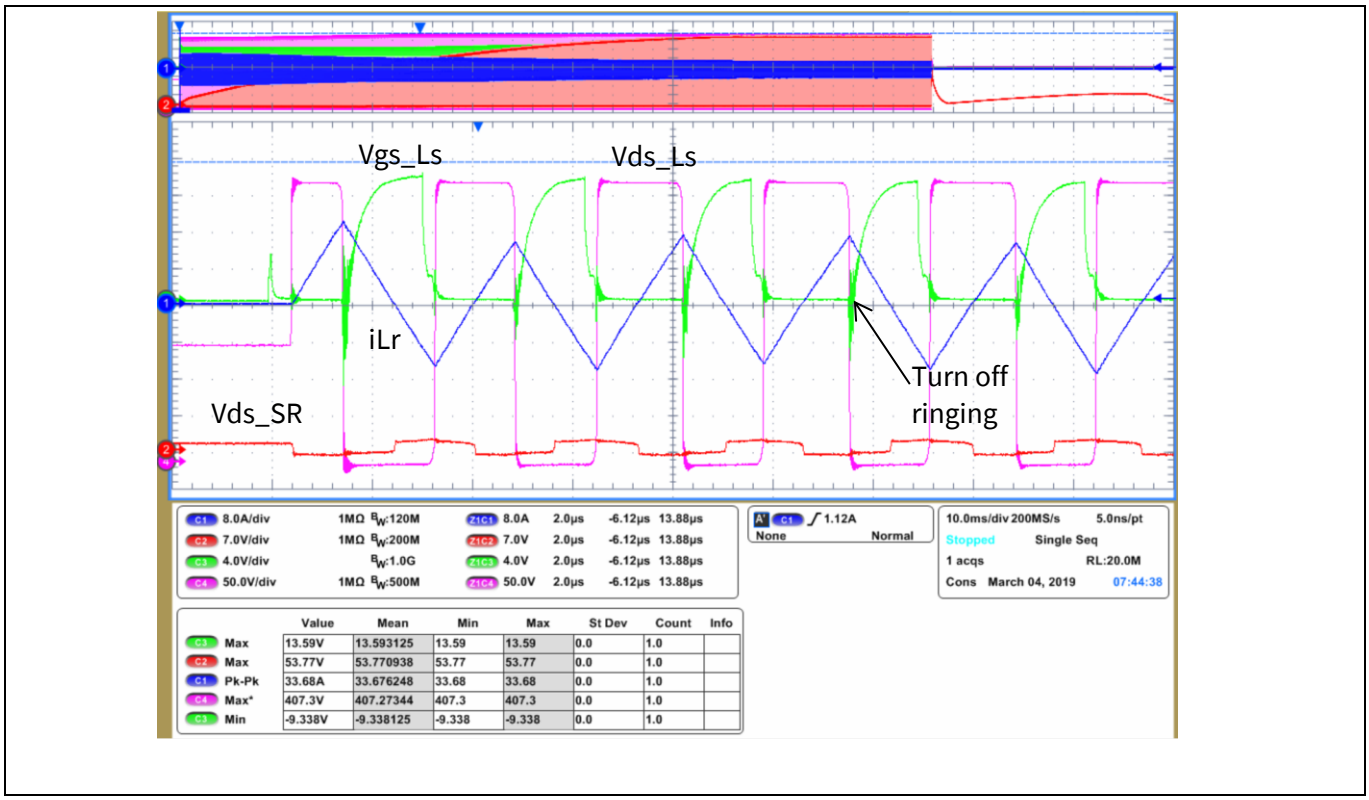

Figure 44 **Starting-up sequence. The pulse sequence at the start ensures ZVS of the HB devices while maintaining the peak-to-peak current within reasonable values**

2.2.5 Resonant tank

The current through the primary side of the converter is nearly perfectly sinusoidal at the resonant frequency, around 70 kHz (Figure 45).

The resonant capacitor voltage at full load and during the start-up sequence is plotted in Figure 46 and Figure 47 respectively.

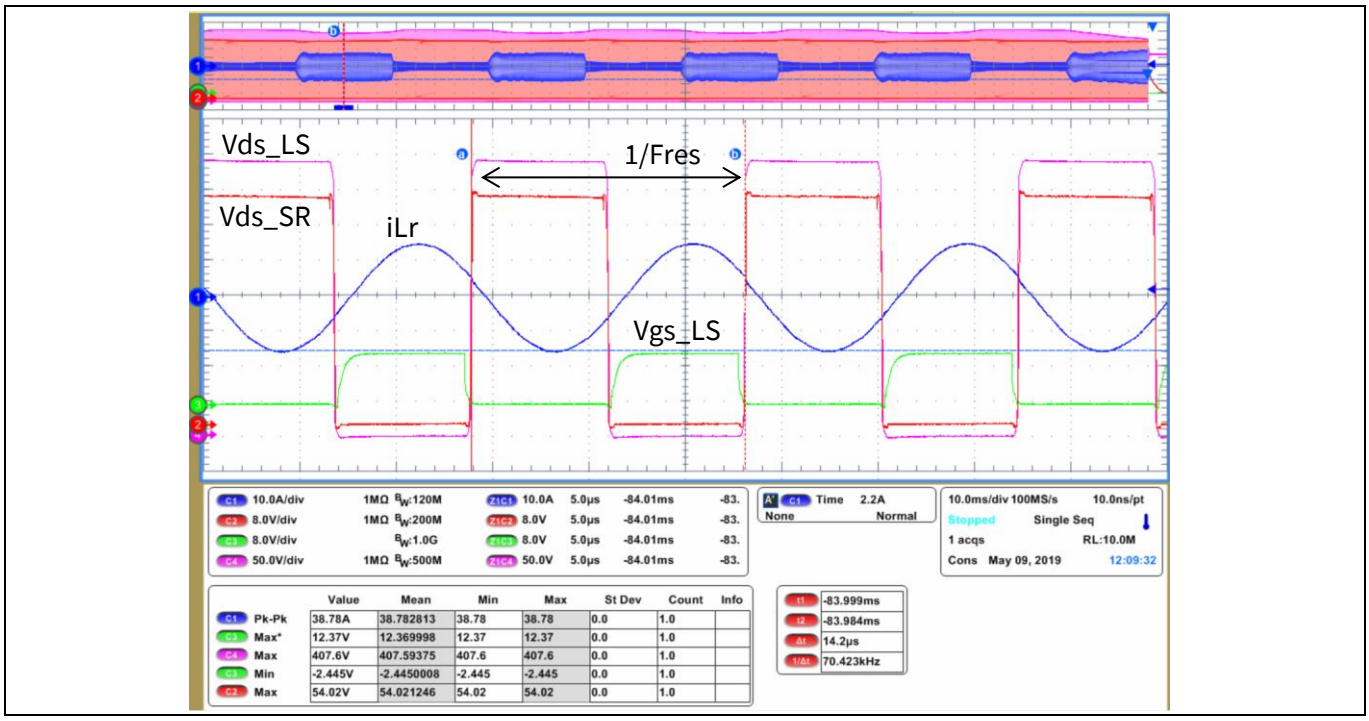

Figure 45 Resonance frequency. Characteristic sinusoidal current through Lr at the resonant frequency of the resonant tank

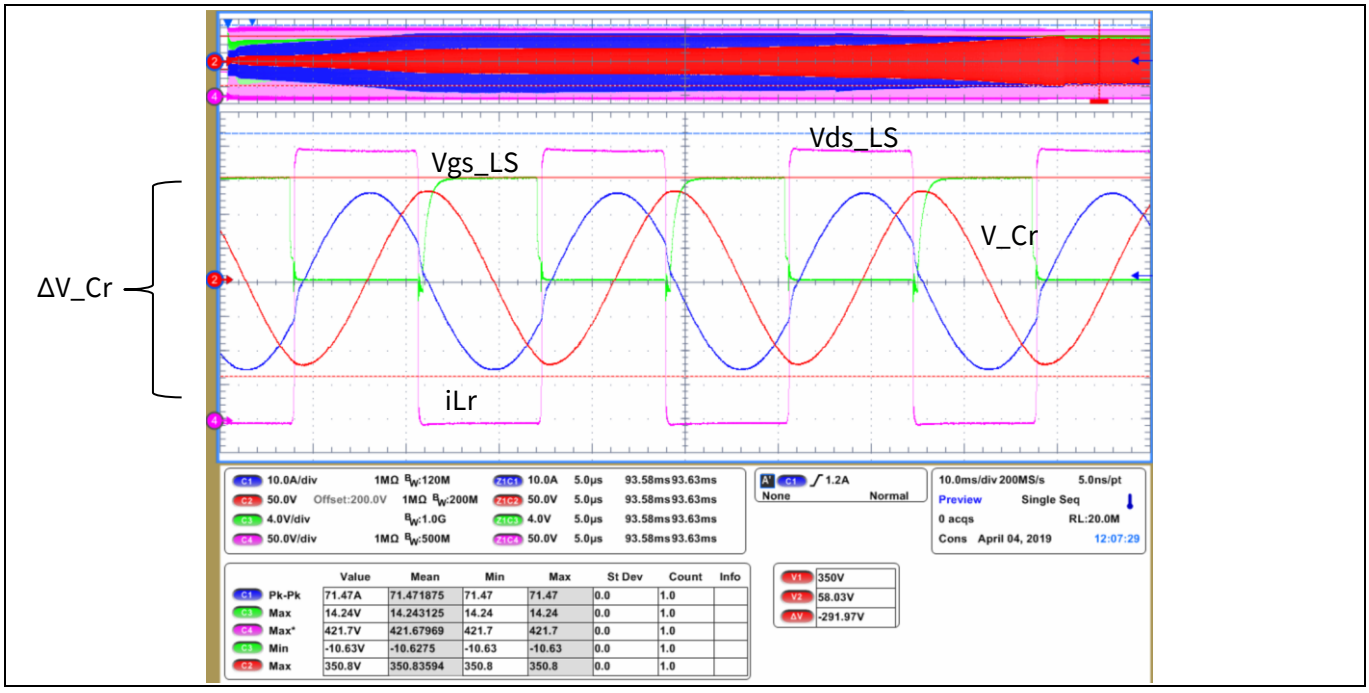

Figure 46 C_r at full load (65 A), nominal input 400 V and nominal output 51.5 V

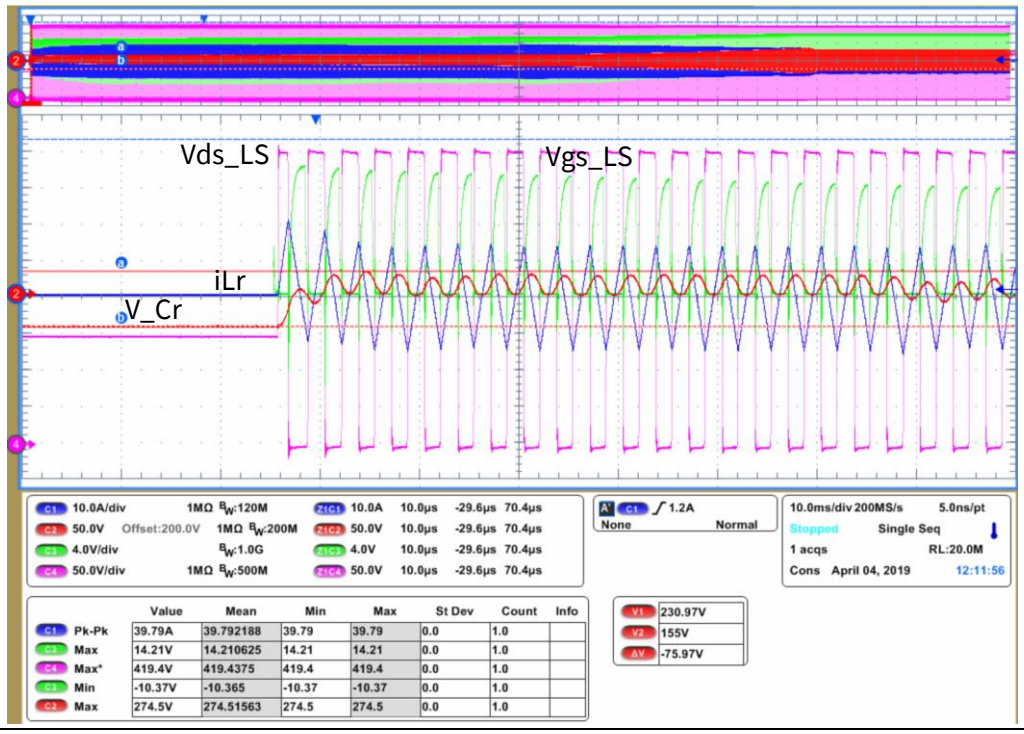

Figure 47 **C_r during start-up at nominal input 400 V and nominal output 51.5 V**

2.2.6 Brown-in and brown-out

The converter starts up above 375 V input and shuts down under 350 V (Figure 48), giving enough room for the operation during hold-up time when the LLC converter is part of a full AC-DC power supply. The amount of bulk capacitance required during hold-up time can be calculated with the equation (7).

$$C_{bulk}\frac{(V_{in,nom}-V_{in,min})^2}{2}=\frac{P_{o,max}}{\eta_{DCDC}}T_{hold}$$

Equation 7

At the lower input voltages the converter operates deep under resonance (Figure 49).

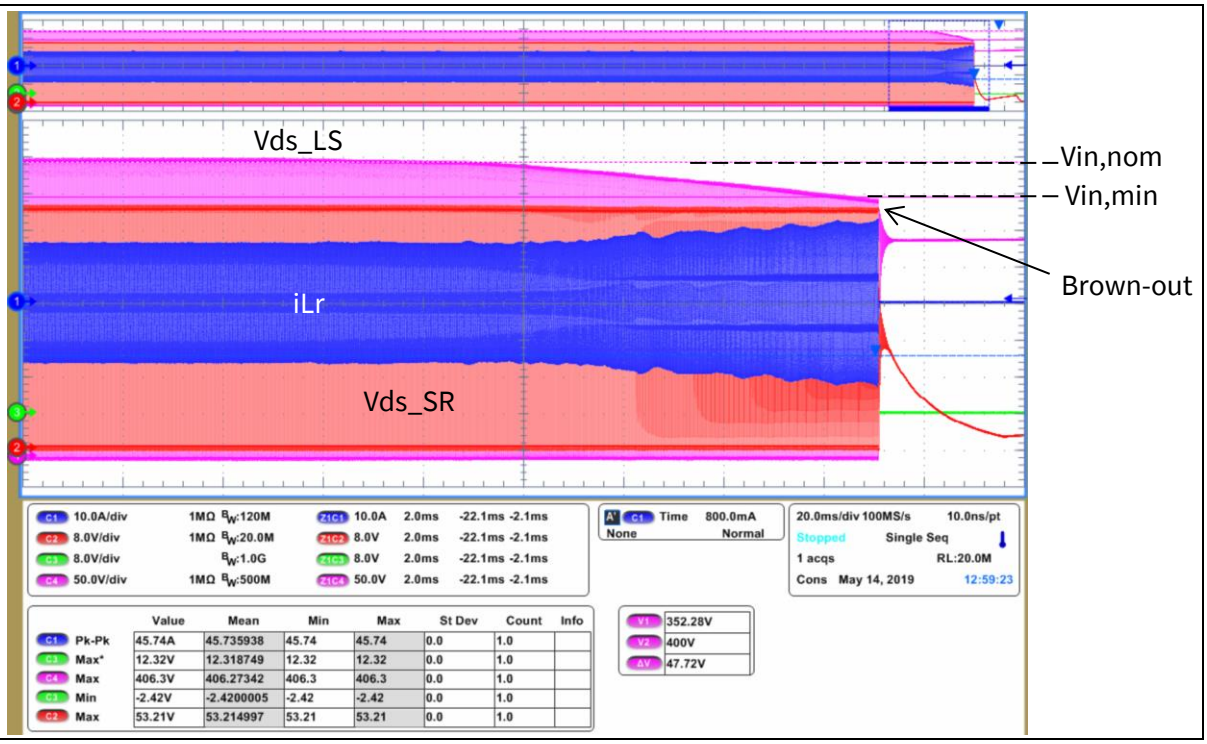

Figure 48 **Brown-out. The converter turns off when the input voltage falls under approx. 350 V**

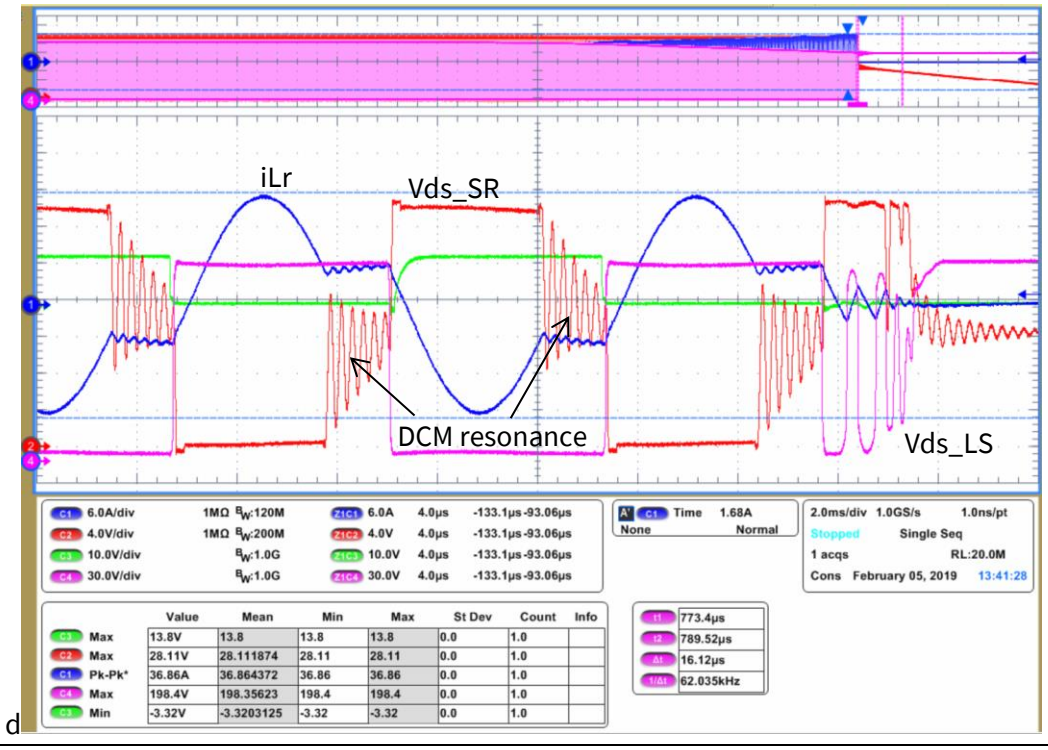

Figure 49 **Brown-out. The converter operates deep under resonance when the input voltage decays (boost operation). A similar scenario would occur during the hold-up time operation**

2.2.7 Overcurrent protection

Several redundant protection mechanisms have been implemented on the fully digital control solution with XMC™ microcontrollers from Infineon. The multiple protections ensure reliable operation under any operating conditions of the converter.

Specifically for the over-load protection or OCP of the converter, also including solutions in the hardware, these are the main mechanisms:

- Clamping diodes on the primary side of the converter. Limits the maximum current and voltage ripple on the resonant tank capacitors. Moreover, limits the primary- and secondary-side maximum peak currents
- Cycle-by-cycle peak current limit. An integrated analog comparator within the XMC™ limits the maximum primary-side peak current to 40 A (Figure 50)
- Maximum average output current. The average output current of the converter is measured through a resistive shunt. The maximum average load current is limited to 68 A with a programmable time delay (Figure 51). The maximum average current limit varies at higher output voltages to avoid the clamping diodes' conduction in steady-state (Figure 11)
- Output UVLO. In the event of short-circuit or strong overloads, the output voltage of the converter drops out of control. The converter detects the abnormal working conditions when the voltage goes out of a ±3 V window around the output voltage reference setting

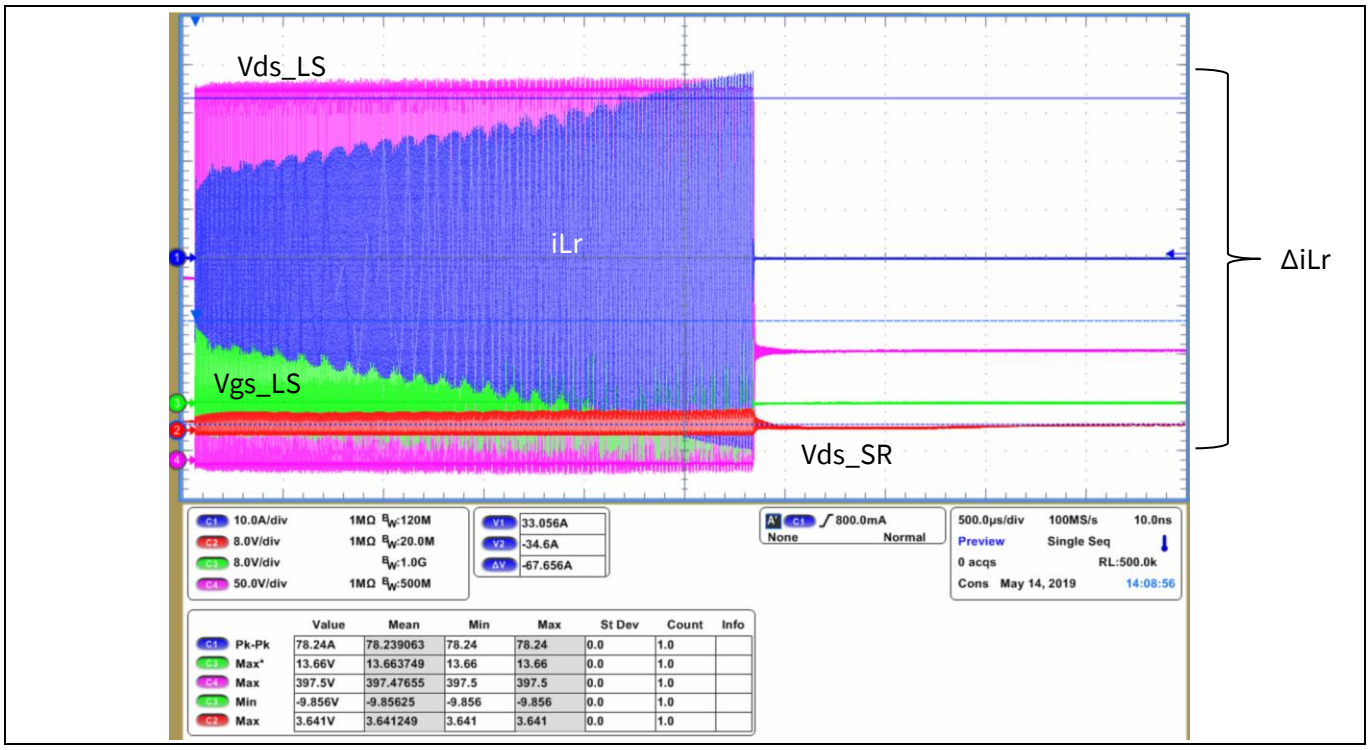

Figure 50 OCP at start-up. Several redundant protection mechanisms protect the converter from overload at start-up: cycle-by-cycle peak current limit, maximum load current and voltage rise time-out

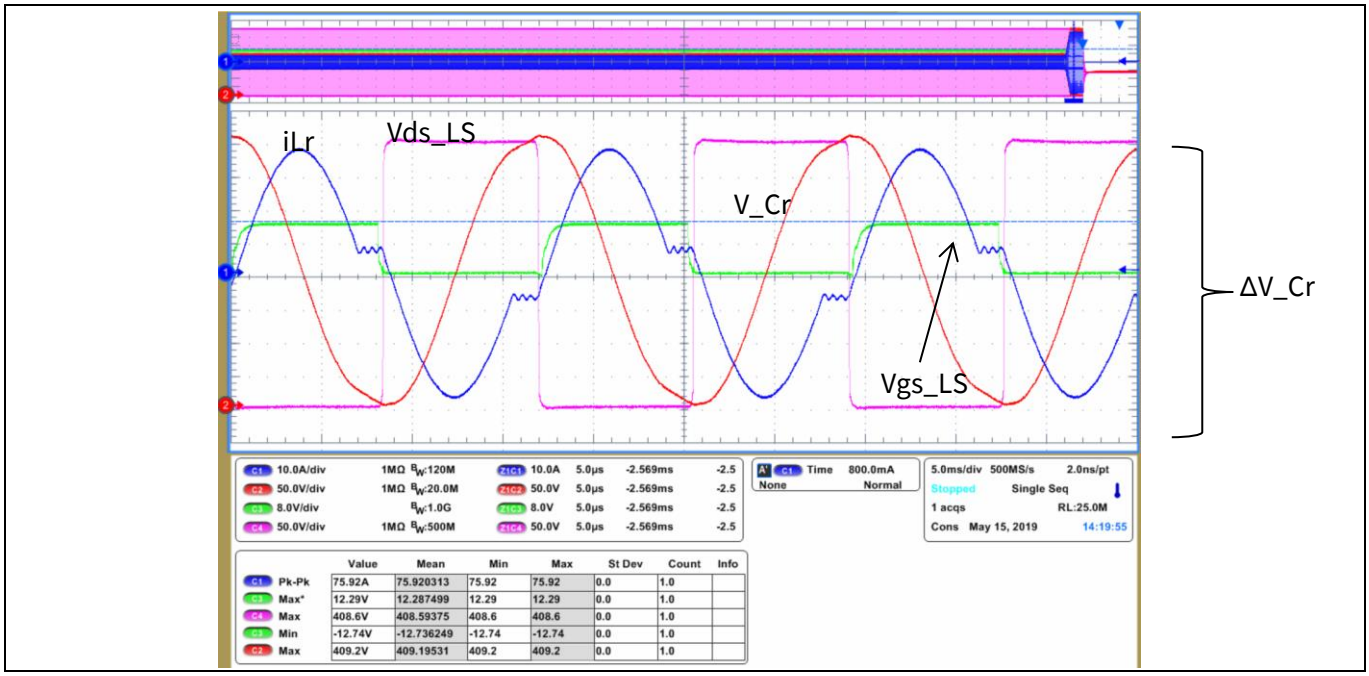

Figure 51 OCP, slow mechanism

2.2.8 Burst mode operation

For further reduction of power losses under light-load conditions the controller implements burst mode operation. The threshold of burst is adaptive for the different output voltages (Figure 13).

The implemented algorithm limits the maximum switching frequency of the converter and enters burst mode when the output voltage goes above a programmable threshold over the reference value ($V_{o,ref}$ + 750 mV) (Figure 52).

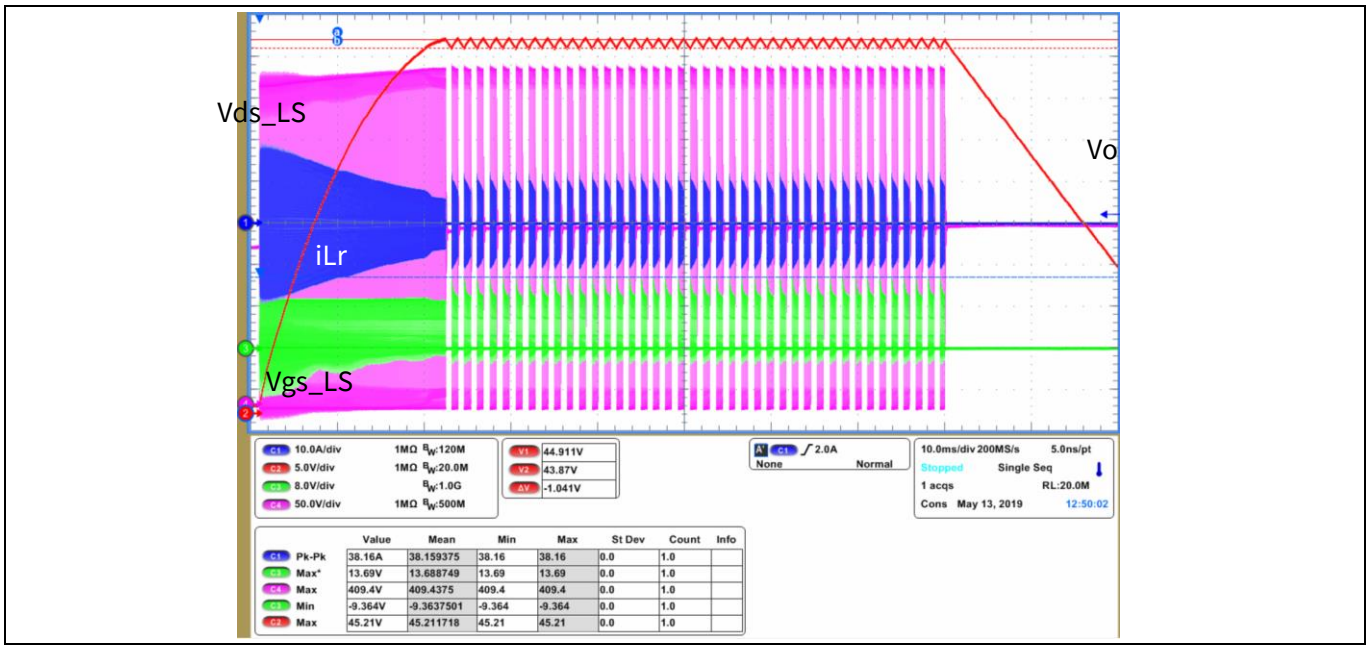

Figure 52 Burst mode. Start-up and stop at light load conditions: 4 A load, 400 V input and 43.5 V output

Burst mode ensures that in every condition the HV MOSFETs operate under full or partial ZVS (Figure 53 and Figure 54) which reduces the power loss and maintains the smooth QR transitions of the drain and gate voltages (resulting in little or no overshoots and better EMI).

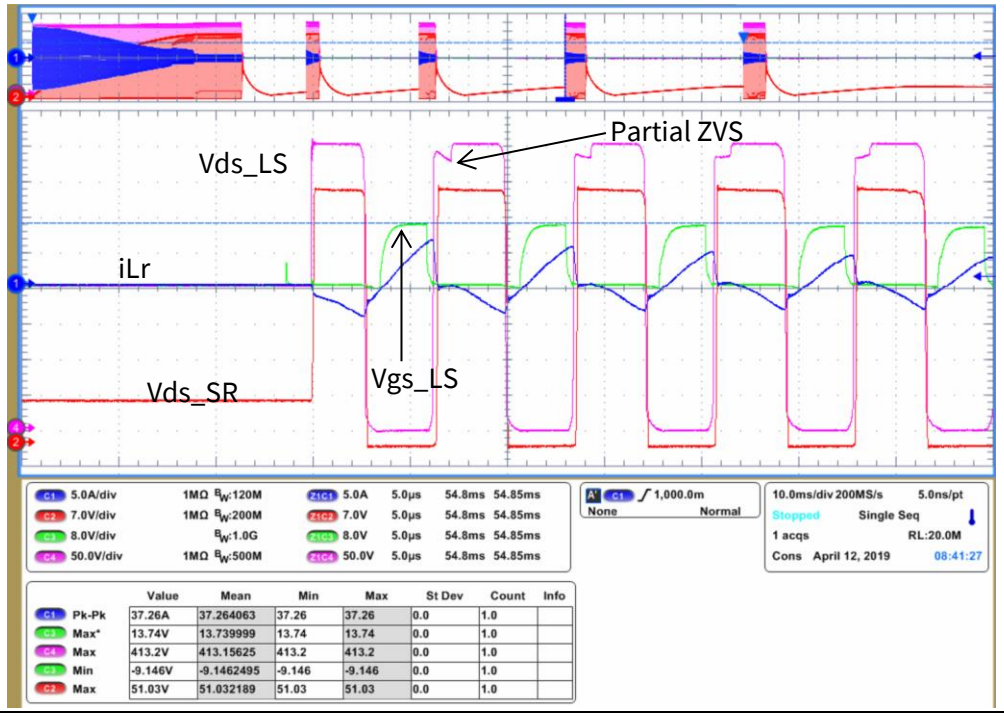

Figure 53 **Burst mode. The switching resumes in ZVS, without overshoot or current stress**

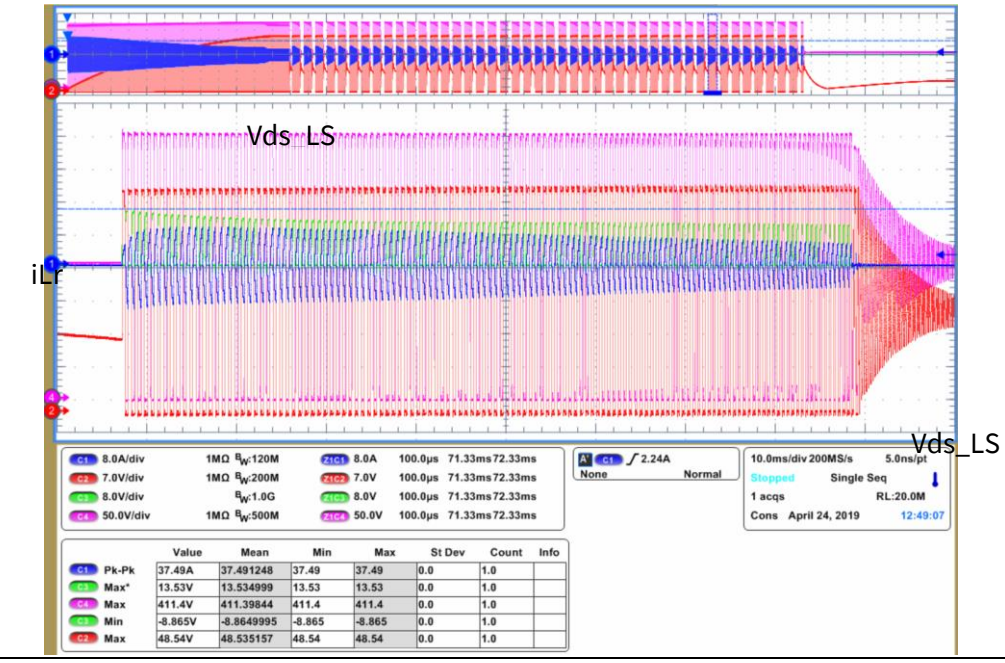

Figure 54 **Burst mode. Full burst sequence. The switching resumes in ZVS, without overshoot or current stress**

2.3 Thermal map

The temperatures of the main components of the converter were discussed in the previous sections. The following figures show the thermal distribution of the converter, from bottom (Figure 55) and top view (Figure 56), operating at full load and nominal conditions: 400 V input and 51.5 V output.

The hottest spot of the converter is the integrated magnetic structure. The high density of the converter concentrates the losses of the secondary-side MOSFETs, the transformer and the resonant inductance in a small area. Moreover, the open-frame design decreases the effectiveness of forced cooling solutions.

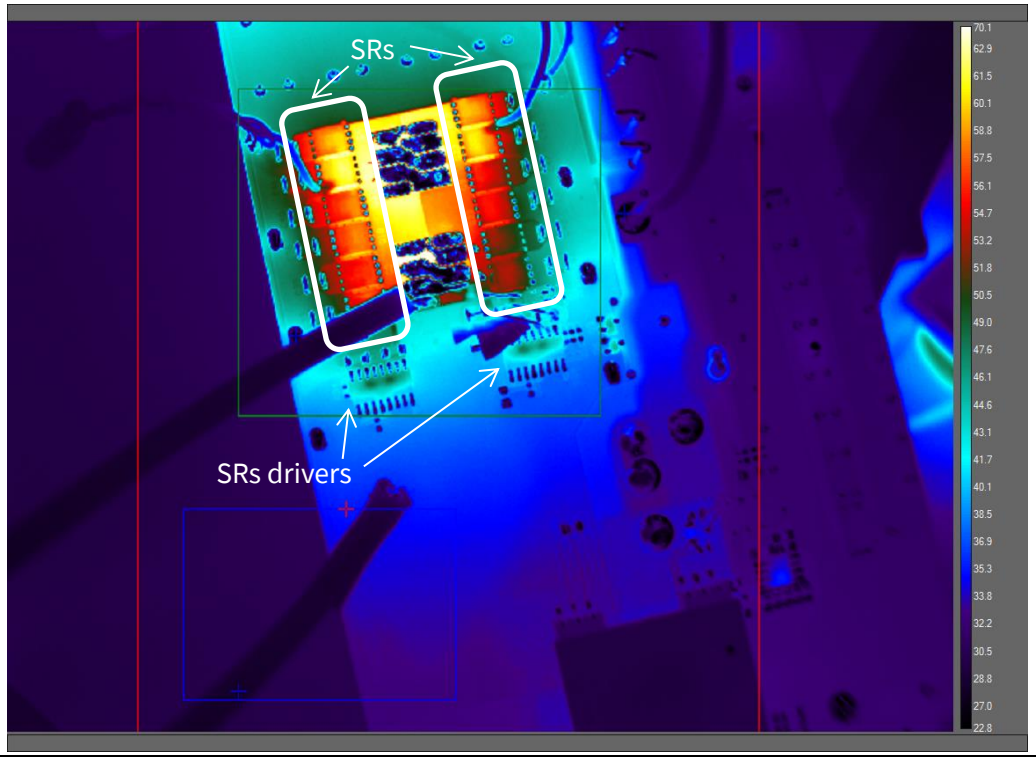

Figure 55 Thermal capture at 65 A load with open case and 25°C ambient temperature. Bottom view

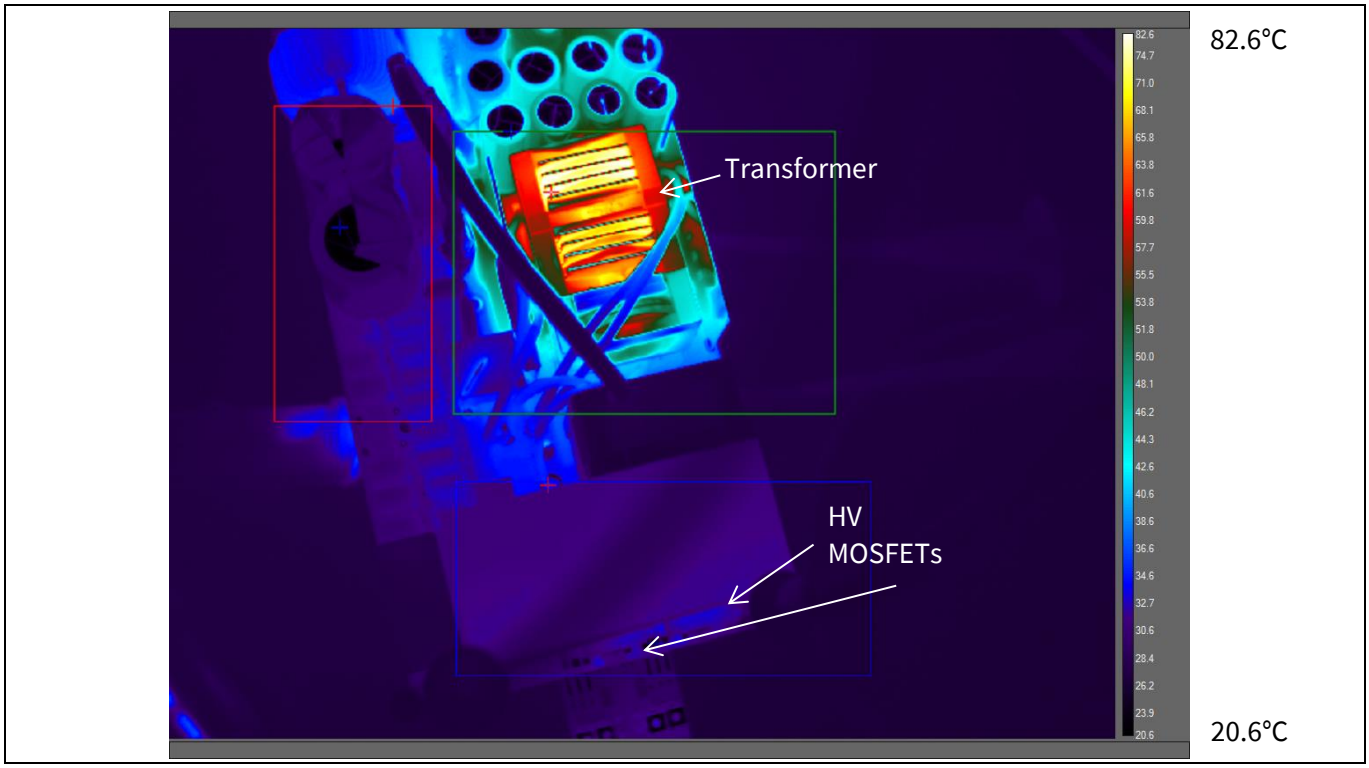

Figure 56 Thermal capture at 65 A load with open case and 25°C ambient temperature. Bottom view

3 User interface

The controller includes serial communication interface (UART) and a proprietary protocol allowing the parametrization of the HV MOSFET dead-times, output voltage settings, protection activation/deactivation and monitoring of status.

The user interface for Windows OS (Figure 57) is an example of the capabilities of the communication library included within the controller firmware. The user interface was specially developed to communicate with the controller through the XMC™ Link (converts UART to USB), although other serial communication interfaces are also possible.

There are two available versions of the GUI:

- Advanced user interface with run-time parametrization capabilities of dead-times, output voltage, protections and working modes (Figure 57)
- Simplified user interface intended for monitoring the converter during run-time (Figure 58)

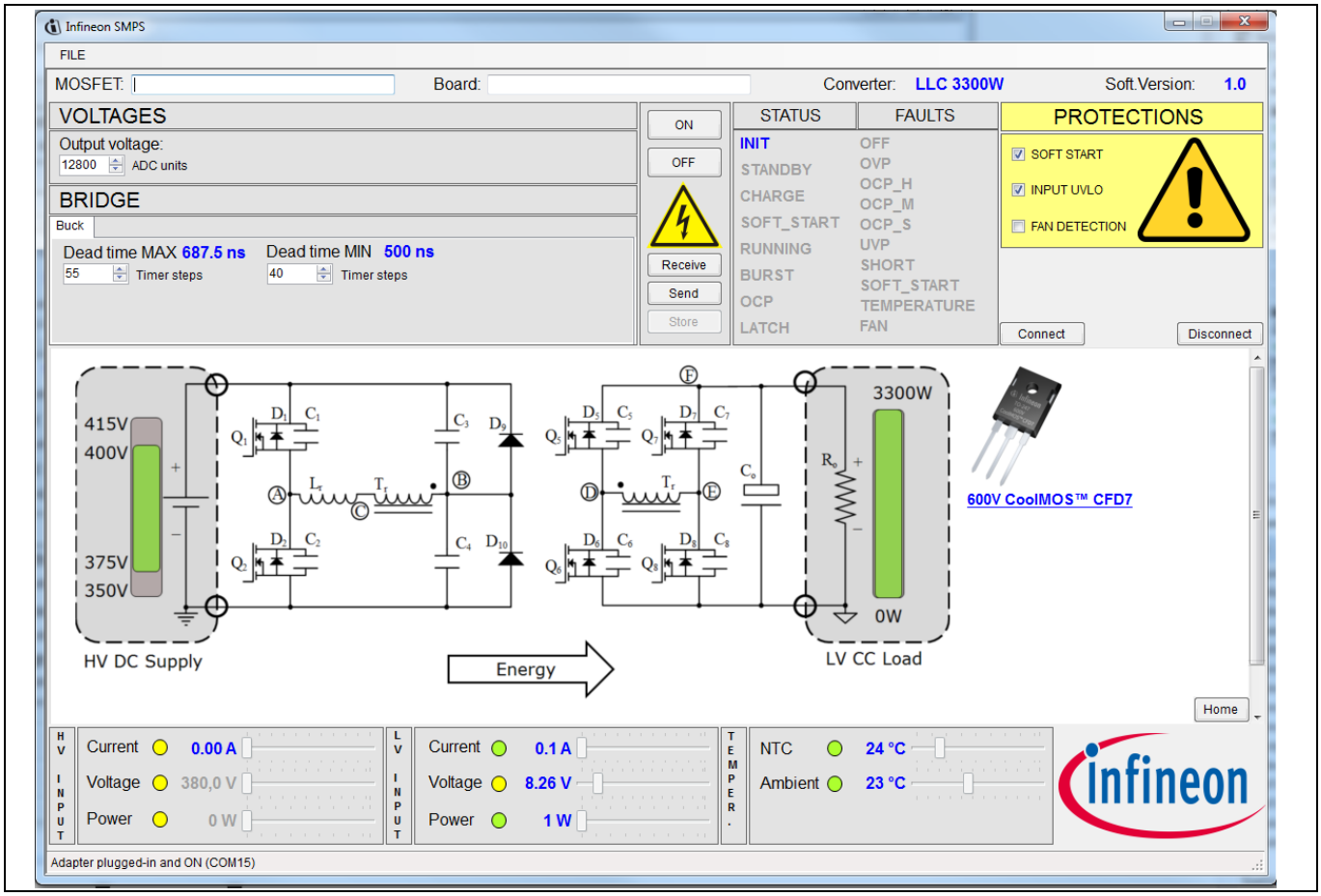

Figure 57 3300 W LLC HB advanced user interface

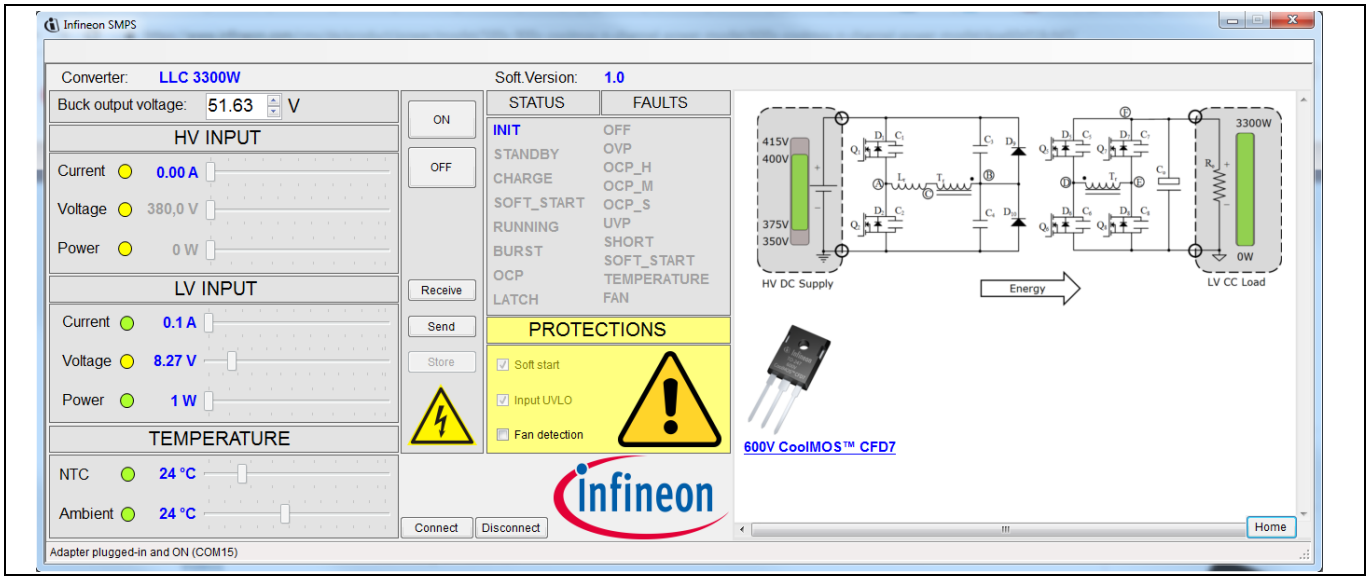

Figure 58 3300 W LLC HB simplified user interface

4 Summary

This document introduces a complete Infineon system solution for a 3300 W LLC DC-DC converter from 400 V to 51.5 V achieving 98.1 percent peak efficiency. The achieved power density is in the range of 4 W/cm^3 (66 W/in^3), which is enabled by the use of SMD packages, the innovative stacked magnetic construction and the innovative cooling solution.

Infineon's 600 V CoolMOS™ CFD7 in TO-247 package, the latest and best-performing fast body diode device from Infineon, combined with an optimized layout and an optimized driving circuitry, achieves incomparable performance with minimum stress on the devices, enabled also by the innovative cooling concepts presented in this board.

This DC-DC converter proves the feasibility of HB LLC as a high-efficiency topology for a 3300 W converter, at the level of full-bridge LLC or dual-stage LLC when combined with the latest, best-in-class Infineon devices with their benchmark low $R_{DS(on)}$ and low parasitics.

This DC-DC converter also proves that digital control, powered by Infineon XMC™ microcontrollers, is not only capable of controlling LLC topology but is also the most effective way to overcome its difficulties and pitfalls. Moreover, the included protection mechanisms and control schemes further boost the reliability and performance of the latest Infineon devices, achieving the best possible efficiency.

5 Schematics

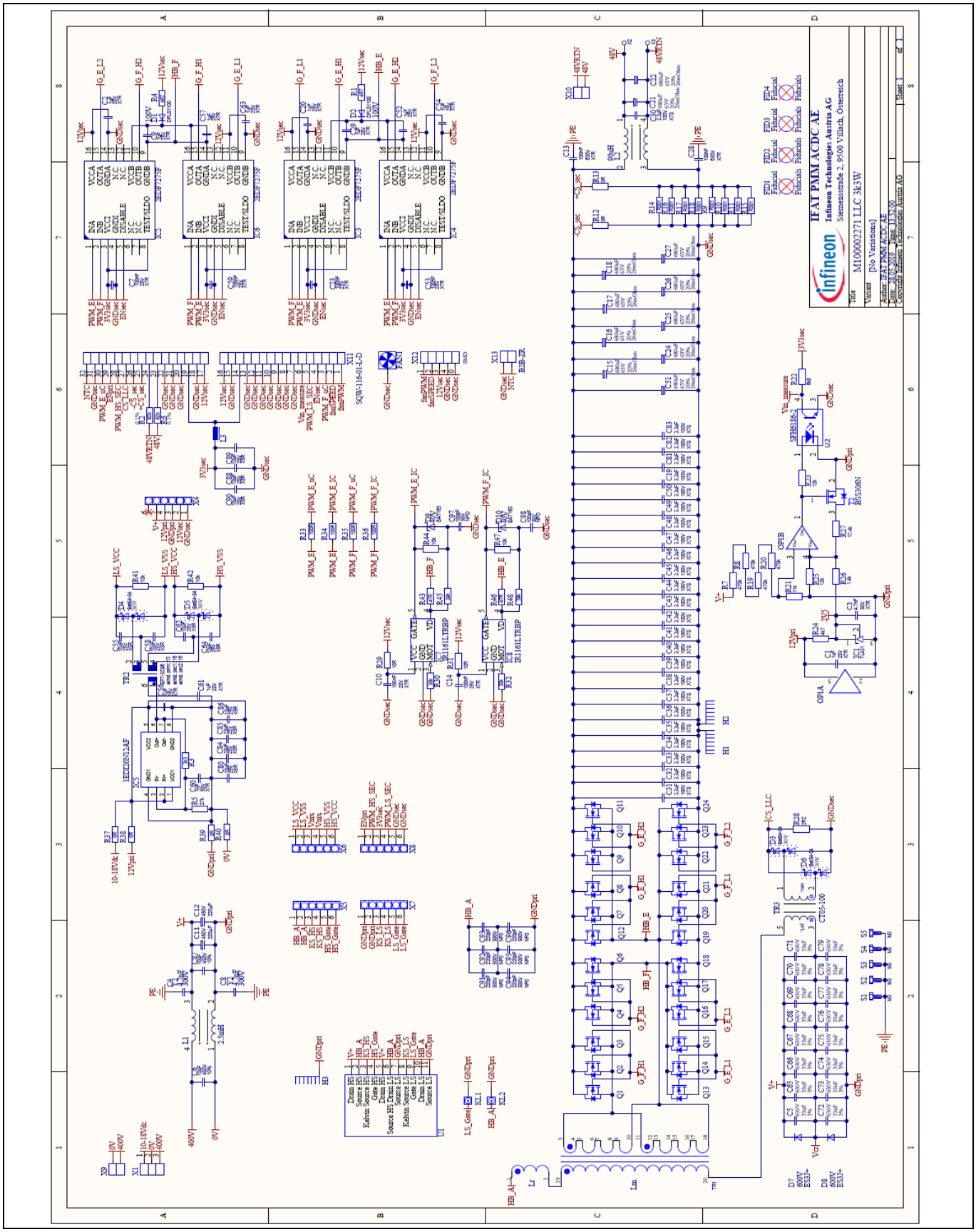

Figure 59 3300 W LLC HB main board with IPW60R018CFD7 and BSC037N08NS5

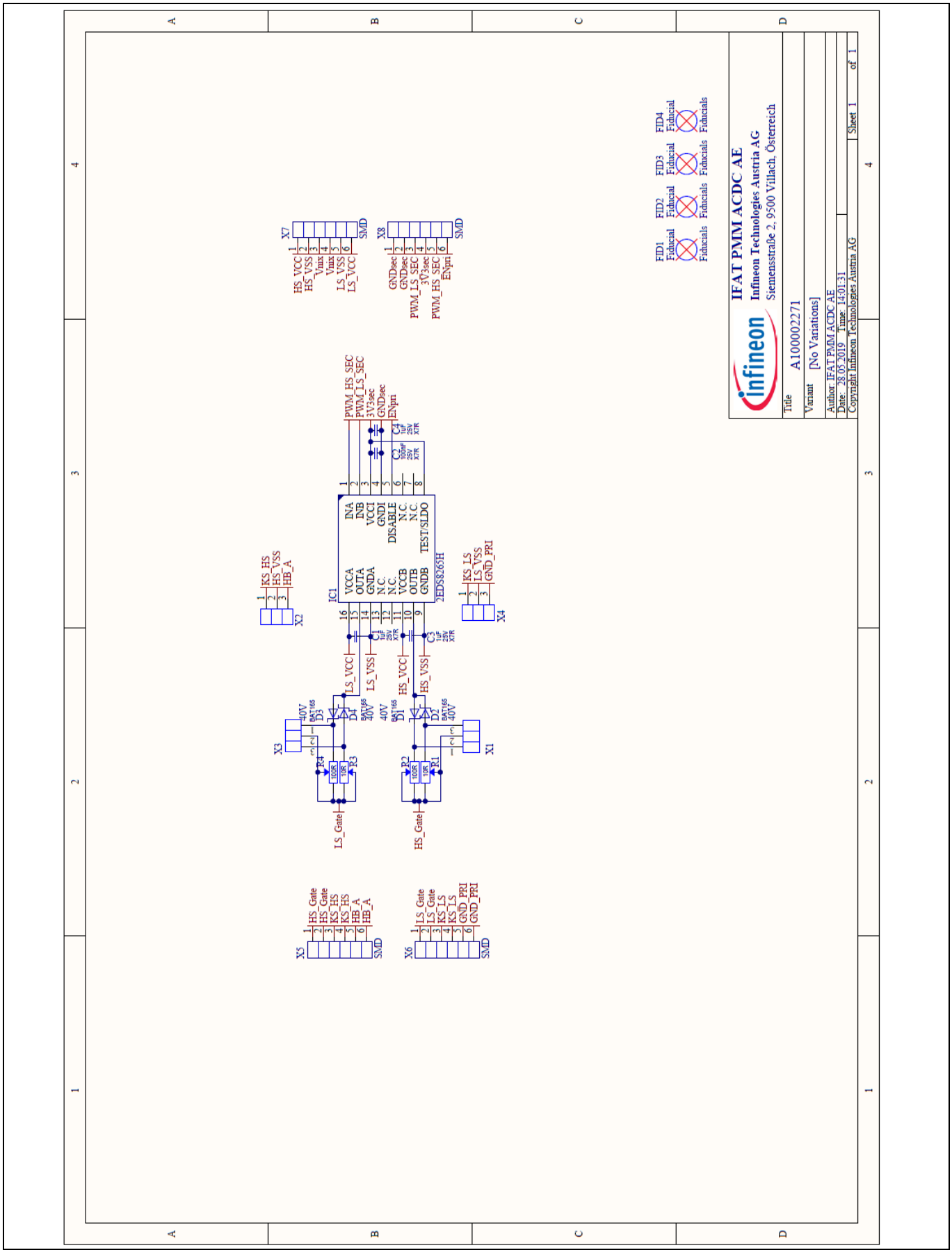

Figure 60 3300 W LLC HB driver card with 2EDS8265H

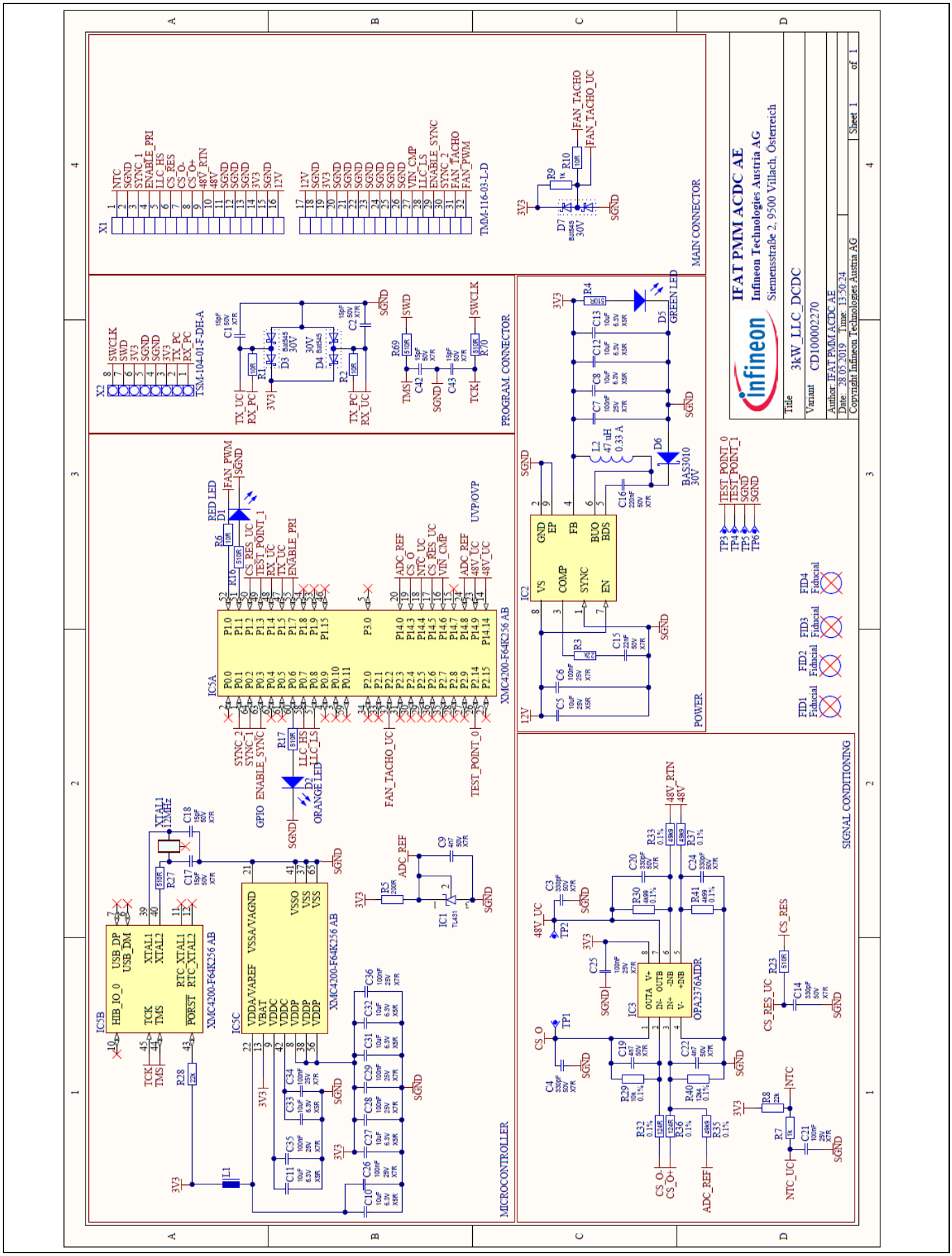

Figure 61 3300 W LLC HB controller card with XMC4200-F64K256AB

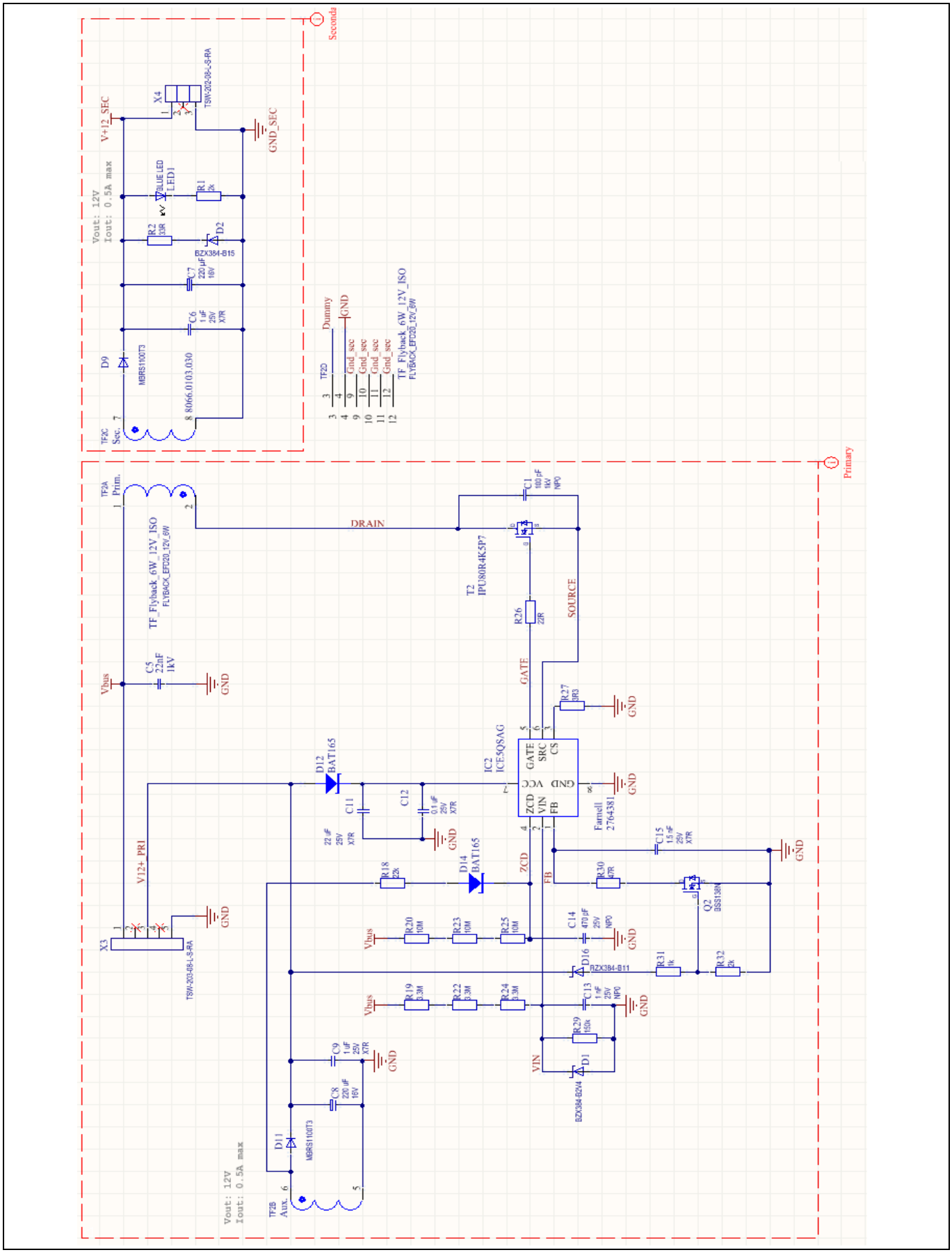

Figure 62 Auxiliary 6 W power supply

6 Bill of materials (BOM)

Parts designators in bold are produced by Infineon.

Table 2 Main board components

Designator	Value	Tolerance	Voltage	Description	Comment
T3, T4	IPW60R018CFD7		600 V	CoolMOS™	THT
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24	BSC037N08NS5			OptiMOS™	SMD
T2	BSS306N			OptiMOS™	SMD
IC5	1EDI20N12AF			EiceDRIVER™	SMD
IC2, IC3, IC4, IC6	2EDF7275F			EiceDRIVER™	SMD
IC7, IC8	IR1161LTRBP			SR controller	SMD
D9, D10	BAT165		40 V	Schottky diode	SMD
D3, D4, D5, D6	Bat54-04		30 V	Schottky diode	SMD
C1, C56	1 µF	X7R	25 V	Ceramic capacitor	SMD
C2, C9, C20, C29, C52, C54, C57, C61, C63	1 µF	X7R	25 V	Ceramic capacitor	SMD
C3	4.7 nF		50 V	Ceramic capacitor	SMD
C4, C8	4.7 nF	Y2	300 V	Ceramic capacitor	THT
C5, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79	33 nF	3 percent	630 V	Foil capacitor	THT
C6, C87	10 µF	10 percent	450 V	Foil capacitor	THT
C7, C10, C14, C23, C53, C59	100 nF	X7R	25 V	Ceramic capacitor	SMD
C11, C12	220 µF		450 V	Polarized capacitor	THT
C13, C28	100 nF	X7R	630 V	Ceramic capacitor	SMD
C15, C16, C17, C18, C21, C22, C24, C25, C26, C27, C51	680 µF	20 percent	63 V	Electrolytic capacitor	THT
C19, C30, C31, C32, C33, C34, C35, C36,	2.2 µF	X7R	100 V	Ceramic capacitor	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C81, C82, C83					
C55, C58, C62, C64, C80, C84, C85, C86, C88, C89, C90	10 µF	X5R	25 V	Ceramic capacitor	SMD
C60	1 nF	X7R	50 V	Ceramic capacitor	SMD
C91, C92, C93, C94, C95, C96	220 pF	NPO	500 V	Ceramic capacitor	SMD
C97, C98	100 pF	NPO	50 V	Ceramic capacitor	SMD
D1, D2	DFLS1100		100 V	Standard diode	SMD
D7, D8	ES3J+		600 V	Standard diode	SMD
H1, H2	HT20000280			Heatsink	THT
H3	HT10000280			Heatsink	THT
IC1	TL431			Adjustable precision shunt regulator	SMD
KL1, KL2	PK1064			Probe holder	THT
L1	2.5 mH			Inductor	THT
L2	90 µH			Inductor	THT
L3	Ferrite bead 60 Ω at 100 MHz			Magnetic	SMD
OP1	TS321IDBVR			Low-power single operational amplifier	SMD
R1, R4	4R7	1 percent		Resistor	SMD
R2, R6	82 k	0.10 percent		Resistor	SMD
R3	3k3	1 percent		Resistor	SMD
R5	27 k	1 percent		Resistor	SMD
R7, R8, R19, R20	470 k			Resistor	SMD
R9, R10, R11, R14, R15, R16, R17, R18	R001	1 percent		Resistor	SMD
R12, R13, R37, R40	0 R	1 percent		Resistor	SMD
R21	11 k			Resistor	SMD
R22	6k8			Resistor	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
R23, R25	12 k			Resistor	SMD
R24	4k7			Resistor	SMD
R26	1.4 k			Resistor	SMD
R27	17.4 k			Resistor	SMD
R28	2R2	1 percent		Resistor	SMD
R29, R31	10 R	1 percent		Resistor	SMD
R30, R32	30 k	1 percent		Resistor	SMD
R34, R36	100 R	1 percent		Resistor	SMD
R41, R42, R44, R47	10 k	1 percent		Resistor	SMD
R43, R46	47 R	1 percent		Resistor	SMD
R45, R48	39 k	1 percent		Resistor	SMD
TR1	MG100002270			Magnetic	THT
TR2	EP7-3C96			Pulse transformer	THT
TR3	CT05-100			Magnetic	THT
U2	SFH6186-2			Optocoupler	SMD
X1	MKDS 5/ 3-6,35 - 1714968			Connector	THT
X2, X3	Power element M6 with internal thread LP – 8-pin			Connector	THT
X5, X6, X7, X8	SSM-103-L-DH			Female header, 6 contacts	SMD
X9, X10	1715022 phoenix contact			Pin header	THT
X11	SQW-116-01-L-D			Pin header, 2 x 16 contacts	THT
X12	53398-0471			Pin header, 5-pole fan	SMD
X13	B2B-ZR		25 V	Connector	THT

Table 3 Control board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC5	XMC4200-F64K256 AB			XMC™	SMD
IC2	IFX91041EJ V33			IC buck	SMD
D3, D4, D7	Bat54S		25 V	Schottky diode	SMD
D6	BAS3010		50 V	Schottky diode	SMD
C1, C2, C17, C18, C42, C43	15 pF	X7R		Ceramic capacitor	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
C3, C4, C14, C20, C24	330 pF	X7R		Ceramic capacitor	SMD
C5	10 µF	X5R	30 V	Ceramic capacitor	SMD
C6, C7, C21, C25, C26, C28, C29, C34, C35, C36	100 nF	X7R	30 V	Ceramic capacitor	SMD
C8, C10, C11, C12, C13, C27, C31, C32, C33	10 µF	X5R	50 V	Ceramic capacitor	SMD
C9, C19, C22	4n7	X7R	6.3 V	Ceramic capacitor	SMD
C15	22 nF	X7R	25 V	Ceramic capacitor	SMD
C16	220 nF	X7R	50 V	Ceramic capacitor	SMD
D1	Red LED		50 V	LED	SMD
D2	Orange LED		50 V	LED	SMD
D5	Green LED		50 V	LED	SMD
IC1	TL431		50 V	Integrated circuit	SMD
IC3	OPA2376AIDR			Integrated circuit	SMD
L1	Ferrite bead 60 Ω at 100 MHz			Magnetic	SMD
L2	47 µH			WE-LQS SMD power inductor	SMD
R1, R2, R6, R10	10 R	1 percent		Resistor	SMD
R3, R8, R28	22 k	1 percent		Resistor	SMD
R4, R16, R17, R23, R27, R69, R70	510 R	1 percent		Resistor	SMD
R5	200 R	1 percent		Resistor	SMD
R7, R9	1 k	1 percent		Resistor	SMD
R29	10 k	0.1 percent		Resistor	SMD
R30, R41	4k99	0.1 percent		Resistor	SMD
R32, R36	124 R	0.1 percent		Resistor	SMD
R33, R35, R37	49k9	0.1 percent		Resistor	SMD
R40	12k4	0.1 percent		Resistor	SMD
X1	TMM-116-03-L-D			Connector	SMD
X2	TSM-104-01-F-DH-A			Female header	THT
XTAL1	12 MHz			Crystal oscillator	SMD

Table 4 Driver board components

Designator	Value	Tolerance	Voltage	Description	Comment
IC1	2EDS8265H			EiceDRIVER™	SMD
X1, X2, X3, X4	TSW-103-07-F-S			Pin header	THT
C2	100 nF	X7R	25 V	Ceramic capacitor	SMD
R1, R3	10 R			Potentiometer	SMD
R2, R4	100 R			Potentiometer	SMD

Designator	Value	Tolerance	Voltage	Description	Comment
C1, C3, C4	1 µF	X7R	25 V	Ceramic capacitor	SMD
D1, D2, D3, D4	BAT165		40 V	Schottky diode	SMD
X5, X6, X7, X8	TSM-103-01-L-DH-A			Pin header 6	SMD

7 Related resources

- 600 V CoolMOS™ CFD7
- OptiMOS™ 5 80 V and 100 V
- 2EDS8265H product page
- 1EDI20I12AF product page
- 2EDF7275F product page
- XMC4200-Q48F256 BA product page

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Document revision	Date	Description of changes
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V 1.1	2025-12-05	Lifecycle review: Updated to the latest template

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